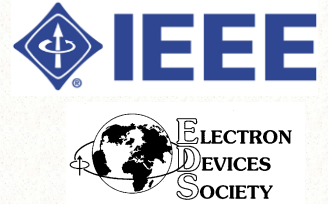




41st IEEE Semiconductor Interface Specialists Conference

December 2-4, 2010 (Tutorial: December 1)
Catamaran Resort Hotel, San Diego, CA
www.ieeesisc.org



Call For Papers

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The SISC is a workshop-style conference that provides a forum for device engineers, solid state physicists and materials scientists to discuss topics of common interest both formally through invited and contributed presentations, and informally during a various events including a poster session. The SISC is sponsored by the IEEE Electron Devices Society, and will be held **immediately prior to IEEE IEDM** (San Francisco).

The program includes talks from all areas of MOS science and technology, including but not limited to:

- **High-k gate dielectrics** and SiO₂ on Si and their interfaces
- **Insulators on high-mobility and alternative substrates** (SiGe, Ge, III-V, GaN, etc.)
- MOS gate stacks with **metal gate electrodes**
- Stacked dielectrics for **non-volatile memory**
- **Oxide and interface structure**, chemistry, defects, passivation: Theory and experiment
- **Electrical characterization, performance and reliability** of MOS-based devices
- **Surface cleaning technology** and impact on dielectrics and interfaces

SISC 2010 will further explore novel topics such as:

- Dielectrics on **nanowires/tubes, graphene**
- Correlated oxides, materials for **non-volatile memory**
- **Functional oxides and oxide electronics** (LaAlO₃/SrTiO₃ etc.)



Invited speakers

- **Prof. Chris Hinkle**, UT Dallas, USA
In-situ studies of High K oxide growth on III-V semiconductors
- **Dr. Paul Kirsch**, SEMATECH, USA
Materials and Processes for high-K Metal Gate Stacks for 28 nm and beyond
- **Dr. Koji Kita**, University of Tokyo, Japan
Understanding of GeO₂ Material Properties for Advanced Ge MIS Stacks
- **Prof. Jochen Mannhart**, University of Augsburg, Germany
Design and Fabrication of Quantum-Enhanced Capacitors for CMOS-Applications
- **Dr. Akihiro Nitayama**, Toshiba, Japan
BiCS Flash Memory technology
- **Dr. Marko Radosavljevic**, INTEL, Portland, USA
High performance InGaAs quantum well FETs with high-K dielectrics
- **Prof. Yee-Chia Yeo**, National University of Singapore, Singapore
Nanowire transistors: Performance limitations, strain engineering, reduction of parasitic resistance

Wednesday evening Tutorial – free to all registered SISC attendees

- **Dr. Matthias Passlack**, TSMC Europe, Leuven, Belgium
Interface state analysis on non-silicon semiconductors and the role of heterostructures

A **Best Student Presentation Award** will be given in memory of E.H. Nicollian.

Deadline for Receipt of Extended Abstracts: July 23, 2010

Abstract submission, previous technical programs, contacting organizers, etc., <http://www.ieeesisc.org>