

44th IEEE Semiconductor Interface Specialists Conference



Key Bridge Marriott Hotel, Arlington, VA
near downtown Washington, DC
December 5–7, 2013 (Tutorial: December 4)
www.ieeesisc.org



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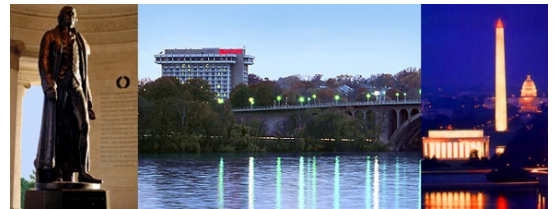
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Call for Papers

The SISC is a workshop-style conference that provides a forum for device engineers, solid state physicists, and materials scientists to discuss topics of common interest, formally through invited and contributed presentations, and informally during various events including a poster presentation session. The SISC is sponsored by the IEEE Electron Devices Society, and will be held immediately prior to the IEEE IEDM.

The program includes talks (*theory and experiment*) from all areas of MOS science and technology, including but not limited to:

- **SiO₂ and high-k gate dielectrics** on Si and their interfaces.
- **Insulators on high-mobility and alternative substrates** (SiGe, Ge, III-V and III-N, SiC, etc.)
- MOS gate stacks with **metal gate electrodes**
- Stacked dielectric layers for **non-volatile memory**
- **Oxide and interface structure**, chemistry, defects, and passivation: Theory and experiment
- **Electrical characterization, performance and reliability** of MOS-based devices
- **Surface cleaning technology** and impact on dielectrics and interfaces
- Dielectrics on **nanowires/-tubes and graphene**
- **Oxide electronics and multiferroics**
- **Interfaces in photovoltaics**, e.g. Si passivation



Invited speakers

- **Prof. Suman Datta**, Penn State University, USA
Materials Selection and Device Design for Low Power Tunnel Transistors
- **Dr. Robin Degraeve**, imec, Belgium
Modeling SET and RESET transients in Hf-based RRAM devices using the Hourglass approach
- **Dr. Thanasis Dimoulas**, NCSR DEMOKRITOS, Greece
Growth and characterization of silicene and germanene
- **Prof. Debdeep Jena**, University of Notre Dame, USA
SymFET: A novel Graphene-Insulator-Graphene Tunneling Device
- **Prof. Yasuyuki Miyamoto**, Tokyo University of Technology, Japan
Heavily doped epitaxially grown source in InGaAs MOSFET for high drain current density
- **Prof. Krishna Saraswat**, Stanford University, USA
Low Resistance MIS Contacts to Ge and III-V Devices
- **Prof. Susanne Stemmer**, University of California at Santa Barbara, USA
Reducing EOT and Interface Trap Densities of High-k/III-V Gate Stacks
- **Prof. Eric Vogel**, Georgia Institute of Technology, USA
Frequency Dispersion in CV plots of MOS Devices on III-V Substrates: Disorder-Induced Gap States or Border Traps

Wednesday evening Tutorial – free to all registered SISC attendees

- **Prof. Michelle Simmons**, The University of New South Wales, Australia
The development of a quantum computer in silicon

A **Best Student Presentation Award** will be given in memory of E.H. Nicollian.

Deadline for Receipt of Extended Abstracts: July 22, 2013

Abstract submission, previous technical programs, contact information, etc.: <http://www.ieeesisc.org>

