SISC 2015

46th IEEE Semiconductor Interface Specialists Conference

IEEE

ELECTRON DEVICES SOCIETY

Key Bridge Marriott, Arlington, VA
December 2–5, 2015 (Tutorial: December 2)
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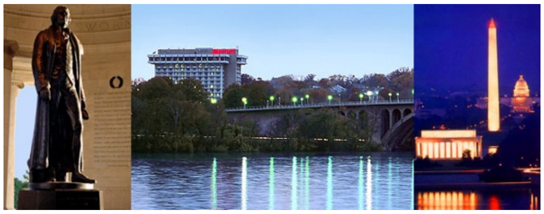
Call for Papers



The SISC is a workshop-style conference that provides a forum for device engineers, solid state physicists, and materials scientists to discuss topics of common interest, formally through invited and contributed presentations, and informally during various events including a poster presentation session. The SISC is sponsored by the IEEE Electron Devices Society, and will be held immediately prior to the IEEE IEDM.

The program includes talks (*theory and experiment*) from all areas of MOS science and technology, including but not limited to:

- **SiO_2 and high-k gate dielectrics** on Si and their interfaces.
- **Insulators on high-mobility and alternative substrates** (SiGe, Ge, III-V and III-N, SiC, etc.)
- MOS gate stacks with **metal gate electrodes**
- Stacked dielectric layers for **non-volatile memory**
- **Oxide and interface structure**, chemistry, defects, and passivation: Theory and experiment
- **Electrical characterization, performance and reliability** of MOS-based devices
- **Surface cleaning technology** and impact on dielectrics and interfaces
- Dielectrics on **nanowires/-tubes** and **graphene**
- **Oxide electronics** and **multiferroics**
- **Interfaces in photovoltaics**, e.g. Si passivation
- **2D materials and devices** and their interfaces

Confirmed invited speakers

- **Dr. Mikhail Baklanov**, imec, Belgium
  Ultralow-k Insulating Materials for 10-nm Technology Node and Beyond
- **Prof. Massimo Fischetti**, UT Dallas, USA
  Physics of Electronic Transport in Low-Dimensionality Materials for Future FETs
- **Prof. Andrew Kummel**, UCSD, USA
  Monolayer Organic Films for Nucleation of ALD on Single Layer Graphene and TMD surfaces
- **Prof. Masaaki Kuzuhara**, Fukui University, Japan
  GaN-based HEMTs for High-voltage and Low-loss Power Applications
- **Prof. Blanka Magyari-Kope**, Stanford University, USA
  Microscopic Aspects of Conductive Filaments Evolution in Metal Oxide RRAM devices
- **Dr. Alessandro Molle**, MDM Laboratory, Agrate Brianza, Italy
  Silicon at the Two-Dimensional Limit: The Debut of the Silicene Transistor
- **Prof. Akira Toriumi,** University of Tokyo, Japan
  Materials and Process Controls for Scaled Germanium Gate Stacks
- **Prof. Wenjuan Zhu,** University of Illinois, Urbana-Champaign, USA
  Two-dimensional Layered Materials and Nano-scale Devices

Wednesday evening Tutorial – free to all registered SISC attendees

- **Dr. Iuliana Radu**, imec, Belgium
  Spin Logic Options for Beyond or Along CMOS

A **Best Student Presentation Award** will be given in memory of E.H. Nicollian.

Deadline for Receipt of Extended Abstracts: August 10, 2015

Abstract submission, previous technical programs, contact information, etc.: **http://www.ieeesisc.org**