47th IEEE Semiconductor Interface Specialists Conference

SISC 2016

Catamaran Hotel, San Diego, CA
December 8–10, 2016 (Tutorial: December 7)
www.ieeesisc.org

Call for Late News Papers

Following a long-standing tradition of discussing the most recent experimental and theoretical results, the SISC invites you to submit a **Late News Paper.** The SISC is a workshop-style conference that provides a forum for device engineers, solid state physicists, and materials scientists to discuss topics of common interest, formally through invited and contributed presentations, and informally during various events including two poster presentation sessions.

The program includes talks and poster presentations from all areas of MOS science and technology, including but not limited to:

- **SiO_2 and high-k gate dielectrics** on Si and their interfaces
- **Insulators on high-mobility and alternative substrates** (SiGe, Ge, III-V and III-N, SiC, etc.)
- MOS gate stacks with **metal gate electrodes**
- Stacked dielectric layers for **non-volatile memory**
- **Oxide and interface structure**, chemistry, defects, and passivation: theory and experiment
- **Electrical characterization, performance and reliability** of MOS-based devices
- **Surface cleaning technology** and impact on dielectrics and interfaces
- Dielectrics on **nanowires/-tubes** and **graphene**
- **Oxide electronics** and **multiferroics**
- **Interfaces in photovoltaics**, e.g. Si passivation
- **2D materials and devices** and their interfaces

Confirmed invited speakers

- **Prof. K. Banerjee,** UCSB
  2D/3D Tunnel FETs
- **Prof. P. McIntyre,** Stanford U.
  Interface Defect Passivation for High Performance Insulator-Protected MIS Photosynthesis and Photovoltaic Cells
- **Dr. J. Müller,** Fraunhofer IPMS-CNT, Dresden, Germany
  Material Innovations in Ferroelectric Hafnium Oxide - Towards Cheaper Memories, Steeper Slopes and New Value Adders for HKMG Technologies
- **Prof. J. Robinson,** Penn State U.
  2D/3D Interfaces: Where the Magic Happens
- **Prof. S. Salahuddin,** UC Berkeley
  Negative Capacitance and Its Implications for Low Voltage Transistors
- **Prof. S. Takagi,** U. Tokyo, Japan
  Critical issues and Challenges of High-k Gate Stacks for Ge MOSFETs
- **Dr. A. Verhulst,** imec, Belgium
  Perspective on III-V Tunnel-FETs: bridging the gap between ideal device design and experimental realizations through calibration
- **Prof. L.-E. Wernersson,** Lund University, Sweden
  III-V Nanowire MosFETs and Tunnel FETs

Wednesday evening Tutorial – free to all registered SISC attendees

- **Dr. T. Theis,** Columbia Nano Initiative
  Materials and Device Architectures for Future Electronics

A **Best Student Presentation Award** will be given in memory of E.H. Nicollian.

Deadline for Receipt of Extended Abstracts: September 30, 2016

Abstract submission, previous technical programs, contact information, etc.: ***http://www.ieeesisc.org***