Gate Dielectrics, Interfaces, and SISC

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On the Occasion of the 40th SISC

Outline

- A little bit of history
- Highlights of some milestone papers
- Stories of some legendary figures
- A little bit of science
- Hopefully entertaining

How SISC Began

- 11/1965: 1st meeting, called "**Silicon** Interface Specialists Conference", was held at Las Vegas
- 3/1967: Changed to "**Semiconductor** Interface Specialists Conference" at Las Vegas
- 3/1968: 3rd meeting was also held at Las Vegas. Original mission accomplished – **mobile ion problem** solved
- 1969-1973: Conference **suspended**

1965-1968 Focus – Mobile Ions

- Identified sodium as culprit
- Developed BTS C-V and quasi-static I-V techniques for monitoring mobile ions
- Developed Na gettering technique by using phosphorus silicate glass
- Discovery of miracle HCl
  - – Oxidation tube cleaning
  - -- Na pinning/neutralization in SiO_2.

1969 - 1973

On Hiatus for 5 Years

1974 - 1976

- **1974**:

  Gary Scoggan and T.P. Ma, "**Effects of Si Dopants on Electron Beam Irradiation of MOS Capacitors,**" *1974 IEEE -SISC,* Puerto Rico

- **1976**:

  T.P. Ma and R.C. Barker, "**Anomalous Surface-Statec Time Constant in MOS Tunnel Junctions,**" *1976 IEEE-SISC,* New Orleans

T.P. Ma's Early Involvement with SISC

Radiation-Induced ΔV_{fb}, ΔV_{th}, ΔV_{mg}

- Both ΔV_{fb} and ΔV_{th} depend on dopant type (p *vs* n) and dopant concentration
- ΔV_{fb} is generally different from ΔV_{th}
- ΔV_{mg} is independent of dopant
- Explained by the nature of interface traps:

✓ Acceptor-type above midgap

✓ Donor-type below midgap

ΔV_{fb} and ΔV_{th} Due to Interface Traps

$\Delta V_{fb} = -\,Q_{it}\,(@\text{flatband})/C_{ox}$

$\Delta V_{th} = -\,Q_{it}\,(@\text{inversion})/C_{ox}$

where Q_{it} is interface trapped charge

Experimental Observation:

	N-channel FET	P-channel FET
ΔV_{fb}	–	+
ΔV_{th}	+	–

Proposed Explanation of the Experimental Results:

- **Interface Traps Above Midgap Are Acceptors:**

  -- **Neutral** when un-occupied with electrons (**above E_F**)

  -- **Negative** when occupied with electrons (**below E_F**)

- **Interface Traps Below Midgap Are Donors:**

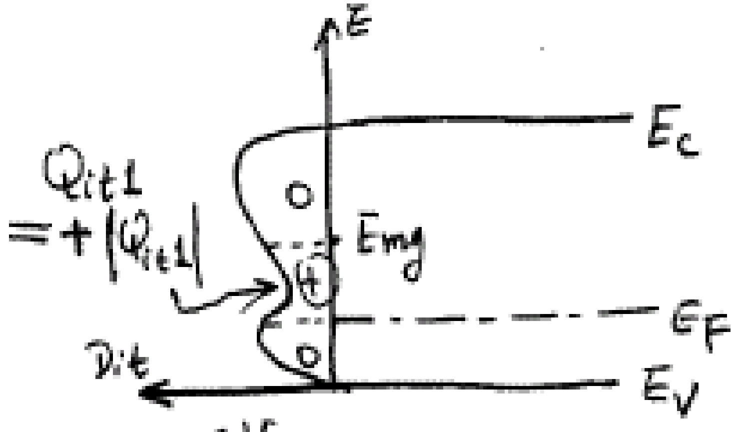
  -- **Positive** when un-occupied with electrons (**above E_F**)

  -- **Neutral** when occupied with electrons (**below E_F**)

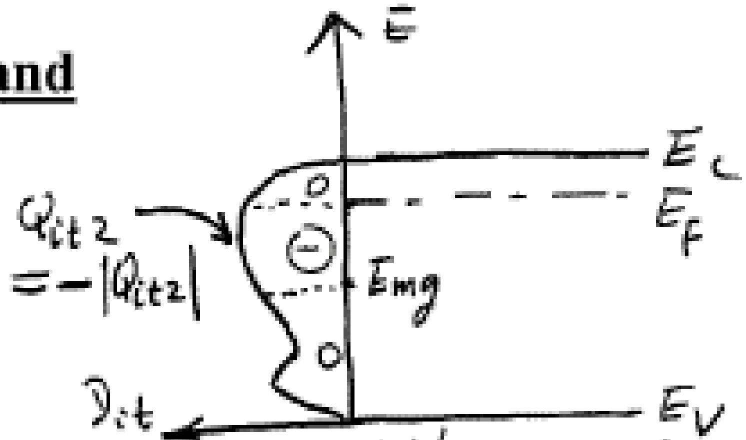
N-channel MOSFET
P-Substrate

P-Channel MOSFET
N-Substrate

Flat Band

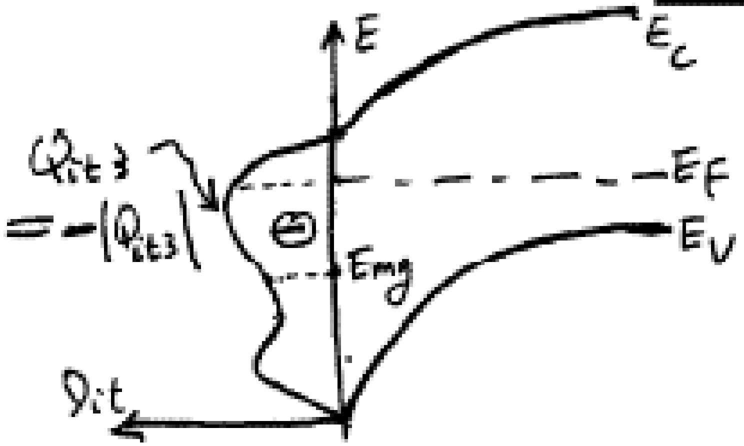


$\Delta V_{FB(n\text{-}ch)} = -$

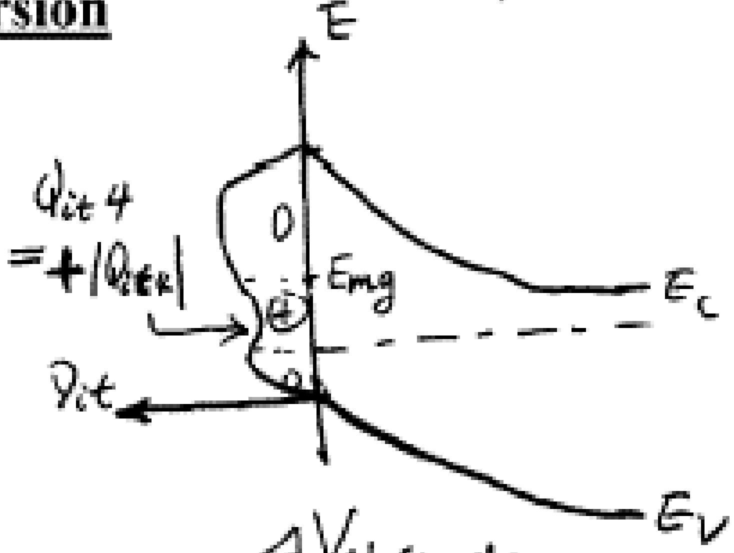


$\Delta V_{FB(p\text{-}ch)} = +$

Strong Inversion



$\Delta V_{th(n\text{-}ch)} = +$



$\Delta V_{th(p\text{-}ch)} = -$

Interface Trapped Charge,
$Q_{it} = 0$
When E_F is at Midgap

One should measure ΔVmg

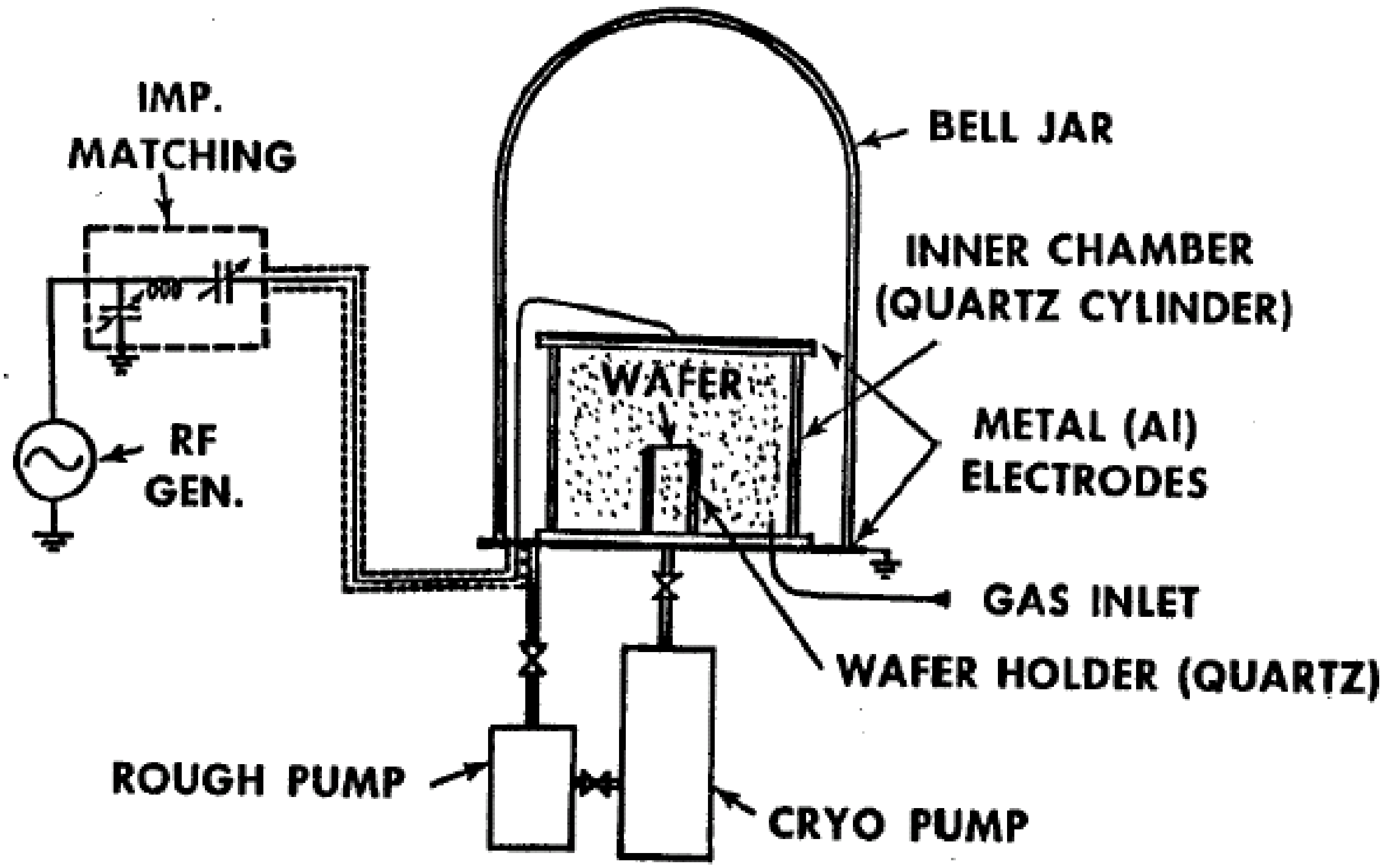
to determine oxide charge density

1977

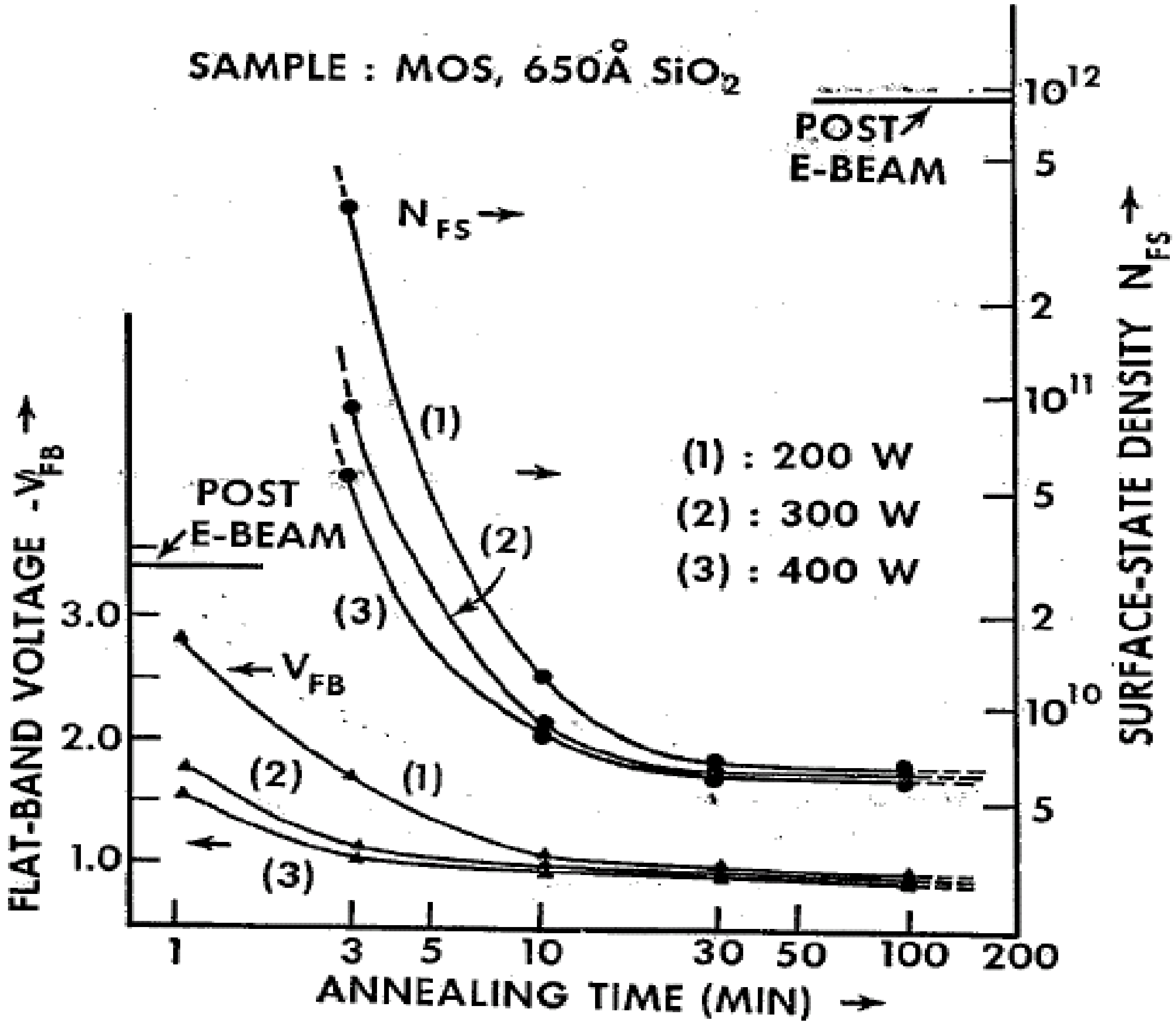
- T.P. Ma and William Ma, “**Low Pressure RF Annealing: A New Technique to Remove Charge Centers in MIS Dielectrics**“

The “**Ma Ma**” Effect

RF Plasma Annealing



RF Plasma Annealing Results

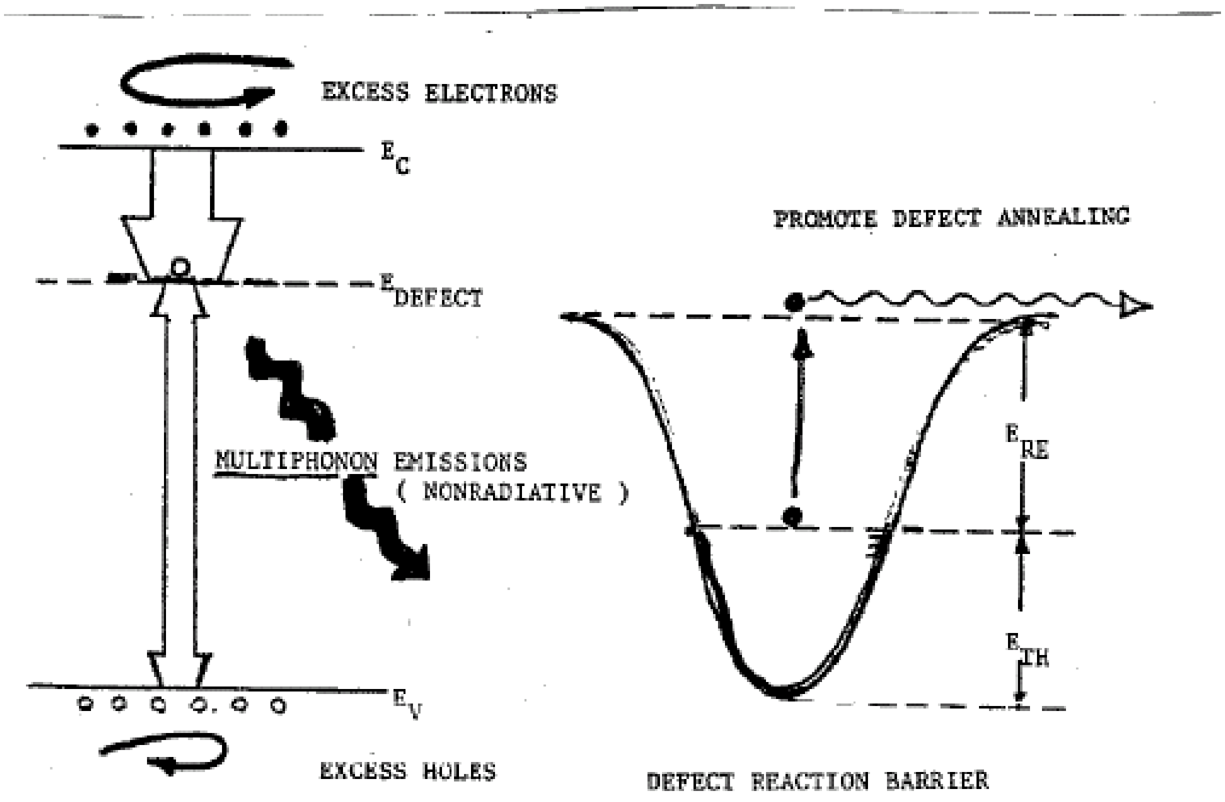


Radiation Damage Effectively Annealed Out in 10-30 Min

Possible Annealing Mechanism

- **Key Components:**
  - **Electron/Hole Pairs Generated by RF Plasma**
  - **Symmetric RF Field**
  - **Plasma Induced Wafer Temperature**

- **Recombination-Enhanced Defect Reactions (REDR)**



1979

- **S. C. Sun and J. D. Plummer**, *"Electron mobility in Inversion and Accumulation Layers on Thermally Oxidized Silicon Surfaces"*

Universal Mobility

- **P. S. Winokur, H. E. Boesch, Jr., F. B. McLean, and J. M. McGarrity**, *"Time-Dependent Buildup of Interface States Following Pulsed e-Beam Irradiation"*

Hydrogen Model

- **K.Hess, B. G. Streetman, Y. Shichijo, and H. Morkoz** , *"Real Space Transfer of Hot Electrons in A1,Gal.,As-GaAs Heterostructtlres"*

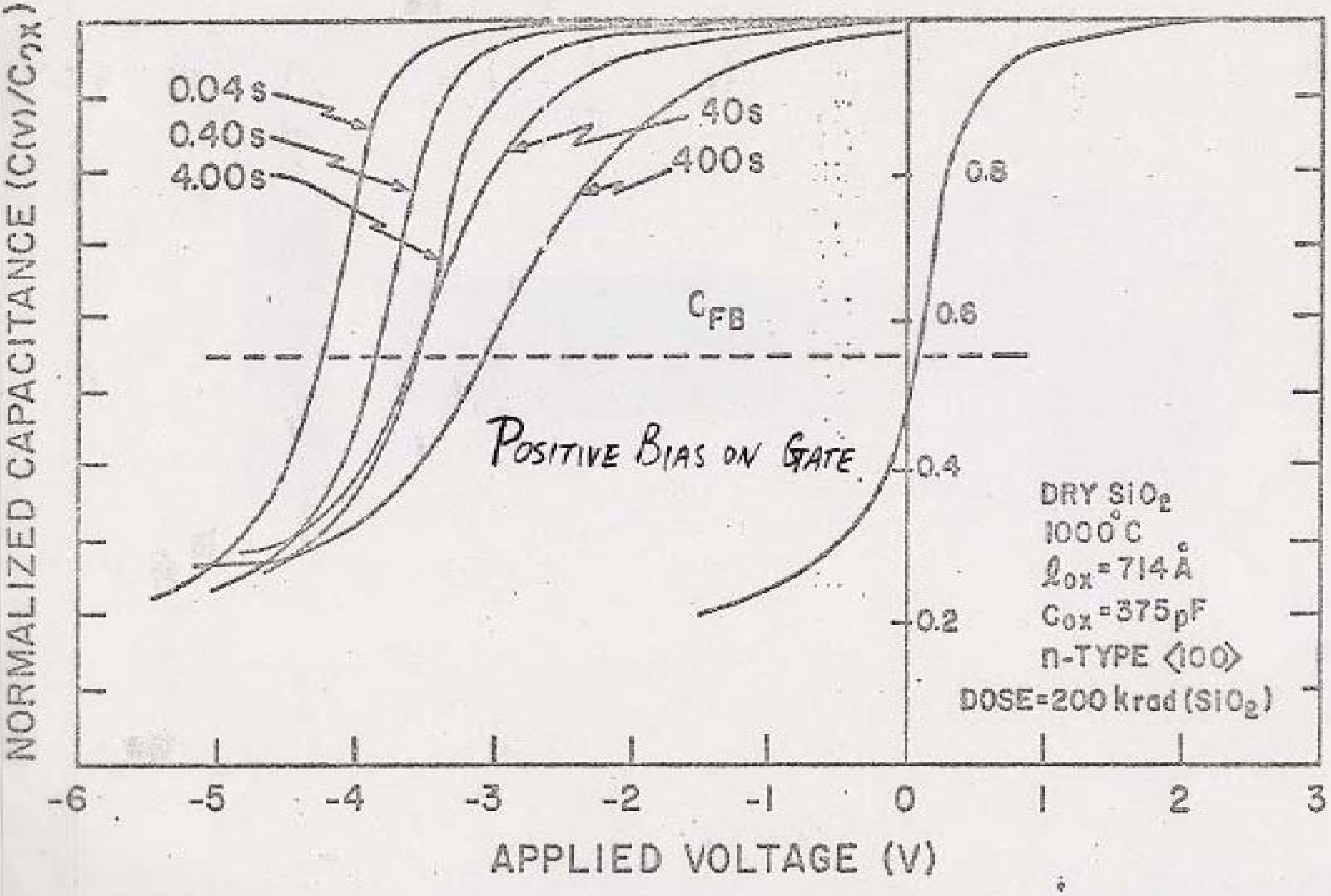
HEMT

- ***W.* E. Spicer, I. Lindau, P. Skeath, and C. Y. Su**, *"Selection of 111-V Compounds for Either Schottky Barrier or MIS Based Devices"*

~~***GaAs MIS***~~

Winokur, Boesch, McGarrity & McLean
1979

POST IRRADIATION C-V CURVES



EFFECT OF VARYING OXIDE FIELD AT SELECTED TIMES DURING ΔN_{SS} BUILDUP

Winokur, et. al

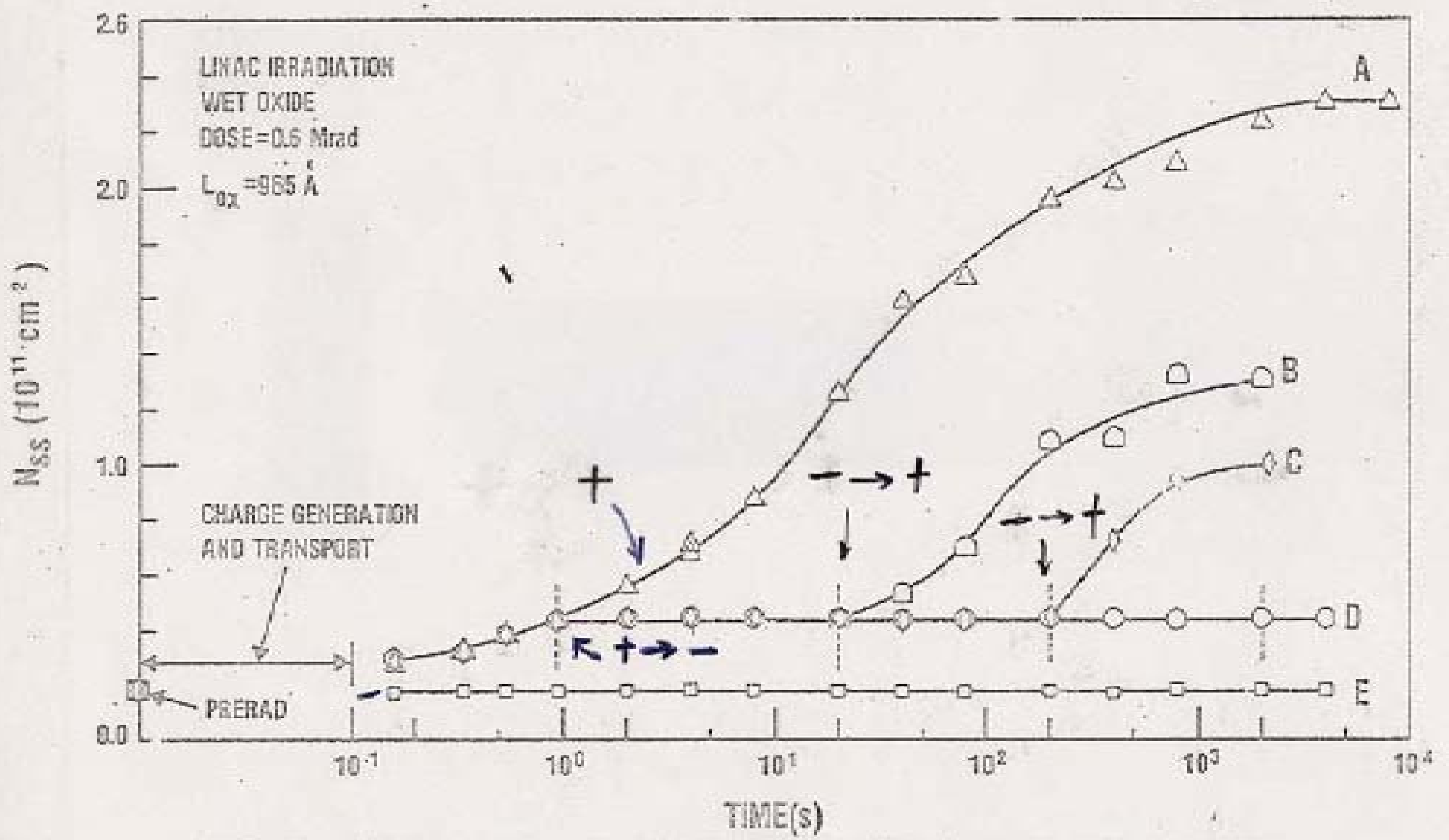


Fig. 4. Effect of reversing polarity of applied field across oxide at varying times for hardened wet-oxide capacitors, illustrating inhibiting effect of negative gate bias on N_{SS} buildup during second stage. The magnitude of the field was 4 MV/cm. Curve A: positive gate bias polarity throughout; Curve E: negative polarity thoughout; Curves B, C, D: gate bias initially positive, but polarity reversed at 1 s and then switched back to positive at 20, 200, and 2000 s, respectively.

1980

- N.Z amani and J. Maserjian, *“Oscillations in Fowler-Nordheim Tunneling as a Probe of the Si/Si02 Interface”*

Quantum Oscillations

1981

- M**.** Z. Massoud and J. D. Plumer, "*Thermal Oxidation of Silicon in Dry 02 in the* ***Thin Region*** *(<500 A)*"

Everything is Relative

- S. K. Lai , " ***Interface Trap Generation*** *in MOS Systems when Electrons are Captured by Trapped Holes*"

Electron Capture Model

- A.C. Gossard, **D. C. Tsui**, and **H. L. Stormer** "*GaAs IGFETS and Two-Dimensional Electrons on MBE Grown AlGaAs/GaAs Heterostructures*"

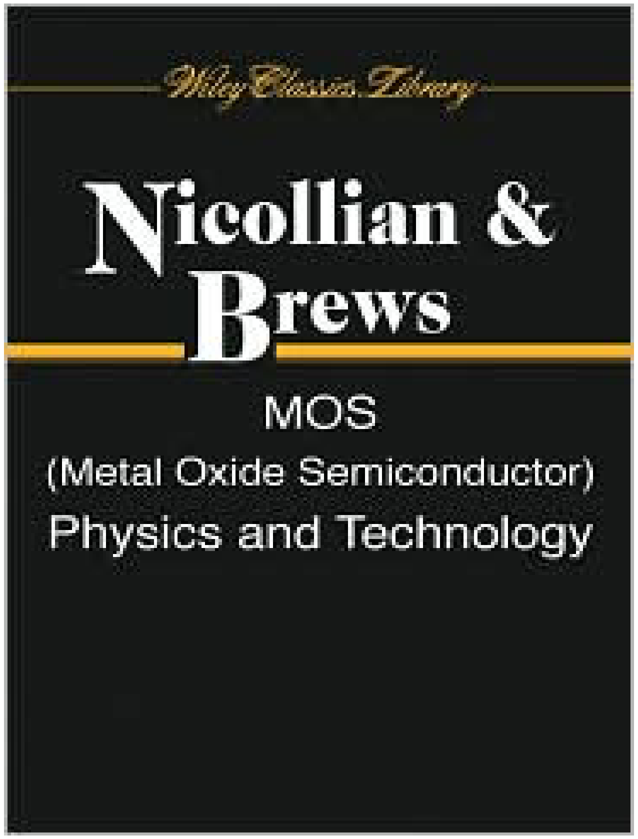
Prelude to Quantum Hall Effect

(Coauthored by Future Nobel Laureates)

1982

- E. H. **Nicollian** and J. R. **Brews**, “*Accurate MOS Capacitor Measurement of Band Bending, Interface Trap Density, Doping Profile, and Oxide Charge Density*”

Prelude to the famous book



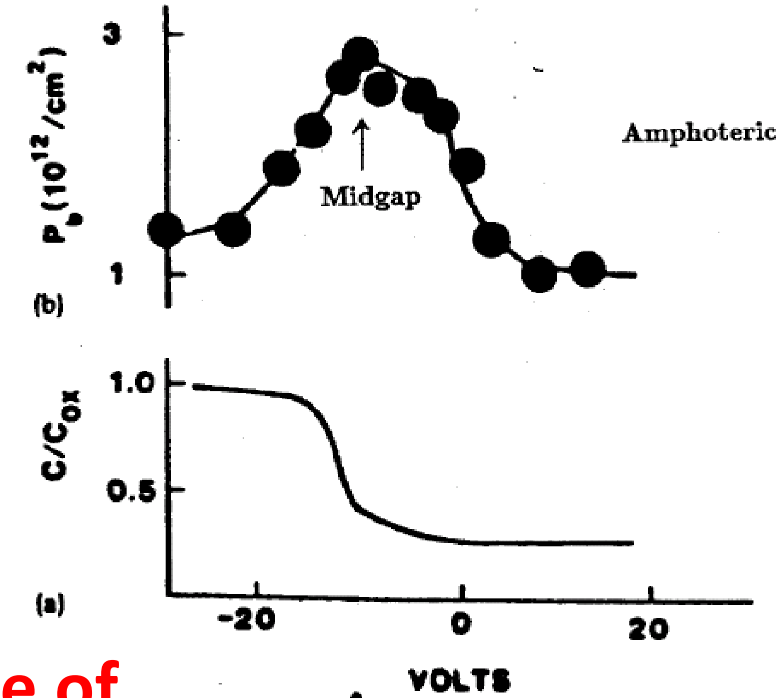
Wiley Classics Library

Nicollian & Brews

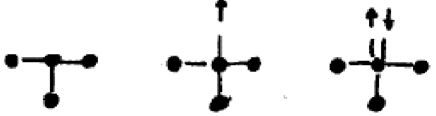
MOS
(Metal Oxide Semiconductor)
Physics and Technology

1982

- **P. *M.* Lenahan and P V. Dressendorfer,** *“An Electron Spin Resonance Study of the Efects of Radiation and High Field Stressing on MOS Devices”*



Amphoteric Nature of Interface Traps



- **B. *E.* Deal,** *“Current Trends in Thermal Oxidation in VLSI”*

1984

- Inauguration of Poster Session

- D. C. Tsui, “*The Quantum Hall Effect*”

Prelude to His Nobel Prize

1987

- Started the process of removing author names and affiliations in submitted abstract

- R. Sites, R. Koch, “*Characterization of SiOx on Si by* ***STM:****Identification of Individual Traps*”
- L. Bell, W. Kaiser, M. Hecht, and F. Grunthaner, “*Process-Dependent Morphology of the SiO2/Si Interface Characterized by* ***Scanning Tunnel Microscopy***”

1987

- Y. Nishioka, E.F. da Silva, X.W. Wang, and T.P. Ma, *“Effects of NF_3 During Si Oxidation on the Radiation Response of MOS Capacitors“*

First F Passivation Paper

1988

- X. Wang, Y. Wang, D. Wang, and T. P. Ma,

  “Radiation Hardness Aging of Fluorinated SiO2/Si Interface”

Three Kings and One Horse

1989

- **Session IV: Silicon-Germanium Technology and Devices**

  B. Meyerson, “*Silicon and Si-Ge structures and devices by UHV chemical vapor deposition*”

First Si-Ge Session

1991

- D. Wang, T. P. Ma, J. W. Golz, B. L. Halpern, and J. J. Schmitt, "*High Quality MNS Capacitors Prepared by Jet Vapor Deposition at Room Temperature*“

First Device-Quality

High-k Gate Dielectric (Si_3N_4)

1992

- **SESSION 5**

  Fundamental Properties of Oxynitrides

- **SESSION 6: Panel Discussion**

Will Any Other Dielectric Replace SiO_2 ?

(Conclusion: No!)

1992

- W. Chen and T.P. Ma, “*Can Interface-Trap Capture Cross Sections as Determined by Charge Pumping Be Used to Predict Surface RecombinationIGeneration Currents*?”
- L. Vishnubhotla and T.P. Ma, “Selective Annealing Behavior of Two Distinct Defect Centers at Irradiated <lOO>Si /Si02 Interface”
- A. Balasinski and T.P. Ma, “Reduction of Interface-trap Density in MOS Devices by Irradiation”
- M.-H. Tsai and T.P. Ma, “*l/f Noise in Hot-Carrier Damaged MOSFET's: Effects of Oxide Charge and Interface Traps*”
- B. Zhang and T.P. Ma, “*How Does Electron Trapping in Buried Oxide and Back-Interface Traps Affect the Front-Channel Characteristics of Thin-Film SOI-INMOSFET7s?*”
- X. W. Wang, Wenliang Chen, and T.P. Ma, “*Conversion of <111>Si/Si02 Interface into <l00>-Like Interface by Introducing Fluorine*”
- L. Vishnubhotla and T.P. Ma H**.** H.Tseng and P. J. Tobin, **“**Hole Trapping, Detrapping and Interface-trap Generation in Flourinated Si02 MOS”

7 Papers from T.P. Ma’s Group

1994

- **SESSION 5: Nitrogen Containing Oxides**
- **SESSION 6: Ultra-Thin Oxides/Advanced Technologies**

Xiewen Wang and T.P. Ma, "***Silicon Nitride*** *Thin Films Made by Jet Vapor Deposition"*

1995

Session 7

Dielectrics Other Than Thermal Oxide

Session 8

Nitrogen Containing Oxides

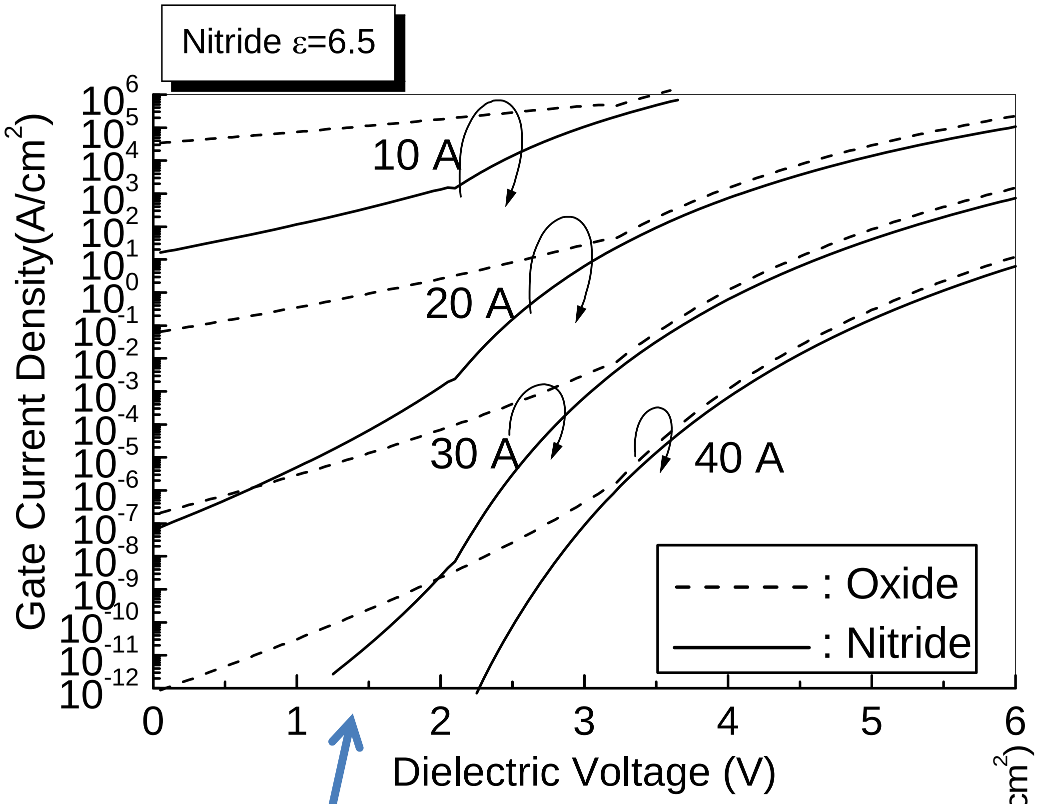
1995 Symposium on VLSI Technology
9B-2

Extending Gate Dielectric Scaling Limit by Use of Nitride or Oxynitride

X. W. Wang, Y. Shi, and T.P. Ma
Dept. of Electrical Engineering, Yale University, New Haven CT 06520
G.J.Cui, T.Tamagawa, J. W. Golz, B.L. Halpern, and J.J. Schmitt
Jet Process Corporation, New Haven, CT 06511

Abstract

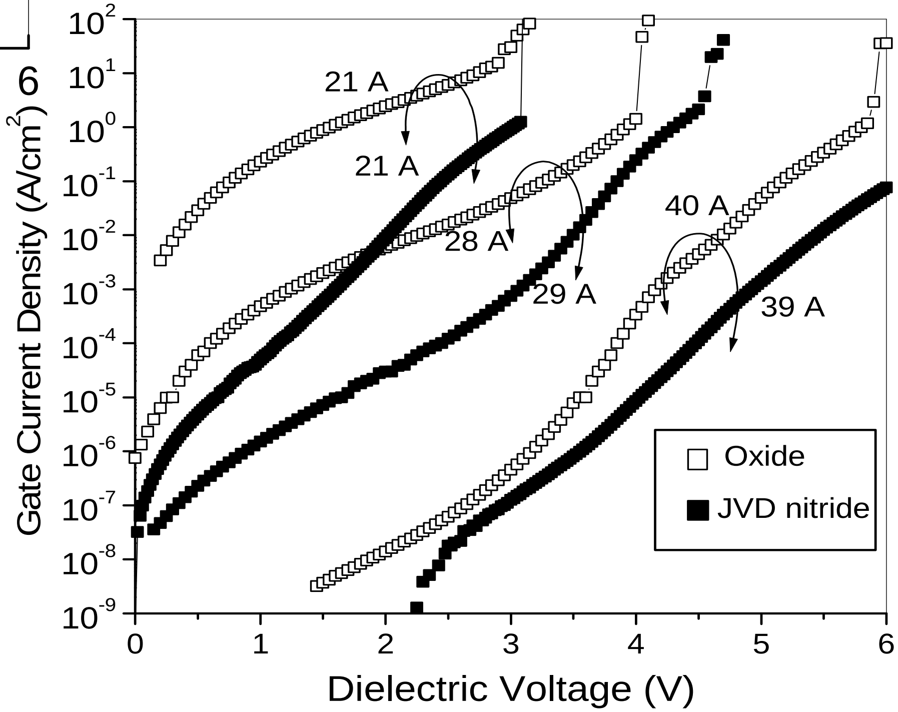
Theoretical calculations indicate that <u>the tunneling currents in silicon nitride or oxynitride are greatly reduced compared to those in $Si0_2$ for equivalent oxide thicknesses (EOT) below 4 nm.</u> Experimental results obtained on Jet Vapor Deposited (JVD) nitrides/oxynitrides are shown to verify the theoretical trend. These results suggest that extending the scaling limit well below 4nm of EOT is possible with the JVD nitride.



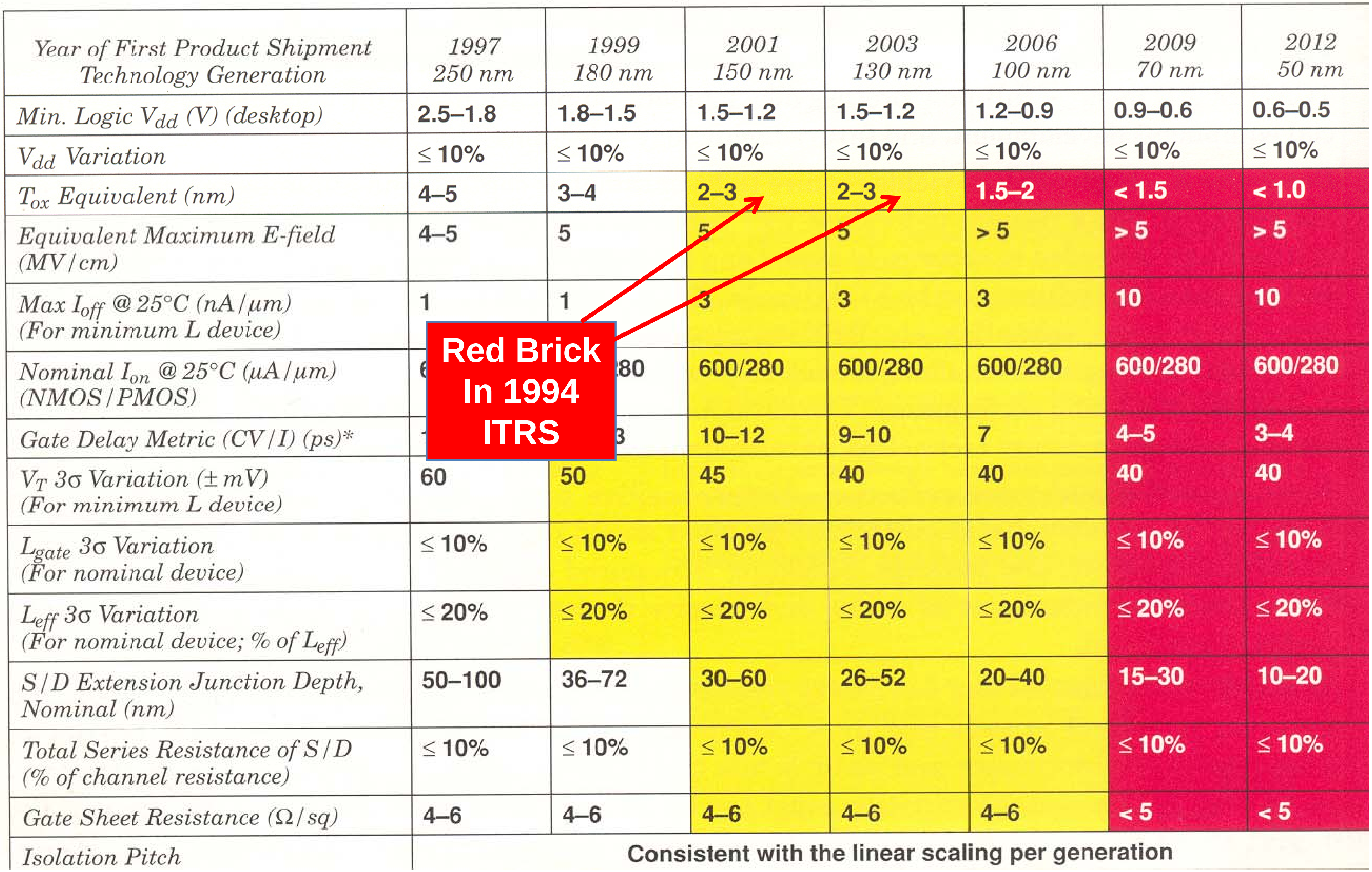
Tunneling Current is Much Reduced for Trap-free Si$_3$N$_4$ of the Same EOT

Theoretical

Measured



1996 ITRS Road Map



Red Brick In 1994 ITRS

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
Min. Logic V_{dd} (V) (desktop)	2.5–1.8	1.8–1.5	1.5–1.2	1.5–1.2	1.2–0.9	0.9–0.6	0.6–0.5
V_{dd} Variation	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%
T_{ox} Equivalent (nm)	4–5	3–4	2–3	2–3	1.5–2	< 1.5	< 1.0
Equivalent Maximum E-field (MV/cm)	4–5	5	5	5	> 5	> 5	> 5
Max I_{off} @ 25°C (nA/μm) (For minimum L device)	1	1	3	3	3	10	10
Nominal I_{on} @ 25°C (μA/μm) (NMOS/PMOS)	6	80	600/280	600/280	600/280	600/280	600/280
*Gate Delay Metric (CV/I) (ps)**	1	3	10–12	9–10	7	4–5	3–4
V_T 3σ Variation (± mV) (For minimum L device)	60	50	45	40	40	40	40
L_{gate} 3σ Variation (For nominal device)	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%
L_{eff} 3σ Variation (For nominal device; % of L_{eff})	≤ 20%	≤ 20%	≤ 20%	≤ 20%	≤ 20%	≤ 20%	≤ 20%
S/D Extension Junction Depth, Nominal (nm)	50–100	36–72	30–60	26–52	20–40	15–30	10–20
Total Series Resistance of S/D (% of channel resistance)	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%
Gate Sheet Resistance (Ω/sq)	4–6	4–6	4–6	4–6	4–6	< 5	< 5
Isolation Pitch	Consistent with the linear scaling per generation						

1995

IN MEMORY OF E. H. NICOLLIAN

The IEEE Semiconductor Interface Specialist Conference mourns the passing of Edward Haig Nicollian who died on December 17, 1994, in Charlotte, North Carolina at age 67

1996

- H.S. Momose, S-i. Nakamura, Y. Katsumata, and H. Iwai, "*Thin Gate Dielectrics for Future CMOS Applications*" (Invited)

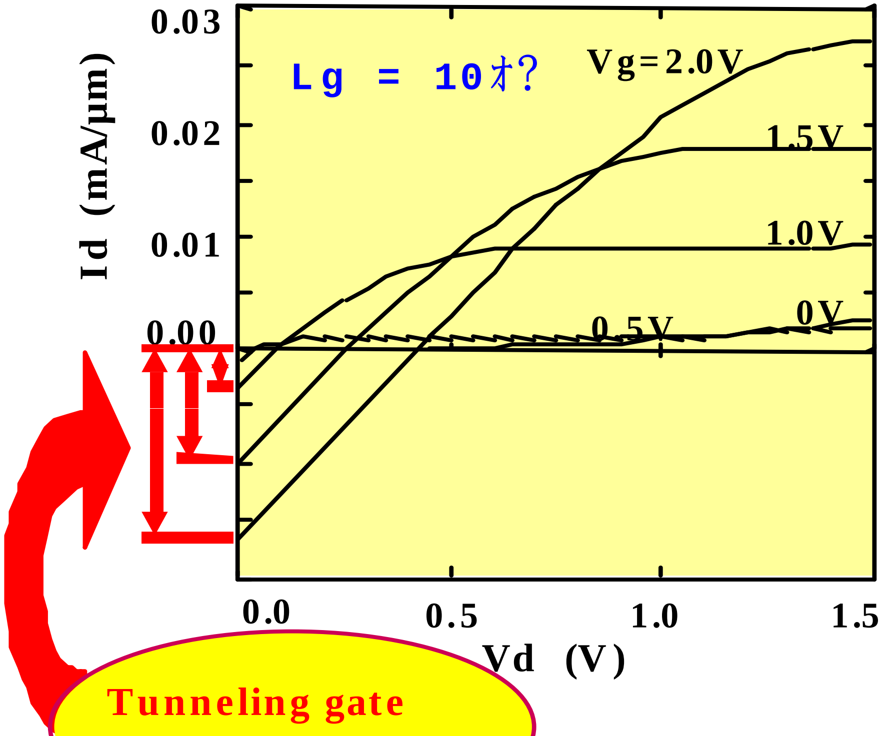
High-Performance CMOS Transistors

with **T_{ox} < 2nm**

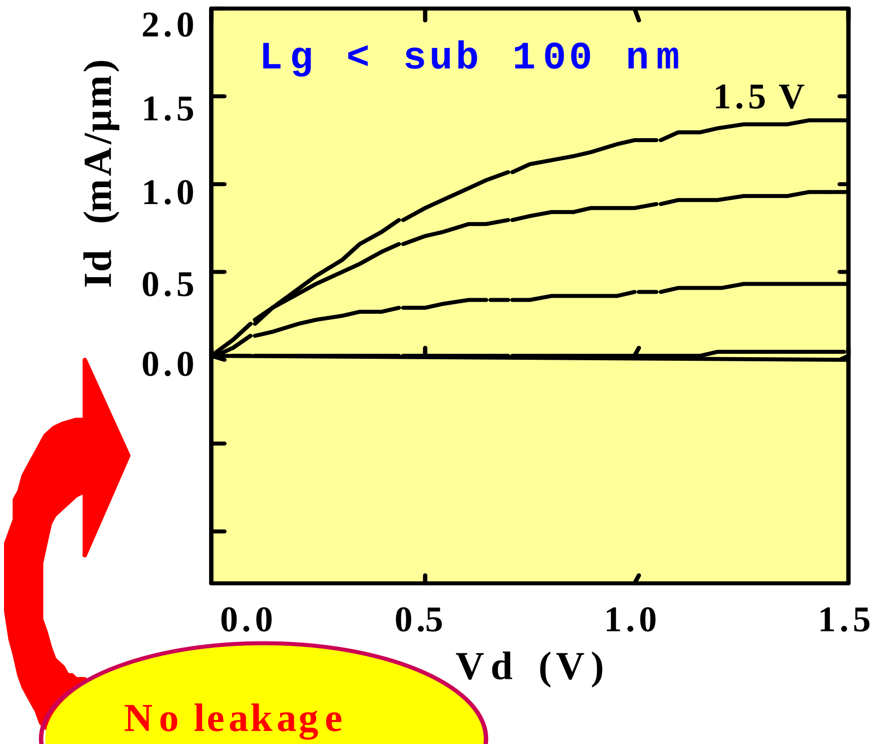
Pushing the Limit of Thermal SiO_2

Gate length dependence of Id - Vd characteristics

1.5 nm Gate Oxide



Tunneling gate leakage current



No leakage current

1997

- D. J. **DiMaria** and J. H. Stathis, "Ultimate Limit for Defect Generation in Ultra-Thin SiO_2"

"Doomsday" Prediction

for SiO_2 < 2 nm

1998

- **Session 6: Nitrides and Oxynitrides**

  Friday, Dec. 4, 1998
- **Session 8: Alternative Dielectrics**

  Saturday, Dec. 5, 1998

Rump Session on Alternative Dielectrics 2 PM - 4 PM Middleton Room

1999

- **Session 1 - Alternative Dielectrics I**

  Thursday, December 2, 1999
- **Session 2 - Alternative Dielectrics II**

  Thursday, December 2, 1999
- **Rump Session - Alternative Dielectrics**

  Friday, Dec. 3, 1999

2000

- **Session 1** - **High-K Gate Dielectrics - I**
  Thursday, December 7, 2000
- **Rump Session – High-k Dielectrics**
  Friday, Dec. 8, 1999
- **Session 10** - **High-K Gate Dielectrics - II**
  Saturday, December 9, 2000
- **Session 11** - **High K Gate Dielectrics - III**
  Saturday, December 9, 2000

2001

- **Session 1 – High-K Gate Dielectrics – I**
- **Poster Session I: High K**
- **Poster Session III: Wide Bandgap & Remaining High K**
- **Session 6 – High K with Hf**
- **Session 7 – High-K Gate Dielectrics – II**

2002

- Session 1 – High-κ Gate Dielectrics – I
- Poster Session I: High-κ Dielectrics
- Session 2 – High-κ Dielectrics – II
- Poster Session II – High-κ Dielectrics
- Session 6 – Modeling High-κ Interfaces
- Rump Session: “High-κ dielectrics: Material of the Future?”
- Session 7 – Issues for High-κ Gate Dielectrics – I
- Session 8 – Issues for High-κ Gate Dielectrics – II

8 of 12 Session are High-k Centric

2003

- **Session 6 - Non-silicon Interfaces**

  (All with III-V Substrates)
- **Poster Session II: Non-silicon Interfaces**

  (All with III-V Substrates)

Onset of Sessions on III-V and Ge Interfaces

2008

Wednesday Evening Tutorial Started

Other Recurring Session Topics

- **SiC and Other Wide-gap Semiconductors**

  (Since 1995)
- **SOI**

  (Since 1997)
- **Nonvolatile Memory Devices**

  (Since 1998)

Gate Dielectrics, Interfaces, and SISC

- A little bit of history
- Highlights of some milestone papers
- Stories of some legendary figures
- A little bit of science
- Hopefully entertaining