SISC 96

27th IEEE Semiconductor Interface Specialists Conference

December 5-7, 1996
The Catamaran Hotel, San Diego California, USA

IEEE

ABSTRACTS

General Chair : **R.E. Stahlbush**

Technical Chair : **D.A. Buchanan**

Arrangements Chair : **L. Trombetta**

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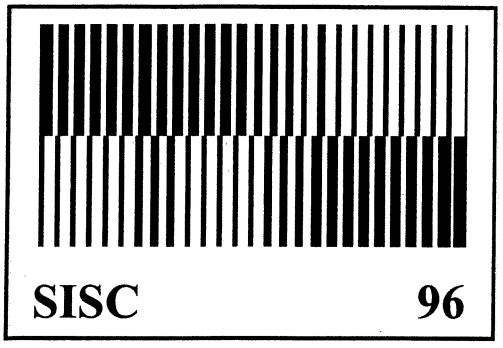

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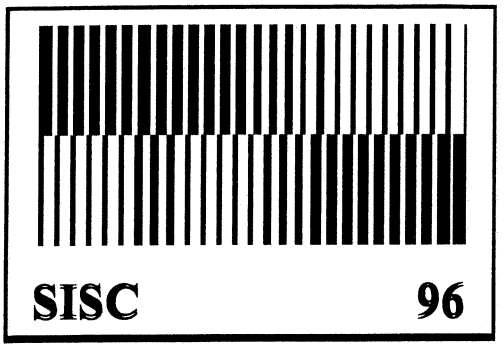
SISC Ed Nicollian Award for Best Student Paper

This year the SISC is continuing with the ***SISC Ed Nicollian Best Student Paper Award.*** This award was started in 1995 to honor the memory Prof. E. H. Nicollian who was a pioneer in the exploration of metal oxide semiconductor (MOS) systems. His contributions were fundamental to establishing the SISC in its early years and he served as the Technical Chair in 1982. With John Brews, he wrote the definitive book about interface and near-interface defects in MOS devices measured by capacitance-voltage techniques.

SISC Ed Nicollian Best Student Paper Award is presented to the best paper presented by a student at the Semiconductor Interface Specialists Conference. To be eligible, the student must be the lead author and give the oral or poster presentation. At the end of the conference, after all papers have been given, the program committee votes for the best student presentation. The award, consisting of a plaque and an honorarium, are presented to the recipient after the conference. The winner from the 1995 SISC was K. A. Ellis, for his paper ***"Gas Phase Chemistry of N_2O Furnace Oxidation"***, by K.A. Ellis and R.A. Buhrman, School of Applied and Engineering Physics, Cornell University.

Those wishing to be considered for the 1996 award should make themselves known to the Technical Chair.



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SESSION 1 - Silicon Carbide

Thursday December 5, 1996 8:00 AM -9:50 AM
Session Chair : D.M. Fleetwood

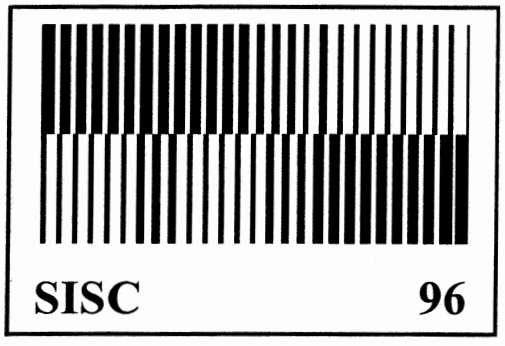
8:00 AM **Opening Remarks**

8:10 AM 1.1 **Electron Transport at the SiC/SiO_2 Interface (Invited),** T.Ouisse, Laboratoire de Physique des Composants à Semiconducteurs (LPCS), UMR-CNRS 5531, ENSERG, Grenoble, France.

8:50 AM 1.2 **Charge Pumping Measurements on 6H-SiC MOSFETs,** M.J. Kivi[1], S. Taylor[1] and L.A. Lipkin[2], [1]Department of Electrical Engineering and Electronics, Liverpool University, Liverpool, UK, [2]Cree Research Inc., Durham, NC USA.

9:10 AM 1.3 **Termination of Dangling Bond Defects at $SiC-SiO_2$ Interfaces,** A. Gölz[1], G. Lucovsky[2], K. Koh[2], D. Wolfe[2] and H. Kurz[1], [1]Institut fur Halbeitnertechnik, RWTH-Aachen, Germany, [2]Department of Materials Science and Engineering, Physics, Electrical and Computer Engineering, North Carolina State University, Raleigh, NC USA.

9:30 AM 1.4 **6H-SiC/SiO_2 Interface Degradation Caused by Electron Injection in the Oxide,** V.V. Afanas'ev[1], M. Bassler[2], G. Pensl[2] and M.J. Schultz[2], [1]Department of Physics, University of Leuven, Belgium, [2]Institute of Applied Physics, Univeristy of Erlangen-Nurnberg, Erlangen, Germany.



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POSTERS P1.1-P1.6

Thursday December 5, 1996 9:50 AM -10:11 AM
Session Chairs : S. Taylor and M. Passlack

9:50 AM P1.1 **Comparing SiO_2 Grown on Aluminum or Boron Doped p-type SiC,** L.A. Lipkin[1] J.W. Palmour[1] and J.S. Suehle[2], [1]Cree Research Inc, Durham, NC USA, [2]NIST, Gaithersburg, MD USA.

9:53 AM P1.2 **Reliability Properties of Ultra-thin Oxide Layers Subjected to Fowler-Nordheim Tunnelling Current Stress,** A. Scarpa[1,2,3], G. Ghibaudo[1], G. Ghidini[2], G. Pananakakis[1], and A. Paccagnella[3], [1]Laboratoire de Physique des Composants à Semiconducteurs, ENSERG, Grenoble, France, [2]SGS-Thomson Microelectronics, Central R&D, Agrate Brianza Italy, [3]Dipartimento di Elettronica e Informatica, Università di Padova, Padova, Italy.

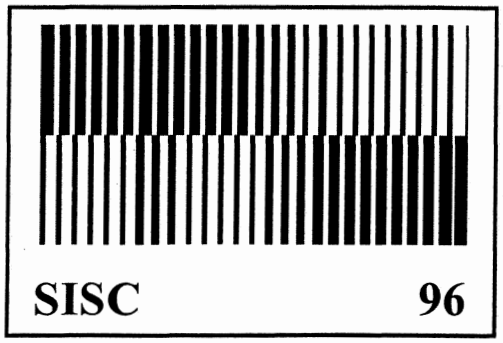
9:56 AM P1.3 **Superior Characteristics of Low Temperature-Grown Ultrathin (3 nm) Oxides with Post Oxidation Annealing,** M. Matsumura, T. Sakoda, T. Komeda and Y. Nishioka, Texas Instruments Tsukuba R&D Center Ltd., Tsukuba, Ibaraki, Japan.

9:59 AM P1.4 **Lateral Distributions of Erase-Induced Hole Trapping and Interface Traps in Flash EPROM/NMOSFET Devices,** C. Chen and T.P. Ma, Center for Microelectronic Materials Structures, Dept. of Electrical Engineering, Yale University, New Haven CT USA.

10:02 AM P1.5 **Leakage Currents in Ultra-thin Silicon Nitride/Oxide Dielectric Stack,** Y. Shi[1], X.W. Wang[1], T.P. Ma[1], G.J. Cui[2], T. Tamagawa[2], B.L. Halpern[2] and J.J. Schmitt[2], [1]Dept. of Electrical Engineering, Yale University, New Haven CT USA, [2]Jet Process Corporation, New Haven CT USA.

10:05 AM P1.6 **Endurance Characteristics of Rapid Thermal Chemical Vapor Deposited Tunnel Dielectrics Annealed in N_2O for EEPROM Applications,** B.E. Hornung, H.H. Heinisch, S.A. Craig and J.J. Wortman, North Carolina State University, Raleigh, NC USA.

10:08 AM **BREAK**



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SESSION 2 - Monte Carlo / Theory

Thursday December 5, 1996 10:45 AM -12:45 AM
Session Chair : M. Morita and A. Toriumi

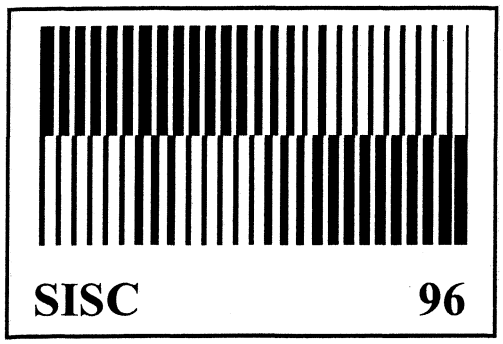
10:45 AM 2.1 **Monte Carlo Simulation of MOS Devices (Invited), M.V. Fischetti** and S.E. Laux, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY USA.

11:25 AM 2.2 **Monte Carlo Simulation of Electron Transport Properties of Quantized Silicon Carbide Inversion Layers,** J.B. Roldán F. Gámiz, J.A. López-Villanueva, and P. Cartujo, Departmento de Electrónica y Technogía de Computadores, Universidad de Granada, Granada, Spain.

11:45 AM 2.3 **Quantum Mechanical Calculation of Capacitance and Tunneling Current of Ultra-thin Gate Oxides with Experimental Verification,** S-H. Lo, D.A. Buchanan, Y. Taur and W-K. Wang, IBM Thomas J. Watson Research Center, Yorktown Heights, NY USA.

12:05 PM 2.4 **Theory of Si- and C- P_b Centers on the (111) Interfaces of β-SiC-SiO_2 System**, A.H. Edwards[1], W.B. Fowler[2], Department of Electrical Engineering, University of North Carolina at Charlotte, Charlotte, NC USA, [2]Department of Physics and the Sherman Fairchild Laboratory, Lehigh University, Bethehem, PA USA.

12:25 PM **LUNCH**



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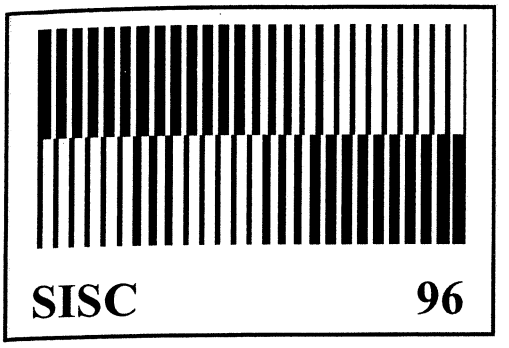
SESSION 3 - Oxide Degradation and Defects

Thursday December 5, 1996 2:00 PM - 4:00 PM
Session Chair : K.R. Farmer

2:00 PM	3.1	**New Insights in the Impact of the Breakdown Mechanisms on the Statistics of Intrinsic and Extrinsic Breakdown in Thin Oxides (Invited), G. Groeseneken**, R. Degraeve, J.-L. Ogier, R. Bellens, Ph. Roussel, M. Depas and H.E. Maes, IMEC, Leuven, Belgium.
2:40 PM	3.2	**Dependence of MOS Oxide Charging and Hole Currents on Poly-Si-Gate-Work-Function,** D.J. DiMaria, IBM-Research Division, T.J. Watson Research Center, Yorktown Heights, NY USA.
3:00 PM	3.3	**Apparent Annihilation of Interface Traps by Hot-Carrier Injection,** Y. Li and T.P. Ma, Dept. of Electrical Engineering, Yale University, New Haven CT USA.
3:20 PM	3.4	**Enhanced Low-Rate Radiation-Induced Charge Trapping at the Emitter-Base/Oxide Interface of Bipolar Devices,** D.M. Fleetwood[1] and R.D. Schrimpf[2], [1]Sandia National Laboratories, Albuquerque, NM USA, [2]Dept. of Electrical and Computer Engineering, Tucson, AZ USA.
3:40 PM	3.5	**Electron and Hole Trap Formation in Buried Thermal Oxide Caused by 1100 to 1325°C Annealing**, R. E. Stahlbush, Naval Research Laboratory, Washington, DC USA.
4:00 PM		**BREAK**



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POSTERS P3.1-P3.5

Thursday December 5, 1996 4:30 PM - 4:45 PM
Session Chairs : W.B. Fowler and D.B. Brown

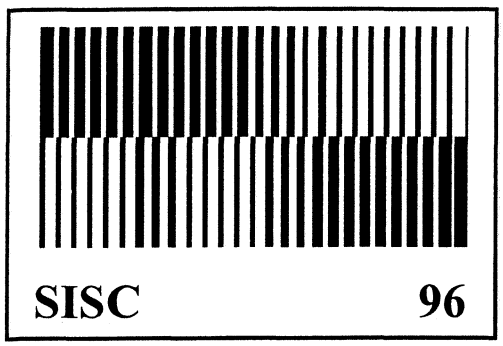
4:30 PM P3.1 **Initial Stages of Si-SiO_2 Interface Formation by Rapid Thermal Oxidation in O_2 and N_2O by On-Line Auger Electron Spectroscopy (AES),** K. Koh, H. Yang, H. Niimi and G. Lucovsky, Department of Materials Science and Engineering, Physcis, Electrical and Computer Engineering, North Carolina State University, Raleigh, NC USA.

4:33 PM P3.2 **Determination of Ultra-Thin Oxide Voltages and Thickness for Dual-Gate Poly FET Structures,** E. Wu[1], S-H. Lo[2], A. Acovic[1], and D.A. Buchanan[2], [1]IBM Microelectronics Division, Essex Junction, VT USA, [2]IBM T. J. Watson Research Center, Yorktown Heights, NY USA.

4:36 PM P3.3 **Degradation and Nitridation Dependence of Steady-State Stress Induced Leakage Current (SILC),** J. De Blauwe, R. Degraeve, R. Bellens, J. Van Houdt, G. Groeseneken, H. E. Maes, IMEC, Leuven, Belgium.

4:39 PM P3.4 **Cathode and Anode Traps in High-Voltage Stressed Silicon Oxides,** L. Chen[1], C-S. Kang[2], D.J. Dumin[1], G.A. Brown[3], P. Bellutti[4], [1]Center for Semiconductor Device Reliability Research, Department of Electrical and Computer Engineering, Clemson University, Clemson, SC USA, [2]Semiconductor Process Laboratory, Texas Instruments, Inc., Dallas, TX USA, [3]Istituto per la Ricerca Scientifica e Tecnologica, Trento, Italy, [4]Department of Electronic Engineering Yuhan College, Kyungki-Do, Korea.

4:42 PM P3.4 **Quasi-Breakdown in Ultra-Thin Gate Dielectrics,** A. Halimaoui[1], O. Brière[1,2], Y. Chroboczek[1], and G. Ghibaudo[3], [1]France Télécom, CNET, Meylan, France, [2]Matra MHS TEMIC, La Chantrerie, Nantes, France, [3]LPCS, Grenoble, France.



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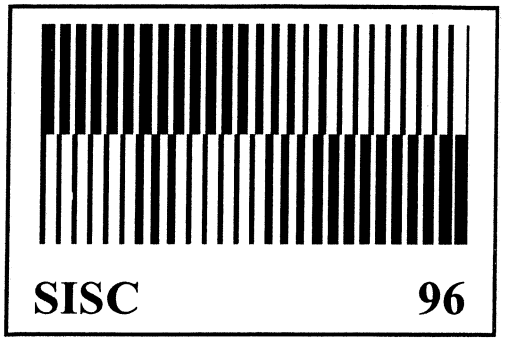
SESSION 4 - TFT's and Hetrostructures

Thursday December 5, 1996 4:45-5:45 PM
Session Chair : T.P. Ma

4:45 PM 4.1 **New Experimental Technique for Evaluating Band Discontinuity - Application of Admittance Spectroscopy to MOS Capacitors Fabricated on $Si/Si_{1-x}Ge_x/Si$ Heterostructures,** S-i Takagi[1], J.L. Hoyt[2], K. Rim[2], J.J. Wesler[2] and J.F. Gibbons[2], [1] ULSI Research Lab, Toshiba Corp., [2]Solid State Electronics Lab, Stanford University, Stanford CA USA.

5:05 PM 4.2 **Effect of Interface Roughness on the Performance of Poly-Si TFT Fabricated by Novel Oxidation Method,** J-H. Jeon, C-M. Park, B-H, Min and M-K. Han, School of Engineering, Seoul National University, Seoul, Korea.

5:25 PM 4.3 **The Characteristics of Oxide on Poly-Si Structure Fabricated by Excimer Laser Irradiation,** C-M. Park, B-H, Min, J-H., Jun, J-S. Yoo, and M-K. Han, School of Engineering, Seoul National University, Seoul, Korea.



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POSTERS P4.1-P4.5

Thursday December 5, 1996 5:45 PM - 6:00 PM
Session Chair : S. Cristoloveanu and D.A. Buchanan

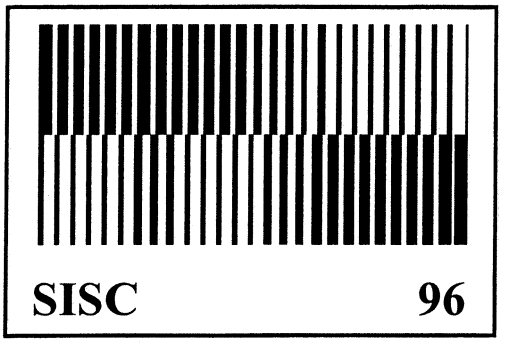
5:45 PM P4.1 **Interaction of H/H^+ with *a*-SiO_2: An *ab initio* Quantum Chemical Study**, S.P. Karna[1], A.M. Ferreira[1], R.D. Pugh[1], C.P. Brothers[1], B.K. Singaraju[1], W.L. Warren[2] and K. Vanheusden[2], [1]US Air Force Phillips Laboratory, Space Electronics Division, Kirtland Air Force Base, NM USA, [2]Sandia National Laboratories, Albuquerque, NM USA.

5:48 PM P4.2 **Trapping Centers in Unibond® Buried Oxides**, B.D. Wallace[1], P.M. Lenahan[1], and J.F. Conley, Jr.[2], [1]The Pennsylvania State University, Department of Engineering Science and Mechanics, University Park, PA, [2]Dynamics Research Corporation, Commercial Systems, Beaverton, OR USA.

5:51 PM P4.3 **Profiling of Both Oxide Charge and Interface States in MOSFET under Various Bias Stress Conditions**, S-M. Cheng, C-M. Yih, C-C. Yeh, S-N. Kuo, and S.S. Chung, Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, Republic of China.

5:54 PM P4.4 **Correlating LDD nMOSFET Hot Carrier Degradtion with a Microstructural Model for Interface Traps**, R. J. Milanowski[1], M. P. Pagey[1], and E. S. Snyder[2], [1]Dept. of Electrical and Computer Engineering, Vanderbilt University, Nashville, TN USA, [2]Sandia Technologies, Albuquerque, NM USA.

5:57 PM P4.5 **Numerical Simulation of Hydrogen Redistribution in Thin SiO_2 Films Under Electron Injection in High Fields,** G. Gadiyak, Institute of Computational Technologies, Russian Academy of Sciences Siberian Division, Novosibirsk, Russia.



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SESSION 5 - Oxide and Interface Characterization

Friday December 6, 1996 8:30 AM - 10:30 AM
Session Chair : A. Ishitani

8:30 AM 5.1 **Application of Femtosecond Lasers to Nonlinear Spectroscopy and Process Monitoring of Si(001) Interfaces (Invited), M.C. Downer**, J.I. Dadap, X.F. Xu, P.T. Wilson, M.H. Anderson, M. ter Beck, O.A. Akisipetrov, E.D. Mishina, N.M. Russell and J.G. Ekerdt, Center for Synthesis, Gowth and Analysis of Electronic Materials, University of Texas at Austin, Austin, TX USA.

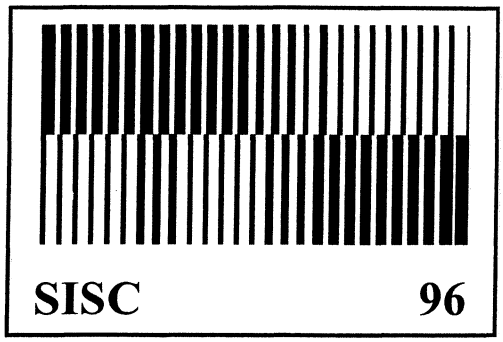
9:10 AM 5.2 **A Slow Trap Profiling Technique for MOS Structure Characterizaton,** Dimitrijev, P. Tanner and H.B. Harrison, School of Microelectronic Engineering, Griffith University, Nathan, Queensland, Australia.

9:30 AM 5.3 **Electronic Structure of P_b Centers at the (100), (111) and (110) Si/SiO_2 Interfaces,** J. H. Stathis and E. Cartier, IBM Research Division, Yorktown Heights, NY USA.

9:50 AM 5.4 **Quantum Electrical Measurements of SiO_2/Si Roughness in MOS Transistors,** C.A. Richter[1] and W.R. Anderson[2], [1]Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD USA, [2]Digital Semiconductor, Digital Equipment Corporation, Hudson, MA USA.

10:10 AM 5.5 **Light Emission during Direct and Fowler-Nordheim Tunneling in Ultra Thin MOS Tunnel Junctions**, E. Cartier, J.C. Tsang, M.V. Fischetti, and D.A. Buchanan, IBM Research Division, T. J. Watson Research Center, Yorktown Heights, NY USA.

10:30 AM **BREAK**



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SESSION 6 - N_2O growth and characterization

Friday December 6, 1996 11:00 AM-12:40 PM
Session Chair : R.E. Stahlbush

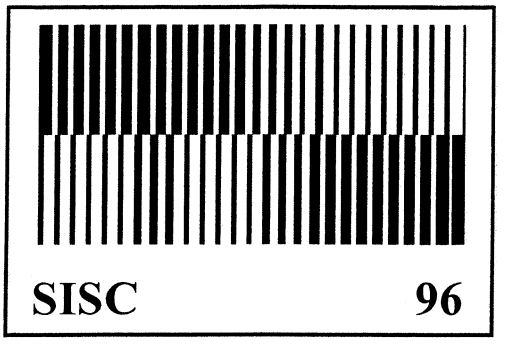
11:00 AM 6.1 **Nitrogen Behaviour during the Thermal Growth of Silicon Oxynitride Films on Si in N_2O,** I.-J. Ganem[1], I. Trimaille[1], S. Rigo[1], I.J.R. Baumvol[2] and F.C. Stedile[2], [1]Groupe de Phys. des Solides, Universités Paris 6 et 7, Paris, France, [2]Instituto de Fisica and Quimica, UFRGS, Porto Alegre, Brazil.

11:20 AM 6.2 **High Resolution Depth Profiling of Ultrathin Silicon Oxynitrides**, H.C. Lu[1], E.P. Gusev[1], T. Gustafsson[1], E. Garfunkel[1], D. Brasen[2], and M.L. Green[2], [1]Departments of Physics and Chemistry, and Laboratory for Surface Modification, Rutgers Unversity, Piscataway, NJ USA, [2]Bell Laboratories Lucent Technologies, Murray Hill, NJ USA.

11:40 AM 6.3 **Growth and Reliability of 3 nm N_2O Gate Oxide,** T Nigam, .M. Depas and M.M. Heyns, IMEC, Leuven, Belgium.

12:00 PM 6.4 **Effect of Nitrogen Implantation on Gate Oxide Reliability**, Chuan Lin[1], A.I. Chou[1], B. Doyle[2], H.R. Soleimani[3], and J.C. Lee[1], [1]Microelectronics Research Center, University of Texas, Austin, TX USA, [2]Intel Corporation, Santa Clara, CA USA, [3]Digital Equipment Corporation, ULSI Operations Group, Hudson, MA USA.

12:20 AM 6.5 **Boron Diffusion in Gate Oxynitrides**, K.A. Ellis and R.A. Buhrman, School of Applied and Engineering Physics, Cornell University, Ithaca, NY USA.



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SESSION 7 - Deuterium and Hydrogen

Saturday December 7, 1996 8:30 AM - 10:10 AM
Session Chair : K.S. Krisch

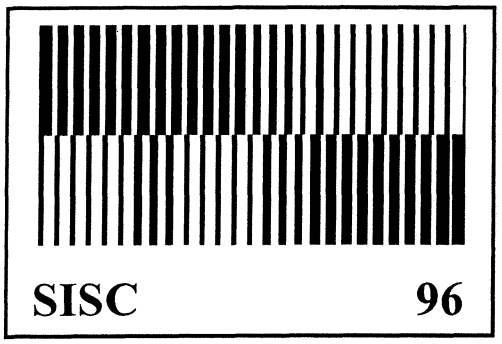
8:30 AM 7.1 **STM Nanofabrication and Deuterium Post Metal Annealing of MOSFETs for Improved Hot Carrier Reliability (Invited), J.W. Lyding[1],** K. Hess[1] and I.C. Kizilyalli[2], [1]Dept. of Electrical and Computer Engineering and Beckman Institute, University of Illinois at Urbana-Champaign, Urbana, IL USA, [2]Bell Laboratories, Lucent Technologies, Orlando, FL USA.

9:10 AM 7.2 **On the Behavior of Deuterium in Ultrathin SiO_2 Films upon Thermal Annealing,** I.J.R. Baumvol[1], F.C. Stedile[2], F.L. Freire Jr.[3], E.P. Gusev[4], M.L. Green[5], and D. Brasen[5], [1]Instituto de Fisica, [2]Instituto de Quimica-UFRGS, Porto Alegre, Brazil, [3]Departamento de Física, PUC-Rio, Brasil, [4]Depts, of Chemistry and Physics, Rutgers University, Piscataway, NJ, USA, [5]Bell Laboratories Lucent Technologies, Murray Hill, NJ, USA.

9:30 AM 7.3 **Temperature Dependent Electron Capture by Protons (H^+) in SiO_2 Thin Films,** K. Vanheusden,[1] W.L. Warren[1], D.M. Fleetwood[1], and R.A.B. Devine[2], [1]Sandia National Laboratories, Albuquerque, New Mexico, USA, [2]France Telecom/CNET, Meylan Cedex, France.

9:50 AM 7.4 **Creation of P_b Interface Defects in Thermal Si/SiO_2 through Annealing: Interface Degradation Mechanism,** A. Stesmans and V.V. Afanas'ev, Department of Physics, University of Leuven, Leuven, Belgium.

10:10 AM **BREAK**



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SESSION 8 - Thin Oxide

Saturday December 7, 1996
Saturday December 7, 1996 10:40 AM - 12:30 AM
Session Chair : H. Maes

10:40 AM 8.1 **Thin Gate Dielectrics for Future CMOS Applications (Invited), H.S. Momose**, S-i. Nakamura, Y. Katsumata and H. Iwai, Toshiba Corporation, Kawasaki, Japan.

11:20 AM 8.2 **Relationship Between Positive Charge and Breakdown in Sub-3.5 nm Oxides on Silicon,** K.R. Farmer[1], C.P. Debauche[1,2], W.R. Buchwald[2] and D.A. Buchanan[3], [1]Dept. of Physics, New Jersey Institute of Technology, Newark, NJ USA, [2]U.S. Army Research Laboratory, Ft. Monmouth, NJ USA, IBM-Research Division, T.J. Watson Research Center, Yorktown Heights, NY USA.

11:40 PM 8.3 **Fluctuations of Tunneling Current in the Direct Tunneling Regime,** G.B. Alers, K.S.Krisch, D. Monroe and B.E. Weir, Bell Laboratories, Lucent Technologies, Murray Hill, NJ USA.

12:00 PM 8.4 **Stacked RTCVD Oxide and Oxynitride Films for Ultrathin Gate Dielectrics**, E.M. Vogel[1], W.K. Henson[1], P.K. McLarty[2], J.J. Wortman[1], J.R. Hauser[1], [1]Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC USA, [2]Texas Instruments Inc., Dallas, TX USA.

12:20 **CLOSING REMARKS**