

**SISC 2014**

**45<sup>th</sup> IEEE  
Semiconductor Interface  
Specialists Conference**

December 10-13, 2014  
Bahia Resort Hotel, San Diego, CA  
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## **CONFERENCE PROGRAM**

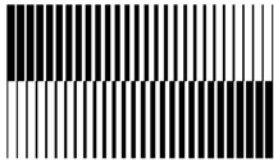
General Chair: Alex Demkov

Program Chair: Peide Ye

Arrangements Chair: Valeri Afanas'ev

Ex-Officio: Chadwin Young

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<u>General Chair</u>	<u>Program Chair</u>	<u>Arrangements Chair</u>	<u>Ex-Officio</u>
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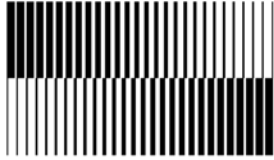
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**This meeting is sponsored by the IEEE Electron Devices Society.**



**The Conference organizers are thankful for the gracious support  
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## **SISC Ed Nicollian Award for Best Student Paper**

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, “MOS Physics and Technology,” published by Wiley Interscience.

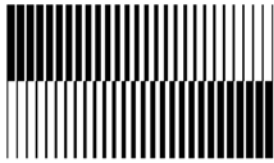
The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author for either an oral or a poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

### **Winner of the 2013 SISC Ed Nicollian Award for Best Student Paper:**

**Heng Wu, *Purdue University***

“Ultra-scaled Junctionless MOSFETs on GeOI Substrates”

with X. F. Li, L. Dong, J. J. Gu, N. J. Conrad, J. Y. Zhang, and P. D. Ye



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**Wednesday Evening Tutorial**

**Wednesday, December 10, 2014, 8:00 PM**

First introduced at SISC 2008, the Wednesday evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

**Perrine Batude**

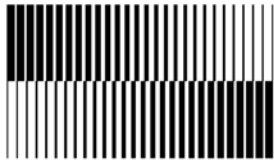
CEA-LETI, France

**3D monolithic integration: an alternative path towards CMOS scalability**

Compared with TSV-based 3D ICs, monolithic or sequential 3D ICs presents higher benefits of going to the vertical dimension. Indeed, it offers the possibility to stack devices with a lithographic alignment precision (few nm) enabling via density  $> 100$  million/mm<sup>2</sup> between transistors tiers. This integration offers promising gains in area and performance as compared to planar technology without scaling the transistor technology node. Several partitioning options are possible: Partitioning at high granularity (stacking complex functions above each other) leading to important interconnections delay reduction and partitioning at the lowest granularity level (Stacking NFET over PFET) leading to gain in process complexity. Best example for process simplification is the stacking of a III-V NFET above a Ge pFET which induce high process complexity in a planar integration.

The technological challenges of this concept will be reviewed as well as the most promising options to obtain a high performance low temperature top transistor while keeping bottom MOSFET integrity. This tutorial will detail especially:

- Bottom MOSFET performance stability as a function of the technology type (implanted and insitu doped raised source-Drain) in order to define the maximum thermal budget of top FET.
- Methodologies to create top semiconductor film on top of a processed transistor with very thin interlayer dielectric thicknesses (20-100nm)
- Key technologies to achieve high performance low temperature transistors including especially Solid Phase Epitaxy and/or laser for junction's activation, low temperature epitaxy for raised source drain formation.
- Performance, Power and Area analysis of 3D monolithic integration will be presented in order to quantify its potential gain versus planar integration.



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## Conference Agenda Overview

### Wednesday, December 10, 2014

Registration.....	6:00 PM – 8:00 PM
Evening Tutorial.....	8:00 PM – 9:30 PM
Hospitality Room.....	9:30 PM – Midnight

### Thursday, December 11, 2014

Registration.....	8:00 AM – 5:00 PM
Session 1 – Ge MOSFETs.....	8:00 AM – 9:50 AM
Session 2 – Poster Preview Session I – Ge / III-V.....	9:50 AM – 10:16 AM
Session 3 – III-V.....	10:40 AM – 12:00 PM
Session 4 – High-k Dielectrics I.....	1:30 PM – 3:35 PM
Session 5 – Poster Preview Session II High-k Dielectrics.....	4:00 PM – 4:50 PM
Session 6 – Wide Bandgap Semiconductors.....	4:50 PM – 5:45 PM
Poster Session I.....	7:00 PM – 10:00 PM
Hospitality Room.....	10:00 PM – Midnight

### Friday, December 12, 2014

Registration.....	8:00 AM – Noon
Session 7 – Two-Dimensional Materials I.....	8:00 AM – 9:55 AM
Session 8 – Two-Dimensional Materials II.....	10:20 AM – 12:15 PM
Technical Committee / Invited Speaker Luncheon.....	12:15 PM – 2:00 PM
Session 9 – Poster Preview Session III 2D/Reliability.....	2:00 PM – 2:30 PM
Session 10 – Heterogeneous Integration.....	2:30 PM – 3:30 PM
Session 11 – Poster Preview Session IV Heterogeneous Integration/Memory..	4:00 PM – 4:50 PM
Poster Session II.....	4:50 PM – 6:50 PM
Conference Banquet and Limerick Contest.....	7:00 PM – 10:00 PM
Hospitality Room.....	10:00 PM – Midnight

### Saturday, December 13, 2014

Session 13 – Memory.....	8:00 AM – 10:00 AM
Session 14 – Reliability.....	10:20 AM – 12:40 PM



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## Conference Program

### Wednesday, December 10, 2014

#### Tutorial

Session Chair: P. D. Ye

8:00 PM *Tutorial - 3D monolithic integration: an alternative path towards CMOS scalability*, P. Batude, *CEA-LETI, France*

9:30 PM – Midnight Hospitality Room

### Thursday, December 11, 2014

8:00 AM Welcome and opening remarks

#### Session 1 – Ge MOSFETs

Session Chair: C. Young

8:10 AM Opening remarks

8:15 AM 1.1 *Invited - From global and local Ge integration approaches on Si(001): Novel insights by advanced synchrotron XRD techniques*, T. Schroeder<sup>1,2</sup>, M. Zoellner<sup>1</sup>, G. Capellini<sup>1</sup>, O. Skibitzki<sup>1</sup>, F. Montalenti<sup>3</sup>, A. Marzegalli<sup>3</sup>, M. I. Richard<sup>4</sup>, T. Schuelli<sup>4</sup>, Y. Yamamoto<sup>1</sup>, P. Storck<sup>5</sup>, and B. Tillack<sup>1,6</sup>, <sup>1</sup>*IHP, Germany*, <sup>2</sup>*TU Brandenburg, Germany*, <sup>3</sup>*U. di Milano, Italy*, <sup>4</sup>*European Synchrotron Radiation Facility, France*, <sup>5</sup>*Siltronic, Germany*, <sup>6</sup>*TU Munich, Germany*

8:50 AM 1.2 - **Ge nFETs: A Study on Interface and Contact Resistance**, H. Wu, M. Si, J. Zhang, H. Zhou, and P. D. Ye, *Purdue U.*

9:10 AM 1.3 - **Very Low EOT and High Mobility in Ge MOSFETs with Very High Oxidation State Interfacial Layer by In-situ Plasma and Desorption Processes**, Y.-L. Li, K.-S. Chang-Liao, C.-C. Li, L.-J. Liu, T.-C. Chen, and T.-M. Lee, *National Tsing Hua U., Taiwan*

9:30 AM 1.4 - **Engineering of NiGe/Ge Junction by P Ion Implantation after Germanidation for Metal S/D Ge CMOS Technology**, H. Oka, Y. Minoura, R. Asahara, T. Hosoi, T. Shimura, and H. Watanabe, *Osaka U., Japan*



## Session 2 – Poster Preview Session I – Ge / III-V

Session Chair: R. Wallace

- 9:50 AM Opening remarks
- 9:52 AM 2.1 - **Fabrication of GeSn-on-insulator Structure by Utilizing Lateral Liquid-Phase Epitaxy**, T. Hosoi, K. Kajimura, K. Tominaga, T. Shimura, and H. Watanabe, *Osaka U., Japan*
- 9:54 AM 2.2 - **Demonstration of III-V fins with vertical sidewalls using Cl<sub>2</sub>/CH<sub>4</sub>/H<sub>2</sub>/O<sub>2</sub> dry etch chemistry in conjunction with digital etching for recovery of etch damage**, U. Peralagu<sup>1</sup>, X. Li<sup>1</sup>, O. Ignatova<sup>1</sup>, M. Steer<sup>1</sup>, I. Povey<sup>2</sup>, P. Hurley<sup>2</sup>, and I. Thayne<sup>1</sup>, <sup>1</sup>*U. Glasgow, UK*, <sup>2</sup>*Tyndall National Institute, Ireland*
- 9:56 AM 2.3 - **Functionalization of SiGe via H<sub>2</sub>O<sub>2</sub>(g) Dosing**, S. W. Park, T. Kaufman-Osborn, E. Chagarov, and A. C. Kummel, *UC San Diego*
- 9:58 AM 2.4 - **Band alignment characteristics of ALD Dielectrics on Ga- and N-face GaN**, J. Yang, B. S. Eller, and R. J. Nemanich, *ASU*
- 10:00 AM 2.5 - **Low-D<sub>it</sub> HfO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As Gate Stack Achieved With Plasma-Enhanced Atomic Layer Deposition**, V. Djara, N. Dordevic, L. Czornomaz, M. Sousa, C. Marchiori, E. Uccelli, D. Caimi, C. Rossel, and J. Fompeyrine, *IBM, Switzerland*
- 10:02 AM 2.6 - **Native oxide removal techniques and their effects on HfO<sub>2</sub> nucleation on InGaAs (001) and (110)**, T. J. Kent<sup>1</sup>, K. Tang<sup>2</sup>, V. Chobpattana<sup>3</sup>, M. A. Negara<sup>2</sup>, R. Droopad<sup>4</sup>, P. C. McIntyre<sup>2</sup>, and A. C. Kummel<sup>1</sup>, <sup>1</sup>*UC San Diego*, <sup>2</sup>*Stanford U.*, <sup>3</sup>*UC Santa Barbara*, <sup>4</sup>*Texas State U.*
- 10:04 AM 2.7 - **Border trap reduction and analysis for ALD high-k InGaAs gate stacks**, K. Tang<sup>1</sup>, A. Negara<sup>1</sup>, T. J. Kent<sup>2</sup>, R. Droopad<sup>3</sup>, A. C. Kummel<sup>2</sup>, and P. C. McIntyre<sup>1</sup>, <sup>1</sup>*Stanford U.*, <sup>2</sup>*UC San Diego*, <sup>3</sup>*Texas State U.*
- 10:06 AM 2.8 - **Gate Stack Formation on Highly Tensile Strained Ge and GeSn Alloys**, S. Wirths<sup>1</sup>, M.A. Pampillón<sup>1,2</sup>, D. Stange<sup>1</sup>, A. T. Tiedemann<sup>1</sup>, G. Mussler<sup>1</sup>, A. Fox<sup>1</sup>, E. San Andrés<sup>2</sup>, U. Breuer<sup>1</sup>, S. Mantl<sup>1</sup>, and D. Buca<sup>1</sup>, <sup>1</sup>*Forschungszentrum Juelich, Germany*, <sup>2</sup>*U. Complutense de Madrid, Spain*
- 10:08 AM 2.9 - **Si cap passivation on InGaAs: a route to reduce oxide traps.**, S. Sioncke<sup>1</sup>, L. Nyns<sup>1</sup>, A. Vais<sup>1</sup>, D. Lin<sup>1</sup>, J. Franco<sup>1</sup>, X. Bai<sup>2</sup>, S. El Kazzi<sup>1</sup>, B. Kunert<sup>1</sup>, Y. Mols<sup>1</sup>, C. Porret<sup>3</sup>, T. Maurice<sup>1</sup>, F. Holsteyns<sup>1</sup>, S. De Gendt<sup>1,4</sup>, M. Caymax<sup>1</sup>, M. Heyns<sup>1,4</sup>, N. Collaert<sup>1</sup>, and A. Thean<sup>1</sup>, <sup>1</sup>*imec, Belgium*, <sup>2</sup>*Stanford U.*, <sup>3</sup>*Riber, France*, <sup>4</sup>*U. Leuven, Belgium*
- 10:10 AM 2.10 - **Surface passivation of InGaAs(001)-(2x4) by self-limiting CVD of a silicon control monolayer**, M. Edmonds<sup>1</sup>, T. J. Kent<sup>1</sup>, M. Chang<sup>2</sup>, J.Kachian<sup>2</sup>, R. Droopad<sup>2</sup>, E. Chagarov<sup>1</sup>, and A. C. Kummel<sup>1</sup>, <sup>1</sup>*UC San Diego*, <sup>2</sup>*Applied Materials*, <sup>3</sup>*Texas State U.*
- 10:12 AM 2.11 - **Comparison of MBE-Y<sub>2</sub>O<sub>3</sub> and ALD-Y<sub>2</sub>O<sub>3</sub> passivated n-GaSb(100)**, Y. H. Lin<sup>1</sup>, R. L. Chu<sup>2</sup>, W. J. Hsueh<sup>3</sup>, K. Y. Lin<sup>1</sup>, T. H. Chiang<sup>2</sup>, C. H. Fu<sup>1</sup>, T. W. Pi<sup>4</sup>, J. I. Chyi<sup>3</sup>, J. Kwo<sup>2</sup>, and M. Hong<sup>1</sup>, <sup>1</sup>*National Taiwan U., Taiwan*, <sup>2</sup>*National Tsing Hua U., Taiwan*, <sup>3</sup>*National Central U., Taiwan*, <sup>4</sup>*National Synchrotron Radiation Research Center, Taiwan*
- 10:14 AM 2.12 - **AlN for improved interface passivation of III-V semiconductor MOSFETs**, Y. Guo and J. Robertson, *Cambridge U., UK*
- 10:16 AM Coffee break

## Session 3 - III-V

Session Chair: M. Hong

- 10:40 AM Opening remarks
- 10:45 AM 3.1 **Invited - High k oxides on (In)GaAs surfaces studied by synchrotron radiation photoemission**, T. W. Pi<sup>1</sup>, Y. T. Fanchiang<sup>2</sup>, Y. H. Lin<sup>2</sup>, T. H. Chiang<sup>3</sup>, K. Y. Lin<sup>2</sup>, Y. K. Su<sup>3</sup>, C. H. Wei<sup>1</sup>, Y. C. Lin<sup>1</sup>, G. K. Wertheim<sup>4</sup>, J. Kwo<sup>3</sup>, and M. Hong<sup>2</sup>, <sup>1</sup>National Synchrotron Radiation Research Center, Taiwan, <sup>2</sup>National Taiwan U., Taiwan, <sup>3</sup>National Tsing Hua U., Taiwan, <sup>4</sup>Woodland Consulting
- 11:20 AM 3.2 - **A distributed Admittance Model to study Border Traps Capture/Emission in High-K/III-V MOS devices and its dependence on physical and electrical parameters**, A. Vais<sup>1,2</sup>, K. Martens<sup>1</sup>, D. Lin<sup>1</sup>, N. Collaert<sup>1</sup>, K. De Meyer<sup>1,2</sup>, and A. Thean<sup>1</sup>, <sup>1</sup>imec, Belgium, <sup>2</sup>U. Leuven, Belgium
- 11:40 AM 3.3 - **A Novel Crystalline Oxide Passivation for Al<sub>2</sub>O<sub>3</sub>/AlGaIn/GaN**, X. Qin, H. Dong, J. Kim, and R. M. Wallace, *UT Dallas*
- 12:00 PM Adjourn for lunch

## Session 4 - High-k Dielectrics I

Session Chair: V. V. Afanas'ev

- 1:30 PM Opening remarks
- 1:35 PM 4.1 **Invited - Single-crystal oxide insulators grown epitaxially on GaAs, Ge and GaN by ALD**, R. G. Gordon, X. Liu, X. Wang, and S. B. Kim, *Harvard U.*
- 2:10 PM 4.2 - **Paramagnetic oxide defects in Sc<sub>2</sub>O<sub>3</sub>-passivated (100)Ge/HfO<sub>2</sub> stacks**, A. Stesmans<sup>1</sup>, S. Iacovo<sup>1</sup>, D. Cott<sup>2</sup>, A. Thean<sup>2</sup>, H. Arimura<sup>2</sup>, S. Sioncke<sup>2</sup>, and V. V. Afanas'ev<sup>1</sup>, <sup>1</sup>U. Leuven, Belgium, <sup>2</sup>imec, Belgium
- 2:35 PM 4.3 - **Interfacial layer (IL) formation and its impact on physical & electrical properties of metal/high-k/Si<sub>x</sub>Ge<sub>1-x</sub> gate stack**, S. Siddiqui<sup>1</sup>, L. F. Edge<sup>2</sup>, P. Srinivasan<sup>1</sup>, J. Fronheiser<sup>1</sup>, R. Muthinti<sup>2</sup>, V. Narayanan<sup>2</sup>, and H. Jagannathan<sup>2</sup>, <sup>1</sup>GLOBALFOUNDRIES, <sup>2</sup>IBM
- 2:55 PM 4.4 - **High-k/InAs Interface Metrics and Comparison with GaAs**, M. Passlack<sup>1</sup>, G. Doornbos<sup>1</sup>, T. Vasen<sup>1</sup>, C. H. Wang<sup>1</sup>, S. W. Wang<sup>1</sup>, R. Contreras-Guerrero<sup>2</sup>, J. Rojas-Ramirez<sup>2</sup>, P. Ramvall<sup>1</sup>, G. Vellianitis<sup>1</sup>, R. Oxland<sup>1</sup>, M. C. Holland<sup>1</sup>, R. Droopad<sup>2</sup>, and C.H. Diaz<sup>3</sup>, <sup>1</sup>TSMC, Belgium, <sup>2</sup>Texas State U., <sup>3</sup>TSMC, Taiwan
- 3:15 PM 4.5 - **Improvement of Electrical Properties of InGaAs MOS Interfaces by Inserting La oxide interfacial layers into InGaAs High-k Gate Stacks**, C.-Y. Chang<sup>1,2</sup>, M. Takenaka<sup>1,2</sup>, and S. Takagi<sup>1,2</sup>, <sup>1</sup>U. Tokyo, Japan, <sup>2</sup>JST-CREST, Japan
- 3:35 PM Coffee break

## Session 5 - Poster Preview Session II High-k Dielectrics

Session Chair: A. Demkov

- 4:00 PM 5.1 - **Experimental Investigation on Electric Dipole at Al<sub>2</sub>O<sub>3</sub>/SiC Interface**, X. L. Wang<sup>1</sup>, W. W. Wang<sup>1</sup>, J. J. Xiang<sup>1</sup>, J. Zhang<sup>2</sup>, H. Yang<sup>1</sup>, J. Yan<sup>1</sup>, C. Zhao<sup>1</sup>, D. P. Chen<sup>1</sup>, and T. C. Ye<sup>1</sup>, <sup>1</sup>*Chinese Academy of Sciences, China*, <sup>2</sup>*North China U. Technology, China*
- 4:02 PM 5.2 - **High-k/SiGe Interface Passivation by H<sub>2</sub>O<sub>2</sub>/HF Cleaning Technique**, L. Zhang<sup>1</sup>, V. Hassan<sup>2</sup>, C.-W. Lo<sup>2</sup>, C. Olsen<sup>2</sup>, M. A. Foad<sup>2</sup>, S. Siddique<sup>3</sup>, B. Sahu<sup>3</sup>, and P. C. McIntyre<sup>1</sup>, <sup>1</sup>*Stanford U.*, <sup>2</sup>*Applied Materials*, <sup>3</sup>*GLOBALFOUNDRIES*
- 4:04 PM 5.3 - **Achieving of Ultra High Electron Density on GaN Surface by Ionic Liquid Gating**, H. Zhou and P. D. Ye, *Purdue U.*
- 4:06 PM 5.4 - **Infrared Spectroscopic Study on Near-Interface Structure of Thermally-Grown Oxides and Oxidation-Induced Byproducts at 4H-SiC/SiO<sub>2</sub> Interface**, H. Hirai<sup>1</sup> and K. Kita<sup>1,2</sup>, <sup>1</sup>*U. Tokyo, Japan*, <sup>2</sup>*JST-PRESTO, Japan*
- 4:08 PM 5.5 - **Density-Functional Theory Molecular Dynamics Simulations of High-K Dielectrics on SiGe and GaN Substrates.**, E. Chagarov and A. C. Kummel, *UC San Diego*
- 4:10 PM 5.6 - **Plasma Enhanced Atomic Layer Deposition of Low Voltage Nonlinearity Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> Metal-Insulator-Insulator-Metal (MIIM) Capacitors**, D. Z. Austin<sup>1,2</sup>, D. Allman<sup>2</sup>, D. Price<sup>2</sup>, S. Hose<sup>2</sup>, and J. F. Conley Jr<sup>1</sup>, <sup>1</sup>*Oregon State U.*, <sup>2</sup>*ON Semiconductor*
- 4:12 PM 5.7 - **Structure of Low-Temperature TiO<sub>2</sub>/Si Interface and Impact on Surface Recombination for Low-Cost Si-based PV**, J. Jhaveri, G. Sahasrabudhe, G. Man, K. Nagamatsu, S. Wagner, A. Kahn, J. Schwartz, and J. C. Sturm, *Princeton U.*
- 4:14 PM 5.8 - **A Demonstration of the Utility of the Half-Field Response of Electrically Detected Magnetic Resonance and Defect Concentration Measurements in Insulators and at Semiconductor/Insulator Interfaces**, M. Mutch, M. A. Anders, C. J. Cochrane, and P. M. Lenahan, *Pennsylvania State U.*
- 4:16 PM 5.9 - **Al<sub>2</sub>O<sub>3</sub>/TiO<sub>2</sub> bilayers as passivation and antireflection coating on silicon**, C.-T. Lu, Q.-Q. Chen, and C. W. Liu, *National Taiwan U., Taiwan*
- 4:18 PM 5.10 - **Small Variability and Its Mechanism of Poly-Si/High-k/SiON Gate Stack For Silicon on Thin BOX (SOTB) Transistor**, Y. Yamamoto<sup>1</sup>, H. Makiyama<sup>1</sup>, T. Yamashita<sup>1</sup>, H. Oda<sup>1</sup>, S. Kamohara<sup>1</sup>, N. Sugii<sup>1</sup>, Y. Yamaguchi<sup>1</sup>, T. Mizutani<sup>2</sup>, and T. Hiramoto<sup>2</sup>, <sup>1</sup>*LEAP, Japan*, <sup>2</sup>*U. Tokyo, Japan*
- 4:20 PM 5.11 - **Improved performance of pentacene organic thin-film transistor by using fluorine-implanted HfLaO as gate dielectric**, C. Y. Han<sup>1</sup>, W. M. Tang<sup>2</sup>, C. H. Leung<sup>1</sup>, C. M. Che<sup>1</sup>, and P. T. Lai<sup>1</sup>, <sup>1</sup>*U. Hong Kong, Hong Kong*, <sup>2</sup>*Hong Kong Polytechnic U., Hong Kong*
- 4:22 PM 5.12 - **Polymorphous LaLuO<sub>3</sub>: a universal material as gate dielectric**, A. Schäfer<sup>1,2</sup>, M. Luysberg<sup>1</sup>, F. Wendt<sup>1,2</sup>, G. Niu<sup>3</sup>, T. Schroeder<sup>3</sup>, S. Mantl<sup>1,2</sup>, H. Hardtdegen<sup>1,2</sup>, M. Mikulics<sup>1,2</sup>, and J. Schubert<sup>1,2</sup>, <sup>1</sup>*Forschungszentrum Juelich, Germany*, <sup>2</sup>*JARA, Germany*, <sup>3</sup>*IHP, Germany*
- 4:24 PM 5.13 - **Electronic state configuration of plasma-enhanced atomic layer deposited SiO<sub>2</sub>**, B. S. Eller, J. Yang, and R. J. Nemanich, *ASU*

- 4:26 PM 5.14 - **Interfacial Oxide Formation during Deposition of Al<sub>2</sub>O<sub>3</sub> on Silicon via Prompt Inorganic Condensation (PIC)**, S. W. Smith, D. A. Keszler, and J. F. Conley Jr, *Oregon State U.*
- 4:28 PM 5.15 - **Si/HfO<sub>2</sub> Interface Modification by Proton Irradiation: Experimentation & Analysis**, S. Maurya and M. Radhakrishna, *IIT Allahabad, India*
- 4:30 PM 5.16 - **The Transient Leakage from Spatial Transportation of Phosphorus Contaminants on Gate Oxide Integrity (GOI)**, L. Sheng, B. Williams, T. Haskett, and E. Glines, *ON Semiconductor*
- 4:32 PM 5.17 - **Bonding, Stability and Band Offsets of GaN/HfO<sub>2</sub> Interface Influenced by Interfacial Oxygen Content: A First-Principles Study**, Z. F. Zhang, C. H. Wang, R. Y. Cao, H. B. Li, and W. C. Wang, *Nankai U., China*
- 4:34 PM 5.18 - **InGaAs Passivation with an ALD ZnO Interlayer: Electrical and XPS Characterization**, A. T. Lucero, Y.-C. Byun, X. Qin, R. M. Wallace, and J. Kim, *UT Dallas*
- 4:36 PM 5.19 - **Effect of Post-deposition Annealing on Threshold Voltage and Interface States in ALD-Al<sub>2</sub>O<sub>3</sub>/AlGaIn/GaN MIS-HEMTs on Si Substrates**, T. Kubo, Y. Yoshida, and T. Egawa, *Nagoya Institute of Technology, Japan*
- 4:38 PM 5.20 - **Etching Techniques for the Ge Triangular-channel Ge NFETs on Si**, C.-L. Chu, S.-H. Hsu, and G.-L. Luo, *National Nano Device Laboratories, Taiwan*
- 4:40 PM 5.21 - **Structural and optical evaluation of SiO<sub>2</sub>/AlGaIn/GaN and SiN/AlGaIn/GaN MIS heterostructures and correlation with electrical properties**, S. Ghosh, S. K. Jana, S. M. Dinara, A. Chakraborty, A. Bag, M. Mahata, P. Mukhopadhyay, and D. Biswas, *IIT Kharagpur, India*
- 4:42 PM 5.22 - **Sulfur Passivation Enhancement for GaSb MOS Devices by Adding H<sub>2</sub>O<sub>2</sub> to (NH<sub>4</sub>)<sub>2</sub>S Solution**, A. Z. Tan<sup>1</sup>, B. L. Zhao<sup>1</sup>, C. Z. Zhang<sup>1,2</sup>, D. B. Shan<sup>1</sup>, E. J. Wang<sup>1</sup>, and F. J. Xu<sup>1</sup>, <sup>1</sup>*Tsinghua U., China*, <sup>2</sup>*Beijing Institute of Technology, China*
- 4:44 PM 5.23 - **Study of SiO<sub>x</sub>-Based Resistive Switching Memory (ReRAM) in Integrated One Diode – One Resistor (1D-1R) Architecture**, Y. F. Chang<sup>1</sup>, B. Fowler<sup>2</sup>, F. Zhou<sup>1</sup>, K. Byun<sup>1</sup>, J. C. Lee<sup>1</sup>, <sup>1</sup>*UT Austin*, <sup>2</sup>*PrivaTran*

## Session 6 - Wide Bandgap Semiconductors

Session Chair: P. Lenahan

- 4: 50PM 6.1 *Invited* - **Dielectric/III-N Interfaces with Nitridation Interlayer for GaN Power Electronics**, K. J. Chen, S. Yang, Z. Tang, and S. Huang, *Hong Kong U. Science and Technology, Hong Kong*
- 5:25 PM 6.2 - **Demonstration of High Channel Mobility in 4H-SiC MOSFETs by Utilizing Boron-Doped Gate Oxide**, D. Okamoto<sup>1</sup>, M. Sometani<sup>1</sup>, S. Harada<sup>1</sup>, R. Kosugi<sup>1</sup>, Y. Yonezawa<sup>1</sup>, and H. Yano<sup>2</sup>, <sup>1</sup>*AIST, Japan*, <sup>2</sup>*U. Tsukuba, Japan*
- 5:45 PM Adjourn

## Poster Session I

Session Chairs: A. Demkov and P. D. Ye

7:00 PM – 10:00 PM Poster Session I

10:00 PM – Midnight Hospitality Room

# Friday, December 12, 2014

## Session 7 - Two-Dimensional Materials I

Session Chair: J. Lisoni

- 8:00 AM Morning announcement and opening remarks
- 8:05 AM 7.1 *Invited - 2D Materials Growth and Prospects*, L. Colombo<sup>1</sup>, S. Banerjee<sup>2</sup>, R. M. Wallace<sup>3</sup>, and C. L. Hinkle<sup>3</sup>, <sup>1</sup>Texas Instruments, <sup>2</sup>UT Austin, <sup>3</sup>UT Dallas
- 8:40 AM 7.2 *Invited - Carrier response in electric-field-induced bandgap of bilayer graphene*, K. Nagashio, *U. Tokyo, Japan*
- 9:15 AM 7.3 - **Computational Study of Interfaces between 2D MoS<sub>2</sub> and Surroundings**, J. Kang, W. Liu, and K. Banerjee, *UC Santa Barbara*
- 9:35 AM 7.4 - **Simple Test Structure for the Electrical Characterization of MoS<sub>2</sub> Interface Functionalization with High-k Dielectrics**, P. B. Vyas, S. McDonnell, P. Bolshakov-Barrett, A. Azcatl, C. L. Hinkle, R. M. Wallace, and C. D. Young, *UT Dallas*
- 9:55 AM Coffee break

## Session 8 - Two-Dimensional Materials II

Session Chair: B. H. Lee

- 10:20 AM 8.1 *Invited - Contact engineering, chemical doping and heterostructures of layered chalcogenides*, A. Javey, *UC Berkeley*
- 10:55 AM 8.2 - **Contact Resistance Reduction for MoS<sub>2</sub> FETs with Insulating Layers**, W. Park, Y. H. Kim, S. K. Lee, U. Jung, J. H. Yang, C. Cho, Y. J. Kim, S. K. Lim, and B. H. Lee, *GIST, Korea*
- 11:15 AM 8.3 - **Ultra-low noise in high performance short channel few-layer MoS<sub>2</sub> transistors**, X. F. Li<sup>1</sup>, L. M. Yang<sup>2</sup>, P. D. Ye<sup>2</sup>, and Y. Q. Wu<sup>1</sup>, <sup>1</sup>Huazhong U. Science and Technology, China, <sup>2</sup>Purdue U.
- 11:35 AM 8.4 - **Will Monolayer Black Phosphorus be a useful 2-D Semiconductor?**, Y. Guo and J. Robertson, *Cambridge U., UK*
- 11:55 AM 8.5 - **HfSe<sub>2</sub> Thin Films: 2D Transition Metal Dichalcogenides Grown by MBE**, A. Barton<sup>1</sup>, R. Yue<sup>1</sup>, S. McDonnell<sup>1</sup>, R. Addou<sup>1</sup>, A. Azcatl<sup>1</sup>, H. Zhu<sup>1</sup>, L. Ning<sup>1</sup>, X. Peng<sup>1</sup>, L. Colombo<sup>2</sup>, J. Kim<sup>1</sup>, M. Kim<sup>1</sup>, R. M. Wallace<sup>1</sup>, and C. L. Hinkle<sup>1</sup>, <sup>1</sup>UT Dallas, <sup>2</sup>Texas Instruments
- 12:15 PM Adjourn for lunch
- 12:15 PM – 2:00 PM Committee / Invited Speaker Luncheon

## Session 9 – Poster Preview Session III 2D/Reliability

Session Chair: C. L. Hinkle

- 2:00 PM Opening remarks
- 2:02 PM 9.1 - **Tuning the Threshold Voltage of 2D Material-based Field-Effect Transistors via CMOS-Compatible Processes**, W. S. Leong, Y. Li, and J. T. L. Thong, *National U. Singapore, Singapore*
- 2:04 PM 9.2 - **MoO<sub>3</sub> as a p-type contact on MoS<sub>2</sub>**, Y. Guo, H. Li, and J. Robertson, *Cambridge U., UK*
- 2:06 PM 9.3 - **Solution Phase deposition of Titanyl Phthalocynine and cobalt crown ether phthalocyanine as a Seeding Layer for Al<sub>2</sub>O<sub>3</sub> on Graphene**, I. Kwak, J. H. Park, and A. C. Kummel, *UC San Diego*
- 2:08 PM 9.4 - **Exploring MoS<sub>2</sub> interface engineering using MOS capacitor structures with high quality ALD alumina**, S. Mukherjee, H. Zheng, V. Su, K. Gangopadhyay, and S. Gangopadhyay, *U. Missouri*
- 2:10 PM 9.5 - **Ballistic transport in graphene-like group-IV nanoribbons: A first-principles study**, M. Houssa<sup>1</sup>, K. Iordanidou<sup>1</sup>, B. van den Broek<sup>1</sup>, A. Lu<sup>1,2</sup>, G. Pourtois<sup>2</sup>, V. V. Afanas'ev<sup>1</sup>, and A. Stesmans<sup>1</sup>, <sup>1</sup>*U. Leuven, Belgium*, <sup>2</sup>*imec, Belgium*
- 2:12 PM 9.6 - **Hot Carrier Injection Study of GaAs(111)A MOSFETs with Atomic Layer Epitaxial La<sub>2</sub>O<sub>3</sub> as Gate Dielectric**, J. Zhang<sup>1</sup>, X. B. Lou<sup>2</sup>, X. W. Wang<sup>2</sup>, L. Dong<sup>1</sup>, X. F. Li<sup>1</sup>, N. J. Conrad<sup>1</sup>, M. Si<sup>1</sup>, R. G. Gordon<sup>2</sup>, and P. D. Ye<sup>1</sup>, <sup>1</sup>*Purdue U.*, <sup>2</sup>*Harvard U.*
- 2:14 PM 9.7 - **Low Frequency Noise of Near-Ballistic III-V Nanowire MOSFETs**, M. Si, N. J. Conrad, J. J. Gu, J. Zhang, and P. D. Ye, *Purdue U.*
- 2:16 PM 9.8 - **Radiation Hardness of InGaAs Nanowire Gate-All-Around MOSFETs**, S. Ren<sup>1</sup>, M. Si<sup>2</sup>, K. Ni<sup>3</sup>, S. Chang<sup>1</sup>, X. Sun<sup>1</sup>, E. X. Zhang<sup>3</sup>, D. M. Fleetwood<sup>3</sup>, P. D. Ye<sup>2</sup>, S. Cui<sup>1</sup>, and T. P. Ma<sup>1</sup>, <sup>1</sup>*Yale U.*, <sup>2</sup>*Purdue U.*, <sup>3</sup>*Vanderbilt U.*
- 2:18 PM 9.9 - **Point Defects in SiC MOSFET Bias Temperature Instabilities**, M. A. Anders<sup>1</sup>, P. M. Lenahan<sup>1</sup>, J. Follman<sup>1</sup>, S. D. Arthur<sup>2</sup>, J. McMahon<sup>2</sup>, L. Yu<sup>2</sup>, X. Zhu<sup>2</sup>, and A. J. Lelis<sup>3</sup>, <sup>1</sup>*Pennsylvania State U.*, <sup>2</sup>*General Electric Global Research*, <sup>3</sup>*U.S. Army Research Laboratory*
- 2:20 PM 9.10 - **Ultrathin SiO<sub>2</sub> Tunnel Oxide and ALD-TiO<sub>2</sub> Leaky Oxide Protective Layers for Silicon Water-Splitting Cells**, A. G. Scheuermann<sup>1</sup>, D. Q. Lu<sup>1</sup>, T. Ito<sup>1,2</sup>, C. E. D. Chidsey<sup>1</sup>, and P. C. McIntyre<sup>1</sup>, <sup>1</sup>*Stanford U.*, <sup>2</sup>*Tokyo Electron*
- 2:22 PM 9.11 - **Analysis on Trapping Mechanism of Trap Causing Gate-Induced Drain Leakage Current Random Telegraph Noise**, S.-W. Yoo, Y.-S. Seo, and H. Shin, *Seoul National U., Korea*
- 2:24 PM 9.12 - **Electrical properties and reliability of decoupling MIM capacitors employing Ta<sub>2</sub>O<sub>5</sub> and ZrO<sub>2</sub> based high-k dielectrics**, M. Czernohorsky<sup>1</sup>, K. Seidel<sup>1</sup>, W. Weinreich<sup>1</sup>, P. Polakowski<sup>1</sup>, J. Sundqvist<sup>1</sup>, M. G. Nolan<sup>2</sup>, and D. H. Triyoso<sup>3</sup>, <sup>1</sup>*Fraunhofer IPMS-CNT, Germany*, <sup>2</sup>*GLOBALFOUNDRIES, Germany*, <sup>3</sup>*GLOBALFOUNDRIES*

## Session 10 - Heterogeneous Integration

Session Chairs: C. Marchiori

- 2:30 PM Opening remarks
- 2:35 PM 10.1 **Invited - In-situ probing surfaces of oxide electronic materials with atomic resolution: physical functionalities and memristive mechanisms**, S. V. Kalinin, *Oak Ridge National Laboratory*
- 3:10 PM 10.2 - **Carrier Density Modulation in Ge Heterostructure by Ferroelectric Switching**, P. Ponath<sup>1</sup>, K. Fredrickson<sup>1</sup>, A. B. Posadas<sup>1</sup>, Y. Ren<sup>1</sup>, X. Wu<sup>1</sup>, R. K. Vasudevan<sup>2</sup>, M. B. Okatan<sup>2</sup>, S. Jesse<sup>2</sup>, T. Aoki<sup>3</sup>, M. R. McCartney<sup>3</sup>, D. J. Smith<sup>3</sup>, S. V. Kalinin<sup>2</sup>, K. Lai<sup>1</sup>, and A. A. Demkov<sup>1</sup>, <sup>1</sup>*UT Austin*, <sup>2</sup>*Oak Ridge National Laboratory*, <sup>3</sup>*ASU*
- 3:30 PM Coffee break

## Session 11 - Poster Preview Session IV Heterogeneous Integration/Memory

Session Chairs: M. M. Frank

- 4:00 PM Opening remarks
- 4:02 PM 11.1 - **A Reliable Tantalum Oxide-based ReRAM with Ultralow Voltage Switching for Fully CMOS-compatible 1T1R Integration**, C.-H. Lin<sup>1</sup>, M.-C. Chen<sup>1</sup>, Y.-F. Hou<sup>1</sup>, Y.-H. Lin<sup>2</sup>, J.-Y. Hsu<sup>2</sup>, Y.-H. Cheng<sup>3</sup>, P.-C. Su<sup>3</sup>, Y.-J. Chen<sup>1</sup>, C.-Y. Lin<sup>1</sup>, K.-H. Li<sup>1</sup>, M.-T. Lee<sup>1</sup>, C.-A. Chung<sup>1</sup>, W.-K. Yeh<sup>1</sup>, and T. Wang<sup>3</sup>, <sup>1</sup>*National Nano Device Laboratories, Taiwan*, <sup>2</sup>*National United U., Taiwan*, <sup>3</sup>*National Chiao-Tung U., Taiwan*
- 4:04 PM 11.2 - **Impacts of HfO<sub>2</sub>/SiN trapping layer and in-situ doped poly-Si channel on 3D stacked junctionless flash memory device**, K.-C. Chou, K.-S. Chang-Liao, C.-Y. Chen, and P.-H. Chen, *National Tsing Hua U., Taiwan*
- 4:06 PM 11.3 - **First Principles Calculations of Chemical Trends of Oxide RRAM Mechanisms**, Y. Guo and J. Robertson, *Cambridge U., UK*
- 4:08 PM 11.4 - **Low-current conductive filament instability in conductive-bridging memories for non-volatile multilevel cells**, U. Celano<sup>1,2</sup>, L. Goux<sup>1</sup>, K. Opsomer<sup>1</sup>, C. Detavernier<sup>3</sup>, M. Jurczak<sup>1</sup>, and W. Vandervorst<sup>1,2</sup>, <sup>1</sup>*imec, Belgium*, <sup>2</sup>*U. Leuven, Belgium*, <sup>3</sup>*U. Gent, Belgium*
- 4:10 PM 11.5 - **Polycrystalline III-V materials characteristics and implementation in vertical channel NAND structures**, E. Capogreco<sup>1</sup>, J. G. Lisoni<sup>1</sup>, C. Merckling<sup>1</sup>, T. Numata<sup>2</sup>, A. Arreghini<sup>1</sup>, K. De Meyer<sup>1</sup>, G. Van den Bosch<sup>1</sup>, and J. Van Houdt<sup>1</sup>, <sup>1</sup>*imec, Belgium*, <sup>2</sup>*Toshiba, Belgium*
- 4:12 PM 11.6 - **Resistive switching and neuromorphic functionality of fully-ALD grown HfO<sub>2</sub>-based stacks**, Yu. Matveyev, K. Egorov, A. Markeev, and A. Zenkevich, *Moscow Institute of Physics and Technology, Russia*
- 4:14 PM 11.7 - **Electrical characteristics of Si nanocrystal filament in unipolar SiO<sub>x</sub> based RRAM**, K. Byun<sup>1</sup>, F. Zhou<sup>1</sup>, B. Fowler<sup>2</sup>, Y. F. Chang<sup>1</sup>, and J. C. Lee<sup>1</sup>, <sup>1</sup>*UT Austin*, <sup>2</sup>*PrivaTran*

- 4:16 PM **11.8 - Highly uniform and robust retention under 30  $\mu$ A current operation by inserting ultrathin  $\text{Al}_2\text{O}_3$  layer in  $\text{TaO}_x$ -based RRAM**, S. Samanta<sup>1</sup>, D. Jana<sup>1</sup>, S. Chakrabarti<sup>1</sup>, M. Dutta<sup>1</sup>, S. Roy<sup>1</sup>, R. Mahapatra<sup>1,2</sup>, S. Maikap<sup>1</sup>, W. S. Chen<sup>3</sup>, F. T. Chen<sup>3</sup>, and M. J. Tsai<sup>3</sup>, <sup>1</sup>*Chang Gung U., Taiwan*, <sup>2</sup>*National Institute of Technology, India*, <sup>3</sup>*Industrial Technology Research Institute, Taiwan*
- 4:18 PM **11.9 - Comparative HRXRD and XRR analysis of GaN/AlGaN heterostructure on  $\text{Al}_2\text{O}_3$  and Si (111) substrate grown by PAMBE**, S. K. Jana, S. Ghosh, S. M. Dinara, A. Chakraorty, and D. Biswas, *IIT Kharagpur, India*
- 4:20 PM **11.10 - First-Principle Simulations of Photovoltaic CZTS/Se Materials.**, A. C. Kummel<sup>1</sup>, E. Chagarov<sup>1</sup>, D. B. Mitzi<sup>2</sup>, R. Haight<sup>2</sup>, <sup>1</sup>*UC San Diego*, <sup>2</sup>*IBM*
- 4:22 PM **11.11 - Electrical Properties of the CdS/Cu(In,Ga)Se<sub>2</sub> Interface in Photovoltaic Devices**, J.V. Li, L.M. Mansfield, B. Egaas, and K. Ramanathan, *National Renewable Energy Laboratory*
- 4:24 PM **11.12 - Designing Conductive Layers for Fully Integrated Oxide Electronics**, A. O'Hara<sup>1</sup>, M. Choi<sup>1</sup>, A. B. Posadas<sup>1</sup>, C. A. Rodriguez<sup>2</sup>, H. Seinige<sup>1</sup>, A. J. Kellock<sup>3</sup>, M. M. Frank<sup>3</sup>, M. Tsoi<sup>1</sup>, S. Zollner<sup>2</sup>, V. Narayanan<sup>3</sup>, and A. A. Demkov<sup>1</sup>, <sup>1</sup>*UT Austin*, <sup>2</sup>*New Mexico State Univeristy*, <sup>3</sup>*IBM*
- 4:26 PM **11.13 - Multi-bit Processing in Sub-8nm FETs Incorporating Quantum Dot Channels**, F. Jain<sup>1</sup>, P.-Y. Chan<sup>1</sup>, M. Lingalugari<sup>1</sup>, J. Kondo<sup>1</sup>, P. Gogna<sup>2</sup>, J. Chandy<sup>1</sup>, and E. Heller<sup>3</sup>, <sup>1</sup>*U. Connecticut*, <sup>2</sup>*Intel*, <sup>3</sup>*Synopsys*
- 4:28 PM **11.14 - Nano-Electronics based on Metal-Insulator Transition Materials? – the prototypal case of  $\text{VO}_2$** , K. Martens<sup>1,2</sup>, I. P. Radu<sup>1</sup>, A. Peter<sup>1</sup>, N. Xu<sup>3</sup>, G. Rampelberg<sup>4</sup>, D. Esfahani<sup>5</sup>, F. Peeters<sup>5</sup>, C. Adelman<sup>1</sup>, C. Detavernier<sup>4</sup>, M. Heyns<sup>1,2</sup>, and M. Jurczak<sup>1</sup>, <sup>1</sup>*imec, Belgium*, <sup>2</sup>*U. Leuven, Belgium*, <sup>3</sup>*UC Berkeley*, <sup>4</sup>*Gent U., Belgium*, <sup>5</sup>*U. Antwerp, Belgium*
- 4:30 PM **11.15 - Temperature and Long Time Annealing Impact on Low Proton Energy Irradiated 4H-SiC nMOSFET**, M. Florentin<sup>1</sup>, M. Alexandru<sup>2</sup>, A. Constant<sup>3</sup>, J. Montserrat<sup>1</sup>, B. Schmidt<sup>4</sup>, P. Godignon<sup>1</sup>, <sup>1</sup>*National Center of Microelectronics-Barcelona, Spain*, <sup>2</sup>*Technische U. Dresden, Germany*, <sup>3</sup>*ON Semiconductor, Belgium*, <sup>4</sup>*Helmholtz-Zentrum, Germany*
- 4:32 PM **11.16 - Enhancing the Performance of Metal/Insulator/Insulator/Metal (MIIM) Tunnel Diodes via Defect Enhanced Direct Tunneling (DEDT)**, J. F. Conley Jr and N. Alimardani, *Oregon State U.*
- 4:34 PM **11.17 - Capacitance nonlinearity in metal oxide based metal-insulator-metal structure**, L. Kankate and H. Kliem, *Saarland U., Germany*
- 4:36 PM **11.18 - Influence of Carrier Traps on Real SiC High-Voltage MOSFET Applications**, Y. Tanimoto<sup>1</sup>, A. Saito<sup>1</sup>, K. Matsuura<sup>1</sup>, H. Kikuchihara<sup>1</sup>, H. J. Mattausch<sup>1</sup>, M. Miura-Mattausch<sup>1</sup>, and N. Kawamoto<sup>2</sup>, <sup>1</sup>*Hiroshima U., Japan*, <sup>2</sup>*Rohm Corp., Japan*
- 4:38 PM **11.19 - Density functional theory study on oxidation of SiC**, T. Ono and S. Saito, *Osaka U., Japan*
- 4:40 PM **11.20 - Recipe for Synthesizing Silicene on Insulators**, K. Shiraishi<sup>1</sup>, H. Shirakawa<sup>2</sup>, S. Tanaya<sup>2</sup>, and Y. Hatsugai<sup>2</sup>, <sup>1</sup>*Nagoya U., Japan*, <sup>2</sup>*U. Tsukuba, Japan*
- 4:42 PM **11.21 - Reduced Metal Contact Resistance To Silicon Using Al Based Interlayers**, S. Ganti, E. Arac, P. J. King, A. J. Barlow, P. J. Cumpson, and A. G. O'Neill, *Newcastle U., UK*



- 4:44 PM 11.22 - **The Effect of Platinum Nanocluster Size on Fermi Level Depinning of Titanium Metal Contact on Silicon**, H. Zheng<sup>1</sup>, S. C. Su<sup>1</sup>, S. Mukherjee<sup>1</sup>, K. Gangopadhyay<sup>1,2</sup>, and S. Gangopadhyay<sup>1</sup>, <sup>1</sup>*U. Missouri*, <sup>2</sup>*Nanos Technologies*
- 4:46 PM 11.23 - **Crystal Face Dependence of the Interaction of Water with SiC-MOS Structures: Structure and Electronic Properties**, G. Liu<sup>1</sup>, C. Xu<sup>1</sup>, B. Yakshinskiy<sup>1</sup>, L. Wielunski<sup>1</sup>, T. Gustafsson<sup>1</sup>, J. Bloch<sup>1,2</sup>, S. Dhar<sup>3</sup>, and L. C. Feldman<sup>1</sup>, <sup>1</sup>*Rutgers U.*, <sup>2</sup>*NRCN, Israel*, <sup>3</sup>*Auburn U.*
- 4:48 PM 11.24 - **Effect of Chemical Wet Cleaning on Surface Composition of Thin Film CZTS<sub>Se</sub>**, K. Sardashti<sup>1</sup>, S. Park<sup>1</sup>, A. C. Kummel<sup>1</sup>, R. Haight<sup>2</sup>, W. Wang<sup>2</sup>, and D. B. Mitzi<sup>2</sup>, <sup>1</sup>*UC San Diego*, <sup>2</sup>*IBM*
- 4:50 PM Adjourn

## Poster Session II

Session Chair: A. Demkov and P. D. Ye

4:50 PM – 6:50 PM Poster Session II

7:00 PM – 10:00 PM Conference Banquet and Limerick Contest

10:00 PM – Midnight Hospitality Room

## Saturday, December 13, 2014

8:00 AM Morning announcements

### Session 12 - Memory

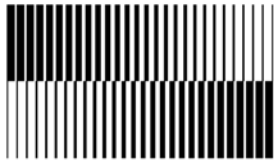
Session Chair: M. Passlack

- 8:05 AM Opening remarks
- 8:10 AM 12.1 *Invited* - **Memory technologies for the terabit era: a paradigm shift**, J. Van Houdt, *imec, Belgium*
- 8:45 AM 12.2 *Invited* - **Memcomputing: computing with and in memory**, M. Di Ventra<sup>1</sup>, F. L. Traversa<sup>1</sup>, Y. V. Pershin<sup>2</sup>, <sup>1</sup>*UC San Diego*, <sup>2</sup>*U. South Carolina*
- 9:20 AM 12.3 - **SrTiO<sub>3</sub> for sub-20 nm DRAM technology nodes—characterization and modeling**, B. Kaczer<sup>1</sup>, L. Larcher<sup>2,3</sup>, L. Vandelli<sup>2,3</sup>, H. Reisinger<sup>4</sup>, M. Popovici<sup>1</sup>, S. Clima<sup>1</sup>, Z. Ji<sup>5</sup>, S. Joshi<sup>6</sup>, J. Swerts<sup>1</sup>, A. Redolfi<sup>1</sup>, V. V. Afanas'ev<sup>6</sup>, and M. Jurczak<sup>1</sup>, <sup>1</sup>*imec, Belgium*, <sup>2</sup>*U. Modena e Reggio Emilia, Italy*, <sup>3</sup>*MDLab, Italy*, <sup>4</sup>*Infineon, Germany*, <sup>5</sup>*LJMU, UK*, <sup>6</sup>*U. Leuven, Belgium*
- 9:40 AM 12.4 - **The Piezoelectronic Transistor: a post-CMOS logic with high speed and low power**, G. J. Martyna and D. M. Newns, *IBM*
- 10:00 AM Coffee break

## Session 13 - Reliability

Session Chair: F. Martin

- 10:20 AM Opening remarks
- 10:25 AM 13.1 *Invited* - **Reliability challenges of high mobility channel technologies: SiGe, Ge and InGaAs**, J. Franco<sup>1</sup>, B. Kaczer<sup>1</sup>, Ph.J. Roussel<sup>1</sup>, M. Cho<sup>1</sup>, T. Grasser<sup>2</sup>, H. Arimura<sup>1</sup>, D. Cott<sup>1</sup>, J. Mitard<sup>1</sup>, L. Witters<sup>1</sup>, N. Waldron<sup>1</sup>, D. Zhou<sup>1</sup>, A. Alian<sup>1</sup>, A. Vais<sup>1</sup>, D. Lin<sup>1</sup>, K. Martens<sup>1</sup>, M. A. Pourghaderi<sup>1</sup>, S. Sioncke<sup>1</sup>, N. Collaert<sup>1</sup>, A. Thean<sup>1</sup>, M. Heyns, and G. Groeseneken<sup>3</sup>, <sup>1</sup>*imec, Belgium*, <sup>2</sup>*TU Wien, Austria*, <sup>3</sup>*U. Leuven, Belgium*
- 11:00 AM 13.2 *Invited* - **Evaluation of thermal properties of nanoscale MOSFETs and thermal aware device design of nano devices**, K. Uchida<sup>1,2</sup>, A. Shindome<sup>1</sup>, T. Takahashi<sup>1,2</sup>, T. Matsuki<sup>3</sup>, T. Shinada<sup>3</sup>, and Y. Inoue<sup>3</sup>, <sup>1</sup>*Keio U., Japan*, <sup>2</sup>*CREST, Japan*, <sup>3</sup>*AIST, Japan*
- 11:35 AM 13.3 - **Interface Friendly High-k Dielectrics for Sub-nm EOT Gate Stacks Formation on Germanium**, C. Lu<sup>1,2</sup>, C. H. Lee<sup>1,2</sup>, T. Nishimura<sup>1,2</sup>, and A. Toriumi<sup>1,2</sup>, <sup>1</sup>*U. Tokyo, Japan*, <sup>2</sup>*JST-CREST, Japan*
- 11:55 AM 13.4 - **Comparison of Al<sub>2</sub>O<sub>3</sub>/Si<sub>1-x</sub>Gex MOS interfaces grown on p-Si (100) and p-Si (110) with plasma post-nitridation**, J.-H. Han<sup>1,2</sup>, M. Takenaka<sup>1,2</sup>, and S. Takagi<sup>1,2</sup>, <sup>1</sup>*U. Tokyo, Japan*, <sup>2</sup>*JST-CREST, Japan*
- 12:15 PM 13.5 - **Direct Determination of Schottky Barrier Heights and Band Bending between Fe<sub>3</sub>Si and GaAs(100) by In-Situ XPS/UPS**, K. Y. Lin<sup>1</sup>, B. Z. Syu<sup>1</sup>, Y. H. Lin<sup>1</sup>, Z. J. Peng<sup>2</sup>, J. F. Lee<sup>2</sup>, C. H. Fu<sup>1</sup>, H. W. Wan<sup>1</sup>, C. P. Cheng<sup>3</sup>, T. W. Pi<sup>4</sup>, J. Kwo<sup>2</sup>, and M. Hong<sup>1</sup>, <sup>1</sup>*National Taiwan U., Taiwan*, <sup>2</sup>*National Tsing Hua U., Taiwan*, <sup>3</sup>*National Chiayi U., Taiwan*, <sup>4</sup>*National Synchrotron Radiation Research Center, Taiwan*
- 12:35 PM Closing remarks
- 12:40 PM Adjourn



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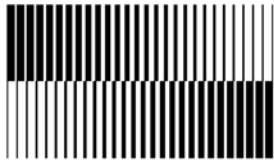
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TSMC, Belgium	4.4
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TU Brandenburg, Germany	1.1
TU Munich, Germany	1.1
TU Wien, Austria	13.1
Tyndall National Institute, Ireland	2.2
U. Antwerp, Belgium	11.14
U. Complutense de Madrid, Spain	2.8
U. Connecticut	11.13
U. di Milano, Italy	1.1
U. Gent, Belgium	11.4
U. Glasgow, UK	2.2
U. Hong Kong, Hong Kong	5.11
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