SISC 2015

46th IEEE Semiconductor Interface Specialists Conference

December 2-5, 2015
Key Bridge Marriott, Arlington, VA
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CONFERENCE PROGRAM

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Program Chair: Valeri Afanas'ev

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SISC Ed Nicollian Award for Best Student Paper

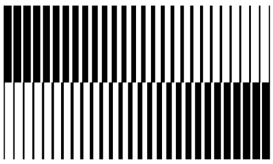
In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology," published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author for either an oral or a poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

Winner of the 2014 SISC Ed Nicollian Award for Best Student Paper:

Aaron Barton, *UT Dallas*

"$HfSe_2$ Thin Films: 2D Transition Metal Dichalcogenides Grown by MBE"
with R. Yue, S. McDonnell, R. Addou, A. Azcatl, H. Zhu, L. Ning, X. Peng, L. Colombo, J. Kim, M. Kim, R. M. Wallace, and C. L. Hinkle



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ELECTRON DEVICES SOCIETY

Wednesday Evening Tutorial

Wednesday, December 2, 2015, 8:00 PM

First introduced at SISC 2008, the Wednesday evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

Iuliana Radu

imec, Belgium

Spin logic options for Beyond or Along CMOS

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Conference Agenda Overview

Wednesday, December 2, 2015

Registration ..... 6:00 PM – 8:00 PM
Evening Tutorial ..... 8:00 PM – 9:30 PM
Hospitality Room ..... 9:30 PM – Midnight

Thursday, December 3, 2015

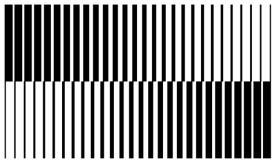
Registration ..... 8:00 AM – 5:00 PM
Session 1 – 2D-growth and Characterization ..... 8:00 AM – 10:10 AM
Session 2 – Two-Dimensional Transport and Interfaces ..... 10:30 AM – 12:05 PM
Session 3 – Poster Preview Session I– Ge and 2D Devices ..... 12:05 PM – 12:37 PM
Session 4 – Future Silicon and Si Compounds ..... 2:00 PM – 4:00 PM
Session 5 – Wide-gap Nitride Semiconductors ..... 4:20 PM – 6:15 PM
Session 6 – Poster Preview Session II– Wide Gap and Oxide Materials ..... 6:15 PM – 6:43 PM
Poster Session I ..... 7:00 PM – 10:00 PM
Hospitality Room ..... 10:00 PM – Midnight

Friday, December 4, 2015

Registration ..... 8:00 AM – Noon
Session 7 – AIII-BV Interfaces ..... 8:00 AM – 8:45 AM
Session 8 – Ge Interfaces ..... 8:45 AM – 10:20 PM
Session 9 – 2D Devices ..... 10:40 AM – 12:15 PM
Session 10 – Poster Preview Session III Defects and Reliability ..... 12:15 PM – 12:33 PM
Technical Committee / Invited Speaker Luncheon ..... 12:33 PM – 2:00 PM
Session 11 – Applications of Oxides ..... 2:00 PM – 3:40 PM
Session 12 – Poster Preview Session IV A_{III}-B_V and Memory Devices ..... 4:00 PM – 4:38 PM
Poster Session II ..... 4:50 PM – 6:50 PM
Conference Banquet and Limerick Contest ..... 7:00 PM – 10:00 PM
Hospitality Room ..... 10:00 PM – Midnight

Saturday, December 5, 2015

Session 13 – Towards Deep Scaling ..... 8:00 AM – 9:45 AM
Session 14 – Oxide Switching and Trapping ..... 10:05 AM – 11:40 AM
Session 15 – A_{III}-B_V Devices ..... 11:40 AM – 12:40 PM



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ELECTRON DEVICES SOCIETY

Conference Program

Wednesday, December 2, 2015

Tutorial

Session Chair: V. V. Afanas'ev

8:00 PM – 9:30 PM *Tutorial* - **Spin logic options for Beyond or Along CMOS,** I. Radu, *imec, Belgium*

9:30 PM – Midnight Hospitality Room

Thursday, December 3, 2015

8:00 AM Welcome and opening remarks

Session 1 – 2D-growth and Characterization

Session Chairs: P. D. Ye and I. Radu

8:10 AM Opening remarks

8:15 AM 1.1 *Invited* - **Monolayer Organic Films for Nucleation of ALD on Single Layer Graphene and TMD surfaces,** J. H. Park[1], I. Kwak[1], E. Chagarov[1], K. Sardashti[1], H. C. P. Movva[2], H. Chou[2], S. K. Banerjee[2], S. Fathipour[3], S. K. Fullerton-Shirey[3], A. Seabaugh[3], S. Vishwanath[4], H. G. Xing[4], P. Choudhury[5], and A. C. Kummel[1], *[1]UCSD, [2]UT Austin, [3]U. Notre Dame, [4]Cornell U., [5]New Mexico Tech*

8:50 AM 1.2 - **MBE growth of layered 2D semiconductor heterostructures: Transition metal dichalcogenides and topological insulators,** A. T. Barton[1], R. Yue[1], L. A. Walsh[1], H. Zhu[1], L. Cheng[1], N. Lu[1], R. Addou[1], S. McDonnell[1], J. W. P. Hsu[1], J. Kim[1], M. J. Kim[1], L. Colombo[2], R. M. Wallace[1], and C. L. Hinkle[1], *[1]UT Dallas, [2]Texas Instruments*

9:10 AM 1.3 - **Epitaxial 2D semiconductor / 2D metal v.d.Waals heterostructures,** D. Tsoutsou, K. E. Aretouli, J. Marquez-Velasco, P. Tsipas, E. Xenogiannopoulou, N. Kelaidis, and A. Dimoulas, *NCSR DEMOKRITOS, Greece*

9:30 AM 1.4 - **Paramagnetic defects in polycrystalline 2D MoS_2 films grown on SiO_2 by Mo sulfurization,** A. Stesmans[1], S. Iacovo[1], D. Chiappe[2], I. Radu[2], C. Huyghebaert[2], S. De Gendt[2], and V. V. Afanas'ev[1], *[1]U. Leuven, Belgium, [2]imec, Belgium*

9:50 AM 1.5 - **Atomic-layer deposited Al_2O_3 films on graphene sheets by non-aqueous ALD,** Y. Zhang[1], S. I. Shim[2], H. Li[1], R. Liu[1], and Z.-J. Qiu[1], *[1]Fudan U., China, [2]Samsung, Korea*

10:10 AM Coffee Break

Session 2 - Two-Dimensional Transport and Interfaces

Session Chair: A. Kummel

10:30 AM 2.1 *Invited* - **Physics of electronic transport in low-dimensionality materials for future FETs,** M. V. Fischetti, W. G. Vandenberghe, A. S. Negreira, Z.-Y. Ong, and B. Fu, *UT Dallas*

11:05 AM 2.2 - **Design of Band Offsets for Transition Metal Dichalcogenide Tunnel FET,** Y. Guo, and J. Robertson, *Cambridge U., UK*

11:25 AM 2.3 - **Schottky barrier height measurement for Pd metal on MoS_2 bulk by in situ XPS,** H. Dong[1],C. Gong[2], R. Addou[2],S. McDonnell[2], X. Qin[2], W. Wang[1], W. Wang[1], C. L. Hinkle[2], and R. M. Wallace[2], *[1]Nankai U., China, [2]UT Dallas*

11:45 AM 2.4 - **Surface States Engineering and Schottky Barrier Height Reduction in metal/MoS_2 contacts through Sulfur Treatment,** S. Bhattacharjee, K. L. Ganapathi, D. N. Nath, and N. Bhat, *IIS Bangalore, India*

Session 3 - Poster Preview Session I– Ge and 2D Devices

Session Chair: A. Demkov

12:05 PM Opening remarks

12:07 PM 3.1 - **Fabrication and Numerical Simulation for Eliminating Interfacial Layers from High-K/Metal Gates of Germanium MOS Device,** C.-L. Chu, J.-L. Chen, B.-Y. Chen, and G.-L. Luo, *[1]National Nano Device Laboratories, Taiwan, [2]I-Shou U., Taiwan*

12:09 PM 3.2 - **Platinum Effect in Post Deposition Annealing Performed on Ge/HfO_2/Pt Structures,** G. K. Rolim, G. V. Soares, and C. Radtke, *UFRGS, Brasil*

12:11 PM 3.3 - **Surface Passivation of Ge/GeSn/Ge Using Atomic Layer Deposited SiO_2 and Al_2O_3,** C.-Y. Lin[1], S.-H. Huang[1], C.-T. Lu[1], C. W. Liu[1],Y.-C. Huang[2], H. Chung[2], and C.-P. Chang[2], *[1]National Taiwan U., Taiwan, [2]Applied Materials*

12:13PM 3.4 - **Reduced Interface Trap Density by Al Capping on Al_2O_3 Stack on Ge,** C.-H. Huang, Y.-S. Huang, T.-Y. Lin, and C. W. Liu, *National Taiwan U., Taiwan*

12:15 PM 3.5 - **Nitride Passivation of the Interface between High-k Dielectrics and SiGe,** K. Sardashti[1], K.-T. Hu[1], A. C. Kummel[1], S. Madisetti[2], S. Oktyabrsky[2], S. Siddiqui[3], B. Sahu[3], N. Yoshida[4], and J. Kachian[4], *[1]UCSD, [2]SUNY, [3]GLOBALFOUNDRIES, [4]Applied Materials*

12:17 PM 3.6 - **Effect of ex-situ S-passivation on the quality of $Al_2O_3/Si_{0.3}Ge_{0.7}$(001) interfaces,** K. Sardashti[1], K.-T. Hu[1], A. C. Kummel[1], S. Madisetti[2], S. Oktyabrsky[2], S. Siddiqui[3], B. Sahu[3], N. Yoshida[4], and J. Kachian[4], *[1]UCSD, [2]SUNY, [3]GLOBALFOUNDRIES, [4]Applied Materials*

12:19 PM 3.7 - **Enhanced performance of Y-GeO_2/Ge Gate Dielectric by O_2 Post-deposition Annealing and Al Capping,** Y.-S. Huang, C.-H. Huang, C.-Y. Lin, and C. W. Liu, *National Taiwan U., Taiwan*

12:21 PM 3.8 - **Ge CMOS Devices: Performance and Variation Dependence on Operation Mode and Channel Thickness,** H. Wu, W. Wu, G. Qiu, and P. D. Ye, *Purdue U.*

12:23 PM 3.9 - **Electric field induced topological to trivial insulating phase transition in stanene,** M. Houssa[1], B. van den Broek[1], K. Iordanidou[1], A. Lu[1,2], G. Pourtois[2], V. V. Afanas'ev[1], and A. Stesmans[1], *[1]U. Leuven, Belgium, [2]imec, Belgium*

12:25 PM 3.10 - **Electronic properties of defective HfS_2 monolayers: A first-principles study,** K. Iordanidou[1], M. Houssa[1], G. Pourtois[2], V. V. Afanas'ev[1], A. Stesmans[1], *[1]U. Leuven, Belgium, [2]imec, Belgium*

12:27 PM 3.11 - **First-principles study of the performance degradation of 2D channel-based transistors with sub-10 nm gate lengths,** A. Lu[1,2], G. Pourtois[1], K. Stokbro[3], A. Thean[1], I. Radu[1], and M. Houssa[2], *[1]imec, Belgium, [2]U. Leuven, Belgium, [3]QuantumWise, Denmark*

12:29 PM 3.12 - **Fermi level of graphene under a metal contact modulated by high pressure hydrogen anneal,** Y. J. Kim, S. Y. Kim, U. Jung, S. K. Lee, K. E. Chang, C. Cho, and B. H. Lee, *GIST, Korea*

12:31 PM 3.13 - **The role of interface charge traps in the RF operation of graphene devices,** S. K. Lee, U. Jung, C. Cho, T. J. Yoo, A. N. R. Reza, H. I. Lee, and B. H. Lee, *GIST, Korea*

12:33 PM 3.14 - **Top-Gated, Few-Layer MoS_2 Field Effect Transistors with In-situ UV-Ozone Surface Functionalization and Sub-10nm HfO_2 Dielectric: Fabrication and Electrical Characterization,** P. Zhao[1], A. Azcatl[1], P. Bolshakov-Barrett[1], P. K. Hurley[2], R. M. Wallace[1], and C. D. Young[1], *[1]UT Dallas, [2]Tyndall National Institute, Ireland*

12:35 PM 3.15 - **Direct Atomic Layer Deposition of High-κ Dielectric Films on Graphene with Assistance of Pre-H_2O Treatment,** L. Zheng, X. Cheng, Y. Yu, D. Cao, Z. Wang, Q. Wang, and L. Shen, *Chinese Academy of Sciences, China*

12:37 PM Adjourn for Lunch

Session 4 – Future Silicon and Si Compounds

Session Chairs: P. Lenahan and K. Kita

2:00 PM Opening remarks

2:05 PM 4.1 *Invited* - **Silicon at the two-dimensional limit: the debut of the silicene transistor,** A. Molle, *CNR-IMM, Italy*

2:40 PM 4.2 - **Investigation of ternary SiGeSn MOS structures,** C. Schulte-Braucks[1], T. Lehndorff[1], S. Glass[1], N. von den Driesch[1], S. Wirths[1], J.M. Hartmann[2,3], Z. Ikonic[4], S. Mantl[1], and D. Buca[1], *[1]Forschungszentrum Jülich, Germany, [2]U. Grenoble Alpes, France, [3]CEA-LETI, France, [4]U. Leeds, UK*

3:00 PM 4.3 - **Passivation and Functionalization of SiGe(001) and (110) using atomic hydrogen, H_2O_2, TMA Dosing for high-k ALD Nucleation,** S. W. Park[1], H. Kim[1], S. Wolf[1], E. Chagarov[1], S. Siddiqui[2], B. Sahu[2], N. Yoshida[3], J. Kachian[3], and A. C. Kummel[1], *[1]UCSD, [2]GLOBALFOUNDRIES, [3]Applied Materials*

3:20 PM 4.4 - **SiO_2/SiC Interface Nitridation by High Temperature Pure Nitrogen Annealing,** T. Hosoi, A. Chanthaphan, T. Shimura, and H. Watanabe, *Osaka U., Japan*

3:40 PM 4.5 - **Surface Carrier Density Dependence of Hall Mobility in SiC MOS Inversion Layer,** M. Noguchi[1], T. Iwamatsu[1], H. Amishiro[1], H. Watanabe[1], S. Nakata[1], T. Kuroiwa[1],K. Kita[2], and S. Yamakawa[1], *[1]Mitsubishi Electric, Japan, [2]U. Tokyo, Japan*

4:00 PM Coffee Break

Session 5 – Wide-gap Nitride Semiconductors

Session Chairs: J. Robertson and M. Kuzuhara

4:20 PM 5.1 *Invited* - **GaN-based HEMTs for High-voltage and Low-loss Power Applications,** M. Kuzuhara, J. T. Asubar, and H. Tokuda, *U. Fukui, Japan*

4:55 PM 5.2 - **Effect of Nitrogen Incorporation into Al-based Gate Insulator in AlGaN/GaN MOS-HEMT,** R. Asahara[1], M. Nozaki[1], T. Yamada[1], J. Ito[1], S. Nakazawa[2], M. Ishida[2], T. Ueda[2], A. Yoshigoe[3], T. Hosoi[1], T. Shimura[1], and H. Watanabe[1], *[1]Osaka U., Japan, [2]Panasonic, Japan, [3]Japan Atomic Energy Agency, Japan*

5:15 PM 5.3 - **The role of electron transport in the charge trapping at the III-N/dielectric interface in AlGaN/GaN MIS-HEMT structures,** C. Ostermaier[1], P. Lagger[1], G. Prechtl[1], A. Grill[2], T. Grasser[2], and D. Pogany[2], *[1]Infineon, Austria, [2]TU Vienna, Austria*

5:35 PM 5.4 - **Ultra-low Leakage and High-breakdown AlGaN/GaN MOSHEMTs on Si Substrate Enabled by Epitaxial MgCaO Gate Dielectric,** H. Zhou[1], X. Lou[2], K. D. Chabak[3], R. G. Gordon[2], and P. D. Ye[1], *[1]Purdue U., [2]Harvard U., [3]Air Force Research Laboratory*

5:55 PM 5.5 - **Plasma Enhanced Atomic Layer Deposition Half Cycle Study of Al_2O_3 on AlGaN/GaN High Electron Mobility Transistors,** X. Qin and R. M. Wallace, *UT Dallas*

Session 6 - Poster Preview Session II– Wide Gap and Oxide Materials

Session Chair: M. Baklanov

6:15 PM 6.1 - **Errors Due to Nonlinear and Energy-Dependent Phenomena in the MOS Conductance Technique,** S. Swandono, D. Morisette, and J. A. Cooper, *Purdue U.*

6:17 PM 6.2 - **Effects of High-k Passivation-Layer on Breakdown Voltage in AlGaN/GaN HEMTs,** H. Hanawa, Y. Satoh, and K. Horio, *Shibaura Institute of Technology, Japan*

6:19 PM 6.3 - **Localized VLS Epitaxy Process as a P-type Doping Alternative Technique for 4H-SiC P/N Junctions,** S. Sejil[1,2], M. Lazar[2], D. Carole[1], C. Brylinski[1], D. Planson[2], G. Ferro [1], and C. Raynaud [2], *[1]U. Lyon 1, France, [2]Ecole Centrale de Lyon, France*

6:21 PM 6.4 - **Study of interface states in AlGaN/GaN MIS-HEMTs with HfO_2 fabricated by atomic layer deposition,** T. Kubo, G. Nishino, and T. Egawa, *Nagoya Institute of Technology, Japan*

6:23 PM 6.5 - **Effect of GaN channel thickness on the performance of AlGaN/GaN HEMT,** S.-J. Chang[1], M. Bhuiyan[1], H.-S. Kang[2], J.-H. Lee[3] , Y.-W. Jo[2], S. Cui[1], J.-H. Lee[2], and T.P. Ma[1], *[1]Yale U., [2]Kyungpook National U., Korea, [3]Samsung, Korea*

6:25 PM 6.6 - **Nitrogen Incorporation into Al_2O_3 as a Source of Negative Fixed Charges: A Path to Enhancement Mode GaN Device Operation,** M. A. Negara, R. D. Long, and P. C. McIntyre, *Stanford U.*

6:27 PM 6.7 - **Reliability of Electrically Degraded GaN/AlGaN/GaN/ Si High Electron Mobility Transistors and Role of Surface Oxide Particles,** S. Ghosh, S. Das, P. Mukhopadhyay, S. M. Dinara, and D.Biswas, *IIT Kharagpur, India*

6:29 PM 6.8 - **Formation of nanoscale $BaTiO_3$ MOSCAPs without wet-etching,** P. Ponath[1], A. B. Posadas[1], M. Schmidt[2], P. K. Hurley[2], R. Duffy[2], and A. A. Demkov[1], *[1]UT Austin, [2]Tyndall National Institute, Ireland*

6:31 PM 6.9 - **Impact of Template Residues on Electrical Properties of Spin-on Ultra Low-k Dielectrics,** M. Krishtab[1,2], V. V. Afanas'ev[2], A. Stesmans[2], S. De Gendt[1,2], and M. R. Baklanov[1], *[1]imec, Belgium, [2]U. Leuven, Belgium*

6:33 PM 6.10 - **Effects of top TiN deposition process on electrical and physical properties of ferroelectric HfSiO MIM capacitor,** Y. Kamimuta, S. Fujii, R. Takaishi, T. Ino, Y. Nakasaki, M. Saitoh, and M. Koyama, *Toshiba Corporation, Japan*

6:35 PM 6.11 - **Self-limiting Oxygen Vacancy formation into Anatase-TiO_2 Films by Trimethylaluminium,** I. Yamamoto[1,2], T. Nabatame[2,3], T. Sawada[2,3], A. Ohi[2], K. Kurishima[4], D. D. Thang[2,3], T. Nagao[2,3], T. Chikyo[2], A. Ogura[4], and T. Ohishi[1], *[1]Shibaura Institute of Technology, Japan, [2]NIMS, Japan, [3]CREST, Japan, [4]Meiji U., Japan*

6:37 PM 6.12 - **Electrical Characteristics of 4H-SiC Metal Insulator Semiconductor Structures with Different Dielectrics for MESFET Applications,** M. Hema Lata Rao and N. V. L. Narasimha Murty, *IIT Bhubaneswar, India*

6:39 PM 6.13 - **The electronic structures of TiO_2/Ti_4O_7, Ta_2O_5/TaO_2 interfaces and the interfacial effects of dopants,** H. Li, Z. Zhang, and L. Shi, *Tsinghua U., China*

6:41 PM 6.14 - **Electron blocking by AlInN back barrier in GaN HEMT,** X. G. He[1] and D. G. Zhao[2], *Chinese Academy of Sciences, China*

6:43 PM Adjourn

Poster Session I

Session Chairs: C. Hinkle and V. V. Afanas'ev

7:00 PM – 10:00 PM Poster Session I

10:00 PM – Midnight Hospitality Room

Friday, December 4, 2015

8:00 AM Morning announcement and opening remarks

Session 7 – A_{III}-B_V Interfaces

Session Chair: A. Molle

8:05 AM 7.1 - **Border trap reduction in Al_2O_3/InGaAs gate stacks by low temperature atomic layer deposition of the dielectric,** K. Tang[1], R. Winter[2], R. Droopad[3], M. Eizenberg[2], and P. C. McIntyre[1], *[1]Stanford U., [2]Technion, Israel, [3]Texas State U.*

8:25 AM 7.2 - **Improvement of Electrical Characteristics of La_2O_3/InGaAs Gate Stacks by Ultra-thin ALD Al_2O_3 Capping Layers,** C.-Y. Chang[1,2], M. Takenaka[1,2], and S. Takagi[1,2], *[1]U. Tokyo, Japan, [2]JST-CREST, Japan*

Session 8 – Ge Interfaces

Session Chair: CheeWee Liu

8:45 AM 8.1 *Invited* - **Materials and Process Controls in Germanium Gate Stacks,** A. Toriumi, *U. Tokyo, Japan*

9:20 AM 8.2 - **Properties of slow traps of ALD Al_2O_3/GeOx/Ge gate stacks with plasma post oxidation,** M. Ke[1,2], X. Yu[1,2], M. Takenaka[1,2], and S. Takagi[1,2], *[1]U. Tokyo, Japan, [2]JST-CREST, Japan*

9:40 AM 8.3 - **High Mobility at Ultralow EOT in Ge pMOSFET by Hf-rich Buffer Layer and Microwave Annealing,** C.-C. Li[1], K.-S. Chang-Liao[1], T.-M. Lee[1], M.-C. Li[1], W.-F. Chi[1], T.-C. Chen[1], T.-H. Su[1], Y.-W. Chang[1], C.-C. Tsai[1], Y.-L. Li[1], L.-J. Liu[1], C.-H. Fu[1], C.-C. Lu[1], and Y.-J. Lee[2], *[1]National Tsing Hua U., Taiwan, [2]National Nano Device Laboratories, Taiwan*

10:00 AM 8.4 - **Back Gate Bias induced Carrier Mobility Enhancement in Ge-on-insulator MOSFETs,** W. Wu[1,2,3], H. Wu[3], J. Zhang[3], M. Si[3], Y. Zhao[1,2], and P. D. Ye[3], *[1]Nanjing U., China, [2]Zhejiang U., China, [3]Purdue U.*

10:20 PM Coffee Break

Session 9 – 2D Devices

Session Chair: M. Fischetti

10:40 AM 9.1 *Invited* - **Two-dimensional Layered Materials and Nano-scale Devices,** W. Zhu, *UIUC*

11:15 AM 9.2 - **Gate tunable high photo responsivity due to the unique photo carrier transfer mechanism at graphene/Si interface,** K. E. Chang, U. Jung, T. J. Yoo, H. J. Hwang, W. B. Yoo, Y. J. Kim, S. K. Lee, and B. H. Lee, *GIST, Korea*

11:35 AM 9.3 - **Graphene barristor with nitrogen doped ZnO for high on/off ratio and wide barrier height modulation,** H. J. Hwang, W. B. Yoo, K. E. Chang, C. H. Shim, C. Cho, J. H. Yang, Y. J. Kim, S. K. Lim, W. Park, and B. H. Lee, *GIST, Korea*

11:55 AM 9.4 - **Low frequency noise in high performance ambipolar few-layer BP transistors,** X. Li, *Huazhong U. Science and Technology, China*

Session 10 – Poster Preview Session III Defects and Reliability

Session Chair: P. Blaise

12:15 PM 10.1 - **Ab-initio Simulation on Higher Miller Index Si:SiO_2 Interface for Application in FinFET,** H. Li, Y. Guo, and J. Robertson, *U. Cambridge, UK*

12:17 PM 10.2 - **Interface Trap Density Extraction of Ultra-scaled MOSFETs,** M. Si, J. J. Gu, J. Zhang, and P. D. Ye, *Purdue U.*

12:19 PM 10.3 - **Mechanism of subthreshold swing degradation in p-type tunnel FETs,** U. Jung[1], S. M. Kim[1], D. Lim[2], K. E. Chang[1], Y. J. Kim[1], S. C. Kang[1], S. K. Lim[1], C. Choi[2], and B. H. Lee[1], *[1]GIST, Korea, [2]Hanyang U., Korea*

12:21 PM 10.4 - **Al_2O_3 Deposition by Ultrasonic Spray Pyrolysis Technique for Non-planar MOS Devices,** J.-H. Wang[1], J.-L. Lai[1], P.-A. Chen[1], M.-H. Chiang[1], W.-C. Hsu[1], W.-C. Sun[2], and S.-Y. Wei[2], *[1]National Cheng Kung U., Taiwan, [2]Industrial Technology Research Institute, Taiwan*

12:23 PM 10.5 - **Atomic Layer Deposited Alumina-Silicon Interfaces: Effects of Non-Hydrolytic Chemistries,** R. Marstell and N. C. Strandwitz, *Lehigh U.*

12:25 PM 10.6 - **Understanding of oxygen diffusion at the SiO_2/Si interface by combining Activation Relaxation Technique to first principles calculations,** N. Salles[1,2], A. Hémeryck[1,2], N. Mousseau[3], A. Estève[1,2], M. Djafari Rouhani[1,2] and N. Richard[4], *[1]CNRS, France, [2]U. Toulouse, France, [3]U. Montréal, Canada, [4]CEA, France*

12:27 PM 10.7 - **Quantitative detection of sub-surface nano-scale defects in semiconductor wafers via terahertz scanning reflectometry and imaging,** A. Rahman, S. Bass, and A. K. Rahman, *Applied Research & Photonics*

12:29 PM 10.8 - **Response of Nano-Scaled Oxide Film Thickness of p-channel MOSFET on the Low Absorbed Doses and Low Absorbed Dose Rates,** M. Pejovic[1], K. Stankovic[2], I. Fetahovic[3], and P. Osmokrovic[3], *[1]U. Nis, Serbia, [2]U. Belgrade, Serbia, [3]State U. Novi Pazar, Serbia*

12:31 PM 10.9 - **Defect-assisted GIDL reduction and Performance Analysis of SiGe channel pFET without Ge Pre-amorphization implant for scaled supply voltages,** V. A. Tiwari[1], R. Divakaruni[2], T. Hook[2], D. R. Nair[1], *[1]IIT Madras, India, [2]IBM*

12:33 PM – 2:00 PM Committee / Invited Speaker Luncheon

Session 11 – Applications of Oxides

Session Chairs: C. Dubourdieu and B. Magyari-Kope

2:00 PM Opening Remarks

2:05 PM 11.1 *Invited* - **Ultra low-k insulating materials for advanced nanoelectronics,** M. R. Baklanov, *imec, Belgium*

2:40 PM 11.2 - **Conductance and Capacitance of Bilayer Protective Oxides for Silicon Water Splitting Anodes,** A. G. Scheuermann[1], K. W. Kemp[1], K. Tang[1], P. F. Satterthwaite[1], D. Q. Lu[1], T. Ito[1,2], C. E. D. Chidsey[1], and P. C. McIntyre[1], *[1]Stanford U., [2]Tokyo Electron*

3:00 PM 11.3 - **Electrical Characterization of Epitaxial $SrTiO_3$ (STO) on Si by Inelastic Electron Tunneling Spectroscopy (IETS) and Temperature Dependent I-V Measurements,** S. Ren[1], M. Bhuiyan[1], J. Yang[1], S. Chang[1], K. S. Chang-Liao[2], and T.P. Ma[1], *[1]Yale U., [2]National Tsing Hua U., Taiwan*

3:20 PM 11.4 - **Electro-optically active barium titanate thin films on Si,** K. J. Kormondy[1], S. Abel[2], Y. Popoff[2], D. Caimi[2], C. Marchiori[2], M. Sousa[2], M. D. Rossell[3], A. A. Demkov[1], J. Fompeyrine[2], *[1]UT Austin, [2]IBM, Switzerland, [3]Swiss Federal Laboratories for Materials Science and Technology, Switzerland*

3:40 PM 11.5 - **Study of C-doped InSiO as a novel channel material for oxide TFT,** K. Kurishima[1, 2], T. Nabatame[2], N. Mitoma[2], T. Kizu[2], K. Tsukagoshi[2], T. Sawada[2], A. Ohi[2], I. Yamamoto[2, 3], T. Ohishi[3], T. Chikyo[2], and A. Ogura[1], *[1]Meiji U., Japan, [2]NIMS, Japan, [3]Shibaura Institute of Technology, Japan*

Session 12 - Poster Preview Session IV A_{III}-B_V and Memory Devices

Session Chair: M. Frank

4:00 PM 12.1 - **Effect of surface treatments in InGaAs MOS capacitors fabrication analyzed by DLTS,** G. Chicot [1], P. Ferrandis [1,2], J. Duvernay [1], M. Casse [1], M. Billaud [1], H. Boutry [1], M. Martin [3], T. Baron [3], M. Vinet [1], G. Reimbold [1], *[1]CEA-LETI, France, [2]U. Toulon IM2NP, France, [3]U. Grenoble Alpes LTM, France*

4:02 PM 12.2 - **Total Ionizing Dose Effects on GaAs MOSFETs with Epitaxial High-k Gate Dielectrics,** S. Ren[1], J. Zhang[2], M. Si[2], K. Ni[3], X. Wan[1], J. Chen[3], X. Sun[1], E. X. Zhang[3], D. M. Fleetwood[3], P. D. Ye[2], S. Cui[1], and T. P. Ma[1], *[1]Yale U., [2]Purdue U., [3]Vanderbilt U.*

4:04 PM 12.3 - **InAs-Oxide Interfaces upon Thermal Oxidation and High-k ALD Investigated by XPS,** A. Troian, J. Knutsson, A. S. Babadi, L.-E. Wernersson, A. Mikkelsen, and R. Timm, *Lund U., Sweden*

4:06 PM 12.4 - **Interfacial electronic structure of the noble metals on α2-GaAs(001)-2x4 surface: Atom-to-atom interaction and the Schottky barrier height,** W. S. Chen[1], C. P. Cheng[2], G. J. Wei[2], Y. T. Cheng[2], C. H. Wei[1], Y. C. Lin[1], Y. H. Lin[3], K. Y. Lin[3], T. W. Pi[1], J. Kwo[4], and M. Hong[3], *[1]National Synchrotron Radiation Research Center, Taiwan, [2]National Chiayi U., Taiwan, [3]National Taiwan U., Taiwan, [4]National Tsing Hua U., Taiwan*

4:08 PM 12.5 - **First demonstration of cluster tool based ICP etching of (100) and (110) InGaAs MOSCAPs followed by in-situ ALD deposition of HfO_2 including nitrogen and hydrogen plasma passivation for non-planar III-V MOSFETs,** Y.-C. Fu[1], U. Peralagu[1], X. Li[1], D. Millar[1],O. Ignatova[1],H. Zhou[1],M. Steer[1],R. Droopad[2], and I. Thayne[1], *[1]U. Glasgow, UK, [2]Texas State U.*

4:10 PM 12.6 - **The formation of inverse InGaAs/HfO_2 interfaces via epitaxial lateral overgrowth,** P. Tejedor and M. Benedicto, *ICMM, Spain*

4:12 PM 12.7 - **Surface passivation and functionalization of $In_{0.53}Ga_{0.47}As$(001)-(2x4) and $Si_{0.5}Ge_{0.5}$(110) surfaces by silicon containing control layers,** M. Edmonds[1], T. J. Kent[1], S. Wolf[1], M. Chang[2], J. Kachian[2], R. Droopad[3], E. Chagarov[1], and A. C. Kummel[1], *[1]UCSD, [2]Applied Materials, [3]Texas State U.*

4:14 PM 12.8 - **Fluorine Functionalization Prior to Al_2O_3 ALD Passivation of Etched InAs Surfaces,** E. R. Cleveland, J. A. Nolde, C. Affouda, and E. Aifer, *Naval Research Laboratory*

4:16 PM 12.9 - **Al oxy-nitride for higher Reliability high K gate stacks on Ge and III-Vs,** Y. Guo and J. Robertson, *Cambridge U., UK*

4:18 PM 12.10 - **Interfacial electronic structure of aluminum on GaAs(001)-4x6: Re-examination of the interface with ALD tri-methylaluminum and water,** T. W. Pi[1], C. P. Cheng[2], Y. T. Cheng[2], W. S. Chen[1], S. Wang[2], G. J. Wei[2], C. H. Wei[1], Y. C. Lin[1], Y. H. Chang[3], Y. H. Lin[3], J. Kwo[4], and M. Hong[3], *[1]National Synchrotron Radiation Research Center, Taiwan, [2]National Chiayi U., Taiwan, [3]National Taiwan U., Taiwan, [4]National Tsing Hua U., Taiwan*

4:20 PM 12.11 - **Electrical Properties of ZrO_2/InAs MOSCAPs,** A. S. Babadi, E. Lind, and L.-E. Wernersson, *Lund U., Sweden*

4:22 PM 12.12 - **Enhanced ALD-Y_2O_3 Thin Film Quality and Interface Cleansing Achieved by UHV Annealing for III-V Passivation,** K. Y. Lin[1], Y. H. Lin[1], K. H. Chen[1], L. B. Young[1], C. H. Fu[1], C. P. Cheng[2], T. W. Pi[3], J. Kwo[4], and M. Hong[1], *[1]National Taiwan U., Taiwan, [2]National Chiayi U., Taiwan, [3]National Synchrotron Radiation Research Center, Taiwan, [4]National Tsing Hua U., Taiwan*

4:24 PM 12.13 - **Negative Differential Resistance due to Real Space Transfer of Hot Electrons in $In_{0.53}Ga_{0.47}As$ Channel MOS-HEMTs,** A. S. Yadav, K. H. Goh, X. Gong, and Y.-C. Yeo, *National U. Singapore, Singapore*

4:26 PM 12.14 - **First principles examination of the switching mechanism of the phase change memory (TRAM) using superlattice GeTe/Sb_2Tb_3,** M. Takato, H. Shirakawa, M. Araidai, and K. Shiraishi, *Nagoya U., Japan*

4:28 PM 12.15 - **Oxide Stress Separation technique for the assessment of Inter-Gate Dielectric integrity in 40 nm Flash memory cells,** A. Dobri[1,2,3], S. Jeannot[1], F. Piazza[1], C. Jahan[2], J. Coignus[2], L. Perniola[2], and F. Balestra[3], *[1]STMicroelectronics, France, [2]CEA-LETI, France, [3]IMEP-LAHC, France*

4:30 PM 12.16 - **Multi-State Sub-9 nm QDC-SWS FETs for Compact Memory Circuits,** F. Jain[1], M. Lingalugari[1], B. Saman[1], P.-Y. Chan [1], P. Gogna[1], E.-S. Hasaneen[1], J. Chandy[1], and E. Heller[2], *[1]UCONN, [2]Synopsys*

4:32 PM 12.17 - **Investigation of the Ion Exchanges between Al_2O_3 and CuTe for Hybrid RRAM,** C. Nail[1], P. Blaise[1], G. Molas[1], M. Bernard[1], A. Roule[1], A. Toffoli[1], C. Vallée[2], and L. Perniola[1], *[1]CEA-LETI, France, [2]CNRS LTM, France*

4:34 PM 12.18 - **Unified Kinetic Monte Carlo simulation of Forming, SET, RESET and data retention for Conductive Bridge RAM, a bond between material properties and device behavior.,** J. Guy, G. Molas, and L. Perniola, *CEA-LETI, France*

4:36 PM 12.19 - **FET transconductance as a probe of ferroelectric/semiconductor interface,** A.Hanna, M. Ghoneim, and M. M. Hussain, *King Abdullah U., Saudi Arabia*

4:38 PM Adjourn

Poster Session II

Session Chairs: C. Hinkle and V. V. Afanas'ev

4:50 PM – 6:50 PM Poster Session II

7:00 PM – 10:00 PM Conference Banquet and Limerick Contest

10:00 PM – Midnight Hospitality Room

Saturday, December 5, 2015

8:00 AM Morning announcements

Session 13 – Towards Deep Scaling

Session Chair: Wenjuan Zhu

8:05 AM 13.1 - **At 10nm node, what is the AC impact of dielectric insertions in contact initially meant to decrease the DC contact resistivity?,** J. Borrel[1, 2, 3], L. Hutin[2], O. Rozeau[2], M.-A. Jaud[2], S. Martinie[2], E. Dubois[3], and M. Vinet[2], *[1]STMicroelectronics, France, [2]CEA-LETI, France, [3]IEMN, France*

8:25 AM 13.2 - **Deciphering Reliability in High-K Metal Gate Technology,** M. Drescher[1], E. Erben[2], C. Grass[2], M. Trentzsch[2], F. Lazarevic[3], R. Leitsmann[3], P. Plänitz[3], T. Mtchedlidze[4], K. Seidel[1], and R. Liske[1], *[1]Fraunhofer, Germany, [2]GLOBALFOUNDRIES, Germany, [3]AQcomputare, Germany, [4]TU Dresden, Germany*

8:45 AM 13.3 - **Comprehensive Defect Spectroscopy and Multi-Frequency Charge Pumping Study of HKMG Transistors,** J. Ocker[1], M. Hoffmann[1], M. Drescher[2], T. Mtchedlidze[3], F. Lazarevic[4], R. Leitsmann[4], S. Slesazeck[1], E. Erben[5], and T. Mikolajick[3], *[1]NaMLab, Germany, [2]Fraunhofer, Germany, [3]TU Dresden, Germany, [4]AQcomputare, Germany, [5]GLOBALFOUNDRIES, Germany*

9:05 AM 13.4 - **Distribution of the energy levels of single interface traps in nanoscale MOSFETs and a comparison of the actual number of traps with the values determined by conventional charge pumping theory,** T. Tsuchiya, *Shimane U., Japan*

9:25 AM 13.5 - **Influence of Low Thermal Budget Processing and Post-Processing on Performance and Reliability of HfO_2/TiN Gate-First for 3D VLSI Integration,** C.-M. V. Lu[1,2], R. Gassilloud[1], C. Fenouillet-Beranger[1], C. Leroux[1], X. Garros[1], A. Toffoli[1], N. Rambal[1], V. Lapras[1], J.-M. Pedini[1], M.-P. Samson[1], B. Previtali[1], N. Bernier[1], G. Audoit[1], V. Delaye[1], L. Brunet[1], P. Batude[1], T.Skotnicki[2], and M. Vinet[1], *[1]CEA-LETI, France, [2]STMicroelectronics, France*

9:45 AM Coffee Break

Session 14 – Oxide Switching and Trapping

Session Chairs: J. Robertson and A. Toriumi

10:05 AM 14.1 *Invited* - **Microscopic Aspects of Conductive Filaments Evolution in Metal Oxide RRAM devices,** B. Magyari-Köpe and Y. Nishi, *Stanford U.*

10:40 AM 14.2 - **Impact of ALD process parameters on HfO_2 based 1T-1R RRAM inter-cell variability and switching properties,** A. Grossi[1], E. Perez[2], C. Zambelli[1], P. Olivo[1], R. Roelofs[3], and C. Wenger[2], *[1]U. Ferrara, Italy, [2]IHP, Germany, [3]ASM, Belgium*

11:00 AM 14.3 - **Ferroelectricity of Al-doped HfO_2: Fast Polarization Switching, Long Retention and Robust Endurance,** N. Gong[1], X. Sun[1], H. Jiang[2], Q. Xia[2], T. P. Ma[1,3], *[1]Yale U., [2]U. Massachusetts, [3]Alacrity Semiconductors*

11:20 AM 14.4 - **The role of single oxygen or metal induced defect and correlated multiple defects in the formation of conducting filaments,** H. Li, Z. Zhang, and L. Shi, *Tsinghua U., China*

Session 15 – A_{III}-B_V Devices

Session Chair: M. Passlack

11:40 AM 15.1 - **Analysis of Switching Performance of III-V Hetero-junction Tunnel FETs,** R. Pandey and S. Datta, *Penn State U.*

12:00 PM 15.2 - **InGaAs Bulk FinFET with Vertical Sidewalls,** J. Zhang, M. Si, W. Wu, and P. D. Ye, *Purdue U.*

12:20 PM 15.3 - **Fin Width Effect on the Performance of InGaAs-based Independent Double-Gate Transistors,** S.-J. Chang[1], H. Zhou[2], N. Gong[1], M. Si[2], P. D. Ye[2], and T. P. Ma[1], *[1]Yale U., [2]Purdue U.*

12:40 PM Closing remarks and adjourn

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