SISC 2018

49th IEEE Semiconductor Interface Specialists Conference

December 5-8, 2018
Catamaran Resort Hotel, San Diego, CA
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SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology," published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author for either an oral or a poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

Winner of the 2017 SISC Ed Nicollian Award for Best Student Paper:

Mahmut Sami Kavrik

UCSD

"Ultra-Low Defect Density sub 0.5 nm HfO_2/SiGe Interface Formation via Al Gettering Gate"
with E. Thomson, E. Chagarov, A. Betts, K. Tang, P. C. McIntyre, Q. Wang, M. Kim,
and A. C. Kummel

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Wednesday Evening Tutorial

Wednesday, December 5, 2018, 8:00 PM

First introduced at SISC 2008, the Wednesday evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

Prof. Philippe Vereecken, *U. Leuven and imec*

Solid-state batteries—a story about interfaces

Lithium ion batteries (LIB) dominate the portable electronics market and are the battery technology of choice for hybrid and plug-in electrical vehicles. Lithium ion battery packs have also made their debut for local storage in homes. Currently, the electric vehicle market is the main driver for advancement in LIB technology. Yet, rechargeable batteries in different forms will be a key component and enabler for many future technologies, ranging from small wireless autonomous sensors for the internet of things to storage of renewable energy in the smart grid.

Battery R&D is typically focused on material innovation; i.e. the search for novel cathode and anode chemistries, improvements in design through nanotechnology and optimization of the liquid electrolyte chemistry. However, battery issues such as limited lifetime and charging rates are primarily related to poorly controlled interfaces and to the use of liquid electrolytes. Solid electrolytes are being explored to replace the flammable liquid electrolyte. Next to solving the issues with safety, the transition to a solid-state electrolyte would mean significant improvements in the battery performance as well: higher energy density, longer battery life time and wider temperature range of operation. The solid-state concept allows direct integration of the battery with microsystems such as sensors or implants. For these micro-batteries, CMOS materials and processing can be (re)used. However, ideas for innovation in large scale battery technology can also come from the IC industry, where the downscaling of the transistor has driven tremendous research efforts into new materials and the understanding of charge transport and interfaces. For example, in CMOS technology interfaces are controlled at the atomic scale in contrast to the sometimes micron thick interfacial layers which exist in batteries due to decomposition of electrode and liquid electrolyte.

In this tutorial, we will first introduce the main drivers to go solid-state and the projected roadmaps for the introduction of these next generation Li-ion batteries in electric vehicles. We will review the different solid-state battery contenders in the race and differentiate between thin-film micro-batteries and large capacity particle-composite batteries. Thin-film solid-state batteries have been available already commercially for some time as solid electrolyte materials with ionic conductivities in the order of micro-Siemens are sufficient for the short distance across the sub-micrometer thin-films. For large capacity batteries, however, where the distance between the current collectors can be several hundreds of microns, materials with ion conductivities in the range of milli-Siemens are required instead. Solid electrolytes with such high ion conductivities have been discovered only very recently and work on integration of these electrolytes in solid-state cells is currently ongoing. Some of the integration routes, their issues and needed material solutions will be discussed. The use of thin-film coatings and interface engineering will be highlighted. At imec, we are using a thin-film platform to investigate and engineer solutions for interface related issues. We are developing solid nanocomposite electrolytes where the ion conductivity is tailored through interface conduction. Diffusion of ions along interfaces is a phenomenon that leads to reliability issues in chip interconnects but helps us to engineer novel electrolyte materials. Finally, we will look at examples where the solid-state and thin-film know-how is transferred to particle-based systems for large capacity cells.

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Conference Agenda Overview

Wednesday, December 5, 2018

Registration ..... 6:00 PM – 8:00 PM
Evening tutorial ..... 8:00 PM – 9:30 PM
Hospitality room ..... 9:30 PM – 12:00 AM

Thursday, December 6, 2018

Registration ..... 8:00 AM – 5:00 PM
Keynote ..... 8:00 AM – 8:45 AM
Session 1: Interfaces and Materials for High Performance Devices ..... 8:45 AM – 10:00 AM
Session 2: Atomic Layer Deposition & Selective Processes ..... 10:20 AM – 12:10 PM
Session 3: Poster Preview Session I – High-k Dielectrics and High Mobility Channels ..... 1:30 PM – 2:05 PM
Session 4: Ferroelectrics I: FETs and NC ..... 2:05 PM – 3:40 PM
Session 5: Poster Preview Session II: Interfaces, Materials and Devices ..... 4:05 PM – 5:15 PM
Poster Session 1 & Reception ..... 7:00 PM – 10:00 PM
Hospitality room ..... 10:00 PM – 12:00 AM

Friday, December 7, 2018

Registration ..... 8:00 AM – 12:00 PM
Session 6: 2D Transition Metal Dichalcogenides ..... 8:00 AM – 9:40 AM
Session 7: Poster Preview Session III: 2D Materials and Ferroelectrics ..... 9:40 AM – 10:15 AM
Session 8: Low-D Semiconductors & Novel FETs ..... 10:40 AM – 12:00 PM
Committee / Invited Speaker luncheon ..... 12:00 PM – 1:30 PM
Session 9: SiGe and Ge MOS ..... 1:30 PM – 3:15 PM
Poster Session 2 & Coffee break ..... 3:15 PM – 4:45 PM
Session 10: Ferroelectrics II, Materials and Devices ..... 4:45 PM – 6:05 PM
Conference banquet and Limerick contest ..... 7:00 PM – 10:00 PM
Hospitality room ..... 10:00 PM – 12:00 AM

Saturday, December 8, 2018

Session 11: Interfaces in Solar and Optoelectronic Devices ..... 8:00 AM – 9:55 AM
Session 12: Wide Band-Gap Semiconductors ..... 10:20 AM – 12:00 PM
Session 13: Memory ..... 1:30 PM – 3:15 PM

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Conference Program

Wednesday, December 5, 2018

Tutorial

Session Chair: P. C. McIntyre

8:00 PM – 9:30 PM *Tutorial* - **Solid State Batteries,** P. Vereecken[1,2], [1]*U. Leuven, Belgium,* [2]*imec, Belgium*

9:30 PM – 12:00 AM Hospitality room

Thursday, December 6, 2018

8:00 AM Welcome and opening remarks

8:10 AM *Keynote* - **Interfaces for CMOS bioelectronics,** K. Shepard, *Columbia U.*

Session 1: Interfaces and Materials for High Performance Devices

Session Chair: M. Passlack

8:45 AM 1.1 *Invited* - **Future Scaling of Advanced Logic Devices,** H. Bu, *IBM*

9:20 AM 1.2 - **$GdAlO_3$: a promising high-k dielectric for reliable gate stacks at low thermal budget,** D. Claes[1,2], J. Franco[1], N. Collaert[1], D. Linten[1], and M. M. Heyns[1,2], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

9:40 AM 1.3 - **Improvement of InGaAs interface properties by H_2O-based La_2O_3,** R. Suzuki[1], S. Yoshida[1], T. Sasaki[1], I. Oshiyama[1], T. Hirano[1], M. Saito[1], K. Ohno[1], H. Iwamoto[1], J. Franco[2], V. Putcha[2], D. Cott[2], S. Sioncke[2], A. Vais[2], and N. Collaert[2], [1]*Sony, Japan,* [2]*imec, Belgium*

10:00 AM Coffee break

Session 2: Atomic Layer Deposition & Selective Processes

Session Chair: J. Wrench

10:20 AM 2.1 *Invited* - **ALD for Semiconductor Interfaces,** G. Wilk, *ASM America*

10:55 AM 2.2 *Invited* - **Surface Processes for Selective Atomic Layer Deposition,** S. F. Bent, *Stanford U.*

11:30 AM 2.3 - **Hyper-Selective Co Metal ALD on Cu and Pt Without Passivation,** S. Wolf, M. Breeden, S. Ueda, A. C. Kummel, *UCSD*

11:50 AM 2.4 - **Selective Etching of Native Silicon Oxide and Flowable SiO_2 in Preference to Silicon, Thermal Silicon Oxide and Silicon Nitride,** C. F. Ahles[1], J. Y. Choi[1], R. Hung[2], N. Kim[2], S. Nemani[2], and A. C. Kummel[1], *[1]UCSD, [2]Applied Materials*

12:10 PM Adjourn for lunch

Session 3: Poster Preview Session I – High-k Dielectrics and High Mobility Channels

Session Chair: A. C. Kummel

1:30 PM 3.1 - **Electron Mobility Enhancement by Tensile Strain in Germanium Nanowire NFETs considering surface roughness, channel dopant charge, interface charge, and phonon scattering,** Hung-Yu Ye[1]Chia-Che Chung[1], and C. W. Liu[1,2], *[1]National Taiwan U., Taiwan, [2]National Nano Device Laboratories, Taiwan*

1:32 PM 3.2 - **Correlation of interface state generation and InGaAs MOS interface properties,** S.-H. Yoon, D.-H. Ahn, C. Yokoyama, M. Takenaka, and S. Takagi, *U. Tokyo, Japan*

1:34 PM 3.3 - **High-mobility P- and N-channel GeSn Thin-film Transistors on Transparent Substrate Fabricated by Nucleation-controlled Liquid-phase Crystallization,** T. Hosoi, H. Oka, K. Inoue, Y. Wada, T. Shimura, and H. Watanabe, *Osaka U., Japan*

1:36 PM 3.4 - **Effect of incorporating Hf atoms in AlON gate dielectrics on hole leakage current,** T. Nagura[1], K. Chokawa[1], M. Araidai[1], T. Hosoi[2], H. Watanabe[2], A. Oshiyama[1], and K. Shiraishi[1], *[1]Nagoya U., Japan, [2]Osaka U., Japan*

1:38 PM 3.5 - **Investigation of dipole origin at high k dielectric hetero-junction interface,** L. Zhou, X. Wang, J. Xiang, C. Zhao, T. Ye, and W. Wang, *Chinese Academy of Sciences, China*

1:40 PM 3.6 - **Simulation of Mobility Degradation by Interfacial Dipole in Gate Stack of Ge pMOSFET,** X. Wang, L. Zhou, X. Ma, J. Xiang, and W. Wang, *Chinese Academy of Sciences, China*

1:42 PM 3.7 - **Modulation of InGaAs MOSCAP Interface State Density across the Band-Gap and Direct Correlation with MOSFET Sub-Threshold Swing down to 65 mV/decade,** J. Rozen[1], E. A. Cartier[1], T. Ando[1], M. M. Frank[1], K.-T. Lee[1], P. Kerber[1], J.-B. Yau[1], E. P. O'Connor[2], Y. Ogawa[3], M. Hatanaka[3], and V. Narayanan[1], *[1]IBM, [2]IBM, Switzerland, [3]ULVAC Inc., Japan*

1:44 PM 3.8 - **Further investigation of Fermi-level pinning on Ge from substrate side,** T. Nishimura, X. Luo, T. Yajima, and A. Toriumi, *U. Tokyo, Japan*

1:46 PM 3.9 - **Observation of Anomalous Bias Temperature Instability in $Hf_{0.5}Zr_{0.5}O_2$-based Germanium Ferroelectric Nanowire pFETs,** W. Chung, M. Si, and P. D. Ye, *Purdue U.*

1:48 PM 3.10 - **Investigation of post deposition annealing on hole mobility of Ge pMOSFET,** L. Zhou, X. Wang, J. Xiang, C. Zhao, T. Ye, and W. Wang, *Chinese Academy of Sciences, China*

1:50 PM 3.11 - **Stabilization of Dielectric Layers on Germanium,** L.P. Etcheverry and C. Radtke, *UFRGS, Brazil*

1:52 PM 3.12 - **EOT scaling of MOSCAPs on etched (100)- and (110)-oriented $In_{0.53}Ga_{0.47}As$ layers via a TiN capping layer insertion,** Y.-C. Fu[1], D. Millar[1], X. Li[1], M. Steer[1], U. Peralagu[1], H. Zhou[1], R. Droopad[2], and I. G. Thayne[1], *[1]U. Glasgow, UK, [2]Texas State U.*

1:54 PM 3.13 - **Transport mechanisms in Al_2O_3 and HfO_2 MIG structures with Si-nanosized electrodes,** C. A. Chavarin[1], M. Junige[2], M. Lukosius[1], J. Kitzmann[1], M. Albert[2], J. W. Bartha[2], and C. Wenger[1], *[1]IHP GmbH, Germany, [2]TU Dresden, Germany*

Session 4: Ferroelectrics I – FETs and NC

Session Chair: P. C. McIntyre

2:05 PM 4.1 *Invited* - **Quasi-Static Negative Capacitance (QSNC): Science Fact or Science Fiction?,** T. P. Ma, *Yale U.*

2:40 PM 4.2 - **Sense and non-sense of negative capacitance in ferroelectric devices,** J. Van Houdt, *[1]imec, Belgium, [2]U. Leuven, Belgium*

3:00 PM 4.3 - **On the Diminished Hysteresis Observed in Ferroelectric-gated FET's (FeFET's) Attributed to the Negative Capacitance Effect,** Z. Liu and T. P. Ma, *Yale U.*

3:20 PM 4.4 - **A Ferroelectric Semiconductor Field-Effect Transistor with ALD Passivation,** M. Si and P. D. Ye, *Purdue U.*

3:40 PM Coffee break

Session 5: Poster Preview Session II – Interfaces, Materials and Devices

Session Chair: J. Robertson

4:05 PM 5.1 - **Digital and Analog Resistive Switching Characteristics under 200 nA Current Level using Novel Ni/SiO_x/W 16×16 Cross-point Architecture,** S. Samanta, K. Han, S. Xu, X. Gong, and X. Fong, *NUS, Singapore*

4:07 PM 5.2 - **Surface and Bulk Carrier Transports in Accumulation-mode GaN MOSFETs,** N. Taoka[1], N. H. Trung[1], H. Yamada[1], T. Takahashi[1], T. Yamada[1], T. Kubo[2], T. Egawa[2], and M. Shimizu[1,3], *[1]AIST, Japan, [2]Nagoya Institute of Technology, Japan, [3]Nagoya U., Japan*

4:09 PM 5.3 - **Electron States in Ovonic Switching Ge_xSe_{1-x} (0.4 < x <0.72) Films,** V. V. Afanas'ev[1], N. S. Avasarala[2], L. Goux[2], G. S. Kar[2], M. Houssa[1], and A. Stesmans[1], *[1]U. Leuven, Belgium, [2]imec, Belgium*

4:11 PM 5.4 - **Applications of amorphous Ga_2O_3 deposited by pulsed laser deposition and sputtering at room temperature,** M. I. Pintor-Monroy[1], B. L. Murillo-Borjas[1], G. A. Velázquez-Nevárez[2], and M. A. Quevedo-Lopez[1], *[1]UT Dallas, [2]Instituto Politécnico Nacional, Mexico*

4:13 PM 5.5 - **DFT Study on Atomic and Electronic Structures of SiC/SiO_2 after NO Annealing,** T. Ono, *U. Tsukuba, Japan*

4:15 PM 5.6 - **Self-Assembled Monolayers (SAMs) for Hyperselective Silicide, Metal, and Interconnect Diffusion Barrier,** M. Breeden, J. Choi, S. Wolf, C. F. Ahles, and A. C. Kummel, *UCSD*

4:17 PM 5.7 - **Storing Electric Charge Mechanism of the Potassium Ion Electret Used for New Types of Vibration Power Generation Devices,** T. Miyajima, M. Araidai, and K. Shiraishi, *Nagoya U., Japan*

4:19 PM 5.8 - **One Charge per Cycle Observed in Strong Inversion/Accumulation Charge-Pumping,** K. P. Cheung[1], C. Wang[2], and J. P. Campbell, *[1]NIST, [2]Dalian U. Technology, China*

4:21 PM 5.9 - **Effects of Forming Gas Anneal on Electrical Properties of ALD-Al_2O_3/AlGaN/GaN MIS-HEMTs,** T. Kubo, K. Furuoka, M. Miyoshi, and T. Egawa, *Nagoya Institute of Technology, Japan*

4:23 PM 5.10 - **Graphene Nanopore Transistor for Damaged DNA Detection,** N. B. Athreya, O. Milenkovic, and J.-P. Leburton, *UIUC*

4:25 PM 5.11 - **Formation of Electronically And Chemically Passive Termination on PbSe Quantum Dot Superlattices,** S. T. Ueda[1], I. Kwak[1], S. Wolf[1], M. Breeden[1], A. Abelson[2], C. Qian[2], M. Law[2], and A. C. Kummel[1], *[1]UCSD, [2]UC Irvine*

4:27 PM 5.12 - **Characterization of excess carbon near 4H-SiC/SiO_2 interface and its spatial distribution across the interface,** Y. Terao, T. Hirose, H. Teranishi, H. Sato, and A. Takigawa, *Fuji Electric Co., Japan*

4:29 PM 5.13 - **3D TSV Transistor with Ru Metal Gate,** F. Winkler[1], S. Killge[1], M. Pesic[2], and J. W. Bartha[1], *[1]TU Dresden, Germany, [2]MDLsoft Inc.*

4:31 PM 5.14 - **Breakdown Voltage of AlGaN/GaN HEMTs with Low-k/High-k Double Passivation Layers,** K. Nakano, H. Hanawa, and K. Horio, *Shibaura Institute of Technology, Japan*

4:33 PM 5.15 - **Schottky Barrier Height Tuning on Platinum-gated ZnO Metal-Semiconductor Field Effect Transistors by In-Situ Surface Modification,** R. A. Rodriguez-Davila, R. A. Chapman, I. Mejia, M. A. Quevedo-Lopez, and C. D. Young, *UT Dallas*

4:35 PM 5.16 - **High Improvement On The Threshold Voltage Of E-Mode GaN HEMTs with AlGaN Buffer Layer,** G. Kurt, M. Ozturk, M. E. Gulseren, S. Ural, O. A. Kayal, B. Butun, M. Kabak, and E. Ozbay, *Bilkent U., Turkey*

4:37 PM 5.17 - **Normally-off p-GaN Gate InAlN/GaN HEMT with Gradual p-GaN Surface Etch,** M. E. Gulseren, B. Bozok, G. Kurt, O. A. Kayal, M. Ozturk, S. Ural, B. Butun, and E. Ozbay, *Bilkent U., Turkey*

4:39 PM 5.18 - **Microstructure Investigation of SiO_x Layer in Poly-Si/SiO_x Passivated Contacts for Silicon Solar Cells,** A. S. Kale[1], B. Nemeth[2], S. U. Nanayakkara[2], H. Guthrey[2], A. Norman[2], M. R. Page[2], M. Al Jassim[2], S. Agarwal[1], and P. Stradins[2], *[1]Colorado School of Mines, [2]NREL*

4:41 PM 5.19 - **Eu_2O_3 dielectric layers on GaN(0001) Controlling the Structural Polymorph – from hexagonal to monoclinic,** T. Hadamek[1], D. Shin[1], P.-Y. Chen[1], A. Posadas[1], S. Kwon[2], Q. Wang[2], M. Kim[2], J. Ekerdt[1], and A. A. Demkov[1], *[1]UT Austin, [2]UT Dallas*

4:43 PM 5.20 - **Internal Photoemission Spectroscopy Study of Barrier Heights between Ta-based Amorphous Metals and Atomic Layer Deposited Insulators,** M. A. Jenkins, J. M. McGlone, J. F. Wager, and J. F. Conley Jr, *Oregon State U.*

4:45 PM 5.21 - **Design Considerations with Augmented Spacer Dielectric for Vertically Stacked Gate-All-Around MOSFET,** Y.-C. Huang, S.-H. Chen, M.-H. Chiang, and S.-J. Wang, *National Cheng Kung U., Taiwan*

4:47 PM 5.22 - **Suppression of VFB instability in AlSiO/GaN MOS capacitor with crystallized interlayer,** D. Kikuta[1], K. Mitsuishi[2], K. Ito[1], T. Narita[1], Y. Irokawa[2], T. Nabatame[2], and T. Kachi[3], *[1]Toyota, Japan, [2]National Institute for Materials Science, Japan, [3]Nagoya U., Japan*

4:49 PM 5.23 - **TiO_2-IrO_x Alloy as a Hole Transport Material for Perovskite Solar Cells,** W. Tan, O. L. Hendricks, A. C. Meng, M. Braun, M. D. McGehee, C. E. D. Chidsey, and P. C. McIntyre, *Stanford U.*

4:51 PM 5.24 - **Impact of Interface Roughness on Quantum Transport in Double Gate MOSFETs,** P. B. Vyas, M. L. Van de Put, and M. V. Fischetti, *UT Dallas*

4:53 PM 5.25 - **Influence of Deposition Temperature on Passivation and Fixed Charge Stability of Atomic Layer Deposited Aluminum Oxide on Silicon,** N. C. Strandwitz, R. J. Marstell, and B. Davis, *[1]Lehigh U.*

4:55 PM 5.26 - **The effect of an in-situ atomic layer deposited aluminium nitride interlayer between a N_2 treated GaN surface and aluminium oxide on GaN MOS capacitors,** D. T. Hemakumara[1], X. Li[1], K. Floros[1], S.-J. Cho[1], I. Guiney[2], D. Moran[1], C. Humphreys[2], A. O'Mahony[3], H. Knoops[3], and I. G. Thayne[1], *[1]U. Glasgow, UK, [2]U. Cambridge, UK, [3]Oxford Instruments, UK*

4:57 PM 5.27 - **Hydrophilic Crystalline Nanoparticles Based Ultrasensitive MRI Contrast Agents,** J. Wang, J. Flores, S. L. Blair, W. C. Trogler, and A. C. Kummel, *UCSD*

4:59 PM 5.28 - **Effects of Processing Sequence and Ambient Conditions on Doped Polysilicon / Tunneling SiOx Passivated Contact Stack for Silicon Photovoltaics,** B. Nemeth, D. L. Young, M. R. Page, V. LaSalvia, D. Findley, A. S. Kale, S. Theingi, S. P. Harvey, and P. Stradins, *NREL*

5:01 PM 5.29 - **Modification of chemical Si-surface cleaning with vacuum treatment,** J.-P. Lehtiö[1], Z. J. Rad[1], M. Yasir[1], J. Mäkelä[1], M. Kuzmin[1], E. Vuorinen[1], M. P. J. Punkkinen[1], P. Laukkanen[1], K. Kokko[1], R. Punkkinen[1], H.-P. Hedman[1], P. Repo[2], and H. Savin[2], *[1]U. Turku, Finland, [2]Aalto U., Finland*

5:03 PM 5.30 - **Hybrid dielectric films containing conducting nanoparticles,** M. Wiesinger, T. Welzel, and M. Stutzmann, *TU München, Germany*

5:05 PM 5.31 - **Investigation of the deviation of threshold voltage of low-temperature polycrystalline silicon TFTs depending on the grain configuration and channel length,** K.-H. Kim[1,2], J.-Y. Lee[2], and B.-D. Choi[1], *[1]SKKU, Korea, [2]Samsung, Korea*

5:07 PM 5.32 - **Simulation Study of Channel Length Scaling in Laterally Diffused Metal-Oxide-Semiconductor Field-Effect Transistors,** A. Saadat[1], M. L. Van de Put[1], H. Edwards[2], and W. G. Vandenberghe[1], *[1]UT Dallas, [2]Texas Instruments Inc.*

5:09 PM 5.33 - **Growth of crystalline bismuth oxide thin film on Si(100),** M. Yasir[1], M. Kuzmin[1,2], Z. J. Rad[1], M. P. J. Punkkinen[1], J. Mäkelä[1], P. Laukkanen[1], and K. Kokko[1], *[1]U. Turku, Finland, [2]Ioffe Physical-Technical Institute, Russia*

5:15 PM Adjourn

7:00 PM Poster Session 1 & Reception

10:00 PM – 12:00 AM Hospitality room

Friday, December 7, 2018

Session 6: 2D Transition Metal Dichalcogenides

Session Chair: C. L. Hinkle

8:00 AM 6.1 *Invited* - **Investigating Interface States and Border Traps in the Oxide/MoS_2 System,** P. K. Hurley[1], P. Zhao[2], P. Bolshakov[2], G. Mirabelli[1], E. Caruso[1], F. Gity[1], S. Monaghan[1], J. Lin[1], L. Walsh[1], K. Cherkaoui[1], C. M. Smyth[2], A. Khosravi[2], A. Azcatl[2], C. L. Hinkle[2], R. M. Wallace[2], and C. D. Young[2], *[1]Tyndall National Institute, Ireland, [2]UT Dallas*

8:35 AM 6.2 - **Contact resistance at 1T-MoS_2/2H-MoS_2 lateral heterojunctions,** M. Houssa[1], K. Iordanidou[2], A. Dabral[3], A. Lu[4], G. Pourtois[3], V. V. Afanas'ev[1], and A. Stesmans[1], *[1]U. Leuven, Belgium, [2]U. Oslo, Norway, [3]imec, Belgium, [4]AIST, Japan*

8:55 AM 6.3 - **Hole-Injection at WO_3-WSe_2 Interface Using a Plasma Oxidation Process for Hole Mobility Enhancement and SBH reduction in p- type 2-D WSe_2 Nanosheet FET,** M. Sivan, Y. Li, Y. Zhao, and A. V.-Y. Thean, *NUS, Singapore*

9:15 AM 6.4 - **Tuning the Electrical Transport Properties of Few-Layer $MoTe_2$ by Phase Engineering,** L. Yang, H. Wu, X. Lou, Z. Xie, X. Yu, H. Chang, and W. Zhang, *Huazhong U. Science and Technology, China*

Session 7: Poster Preview Session III – 2D Materials and Ferroelectrics

Session Chair: W. Zhu

9:40 AM 7.1 - **A key role of doping to HfO_2 for ferroelectric phase formation,** Y. Mori[1], T. Nishimura[1], S. Migita[2], and A. Toriumi[1], *[1]U. Tokyo, Japan, [2]AIST, Japan*

9:42 AM 7.2 - **Synthesis and Characterization of Monolayer $WSe_{2-2x}Te_{2x}$,** A. Sharma, K. Xu, S. Kang, S. Xia, R. Haasch, and W. Zhu, *UIUC*

9:44 AM 7.3 - **Cooling-mediated One-step Synthesis of Monolayer WSe_2/$WSe_{2x}Te_{2-2x}$ Lateral Heterostructures for Photodetector Applications,** S. Kang, S. Xia, Z. Zhao, A. Sharma, and W. Zhu, *UIUC*

9:46 AM 7.4 - **Contact Engineering for Dual-Gate MoS_2 Transistors with O_2 Plasma Exposure,** P. Bolshakov[1], C. M. Smyth[1], A. Khosravi[1], P. Zhao[1], A. Azcatl[1], G. Mirabelli[2], P. K. Hurley[2], C. L. Hinkle[1], R. M. Wallace[1], and C. D. Young[1], *[1]UT Dallas, [2]Tyndall National Institute, Ireland*

9:48 AM 7.5 - **Understanding Ferroelectricity of doped-HfO_2 for the NC-FET,** P. Blaise[1], B. Sklénard[1], N. Vaxelaire[1], O. Renault[1], T. Miyashita[2], K. Wong[2], and N. Kim[2], *[1]CEA/LETI, France, [2]Applied Materials*

9:50 AM 7.6 - **Ge 2D Crystal Growth on Hetero-epitaxial Ag/Ge(111) by N_2 Annealing,** A. Ohta, K. Ito, M. Kurosawa, M. Araidai, M. Ikeda, K. Makihara, and S. Miyazaki, *Nagoya U., Japan*

9:52 AM 7.7 - **ESR study of transferred MoS_2 layers grown by MOCVD: evidence for the Mo vacancy,** A. Stesmans[1], B. Schoenaers[1], A. Leonhardt[2], D. Chiappe[2], I. Asselberghs[2], C. Huyghebaert[2], I. Radu[2], S. De Gendt[2], M. Houssa[1], and V. V. Afanas'ev[1], *[1]U. Leuven, Belgium, [2]imec, Belgium*

9:54 AM 7.8 - **Probing the role of substrate chemistry and interface interactions on MoS_2,** A. Leonhardt[1,2], N. Pellens[2], D. Chiappe[1,3], J. Ludwig[1,2], I. Shlyakhov[2], V. V. Afanas'ev[2], S. Brems[1], I. Asselberghs[1], C. Huyghebaert[1], I. Radu[1], and S. De Gendt[1,2], *[1]imec, Belgium, [2]U. Leuven, Belgium, [3]ASM Microchemistry Ltd., Finland*

9:56 AM 7.9 - **Modulating the barrier height in 2D materials for reduced contact resistance,** S. Suryavanshi[1], P. Blaise[2], and E. Pop[1], *[1]Stanford U., [2]CEA/LETI, France*

9:58 AM 7.10 - **Ferroelectric Zr-doped Hafnium Oxide for Memory Applications,** H. Ryu, K. Xu, D. Kim, F. Rao, and W. Zhu, *UIUC*

10:00 AM 7.11 - **Effects of total ionizing dose radiation on $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric capacitors,** M. A. Bhuiyan[1], M. Si[2], P. D. Ye[2], and T. P. Ma[1], *[1]Yale U., [2]Purdue U.*

10:02 AM 7.12 - **Analog resistance tuning in TiN/HfO_2/TiN ferroelectric tunnel junctions,** M. M. Frank, E. A. Cartier, K.-L. Lee, A. Carr, C. Lavoie, J. Bruley, and V. Narayanan, *IBM*

10:04 AM 7.13 - **Ferroelectricity in Hafnia: a Molecular Dynamics Study,** Z. Song[1],Y. Guo[2], and J. Robertson[1], *[1]U. Cambridge, UK, [2]Swansea U., UK*

10:06 AM 7.14 - **Fermi level de-pinning of contacts to MoS_2 – MIGS or Defects?,** S. Zhang[1], Y Guo[2], and J. Robertson[1], *[1]Cambridge U., UK, [2]Swansea U., UK*

10:08 AM 7.15 - **Graphene-Semiconductor Interface Characterizes via Terahertz 3D Imaging,** A. Rahman, *Applied Research and Photonics, Inc.*

10:10 AM 7.16 - **Impact of the Annealing Temperature on C-V Characteristics of Ferroelectric $HfZrO_x$ on a p-type Si Substrate,** Y.-H. Chen[1], C.-J. Su[2], C. Hu[1,3], and T.-L. Wu[1], *[1]National Chiao Tung U., Taiwan, [2]National Nano Device Laboratories, Taiwan, [3]UC Berkeley*

10:12 AM 7.17 - **Ferroelectric Characteristics of $Hf_{0.5}Zr_{0.5}O_2$-based Metal-Ferroelectric-Insulator-Semiconductor Capacitors for Steep-Slope transistor Applications,** J. H. Roh, H. W. Park, Y. B. Lee, S. D. Hyun, K. D. Kim, T. H. Moon, Y. H. Lee, B. S. Kim, B. Y. Kim, H. H. Kim, and C. S. Hwang, *Seoul National U., Korea*

10:15 AM Coffee break

Session 8: Low-D Semiconductors & Novel FETs

Session Chair: I. Radu

10:40 AM 8.1 - **High-Mobility (> 700 cm^2/V-s) Helical Tellurium Field Effect Transistors Enabled by Transfer-Free, Low-Temperature (120 °C) Direct Growth,** G. Zhou[1], R. Addou[1], Q. Wang[1], S. Honari[1], C. R. Cormier[1], L. Cheng[1], R. Yue[1], C. M. Smyth[1], A. Laturia[1], J. Kim[1], W. G. Vandenberghe[1], M. J. Kim[1], R. M. Wallace[1], and C. L. Hinkle[1,2], *[1]UT Dallas, [2]U. Notre Dame*

11:00 AM 8.2 - **High performance black phosphorus top-gate transistors with alucone dielectrics,** X. Li, X. Xiong, T. Li, and Y. Wu, *Huazhong U. Science and Technology, China*

11:20 AM 8.3 - **Vertically Stacked Poly-Si Nanosheet P-channel Junctionless Field-Effect Transistors with Gate All Around Structure,** Yung-Chun Wu*, Kang-Hui Peng, Meng-Ju, Tsai, Yu-Ru Lin, *National Tsing Hua U., Taiwan*

11:40 AM 8.4 - **EOT scaling of planar-type InGaAs TFETs by using W/ZrO_2/Al_2O_3 gate stacks,** D.-H. Ahn, S.-H. Yoon, K. Kato, T. Fukui, M. Takenaka, and S. Takagi, *U. Tokyo, Japan*

12:00 PM Adjourn for lunch

12:00 PM – 1:30 PM Committee/Invited Speaker luncheon

Session 9: SiGe and Ge MOS

Session Chair: Y.-J. Lee

1:30 PM 9.1 - **Selective surface oxidation with periodic ozone dosing into HfO_2 on SiGe for SiOx interface,** M. S. Kavrik[1], V. Hou[2], E. Rotenberg[3], A. Bostwick[3], K. Tang[4], Y. Taur[1], P. C. McIntyre[4], and A. C. Kummel[1], *[1]UCSD, [2]TSMC, Taiwan, [3]Lawrence Berkeley Laboratory, [4]Stanford U.*

1:55 PM 9.2 - **Reduction in interface trap density of TiN/Y_2O_3/$Si_{0.62}Ge_{0.38}$ gate stacks with high temperature PMA,** T.-E. Lee, M. Ke, K. Kato, M. Takenaka, and S. Takagi, *U. Tokyo, Japan*

2:15 PM 9.3 - **Notable Difference between Rapid-Thermal and Microwave Annealings on Ge pMOSFETs,** S.-H. Yi, K.-S. Chang-Liao, C.-W. Hsu, J.-S. Li, W.-Y. Hsu, and T.-Y. Wu, *National Tsing Hua U., Taiwan*

2:35 PM 9.4 - **Mechanism of Ohmic Contacts on Sb- and Bi-based layers on Si and Ge,** Y. Guo[1,2], H. Zhang[1,3], and J. Robertson[1], *[1]Cambridge U., UK, [2]Swansea U., UK, [3]Peking U., China*

2:55 PM 9.5 - **In-situ B-doped Epi-GeSn Layers on Ge-buffered Si by Chemical Vapor Deposition with High Activation ($4.9x10^{20}cm^{-3}$), High Sn Content(14%), and High Growth Rate Enhancement(24x),** F.-L. Lu[1], C.-E. Tsai[1], S.-Y. Lin[1], and C. W. Liu[1,2], *[1]National Taiwan U., Taiwan, [2]National Nano Device Laboratories, Taiwan*

3:15 PM – 4:45 PM Poster Session 2 & Coffee break

Session 10: Ferroelectrics II, Materials and Devices

Session Chair: T. P. Ma

4:45 PM 10.1 - **Ultra-thin ferroelectric HfO_2 and its application for ferroelectric tunnel junctions,** X. Tian[1], S. Migita[2], and A. Toriumi[1], *[1]U. Tokyo, Japan, [2]AIST, Japan*

5:05 PM 10.2 - **Improvement of Ferroelectricity of $Hf_xZr_{1-x}O_2$ Thin Films by New ZrO_2 Nucleation Technique,** T. Onaya[1,2], T. Nabatame[2], N. Sawamoto[1], A. Ohi[2], N. Ikeda[2], T. Nagata[2], and A. Ogura[1], *[1]Meiji University, Japan, [2]National Institute for Materials Science, Japan*

5:25 PM 10.3 - **Mechanism of Ferroelectric Phase Stabilization and Phase Competition in Doped HfO_2 Films: A First-Principles Study,** H. Z. Fang and S. V. Barabash, *Intermolecular Inc.*

5:45 PM 10.4 - **Hysteresis-free internal potential enhancement in ferroelectric/paraelectric capacitors connected in series,** X. Li and A. Toriumi, *U. Tokyo, Japan*

6:05 PM Adjourn

7:00 PM – 10:00 PM Conference banquet and Limerick contest

10:00 PM – 12:00 AM Hospitality room

Saturday, December 8, 2018

Session 11: Interfaces in Solar and Optoelectronic Devices

Session Chair: P. Stradins

8:00 AM 11.1 *Invited* - **Dopant-Free Carrier Selective Contacts for Highly Efficient Si Solar Cells,** A. Javey, *UC Berkeley*

8:35 AM 11.2 - **Passivated Selective Contacts for Photovoltaics: Molybdenum Oxide Contacts with Aluminum Oxide Tunnel Layers,** N. C. Strandwitz and B. Davis, *Lehigh U.*

8:55 AM 11.3 - **Dopant-free Silicon Solar Cells and need for Fermi Level De-pinning layers,** H. Lu[1], Y. Guo[2], and J. Robertson[1], *[1]Cambridge U., UK, [2]Swansea U., UK*

9:15 AM 11.4 - **>10% Solar-to-Hydrogen efficiency water splitting with interface-engineered silicon heterojunction solar cells,** C. S. Tan[1], K. W. Kemp[1], A. C. Meng[1], W. Tan[1], C. E. D. Chidsey[1], W. Ma[2], F. Moghadam[2], and P. C. McIntyre[1], *[1]Stanford U., [2]Sunpreme Inc.*

9:35 AM 11.5 - **Ferroelectric Modulation of Optoelectronic Properties in Wse_2/In_2Se_3 Heterostructures,** K. Xu[1], X. Gao[2], Z. Zhao[1], and W. Zhu[1], *[1]UIUC, [2]Peking U., China*

9.55 AM Coffee break

Session 12: Wide Band-Gap Semiconductors

Session Chair: H. Watanabe

10:20 AM 12.1 - **A Novel I-V Characterization based on Ultraviolet Light for Quantitative Study of Donor- and Acceptor-like Interface Trap Density over Bandgap Energy in β-Ga_2O_3 FETs,** H. Bae, J. Noh, and P. D. Ye, *Purdue U.*

10:40 AM 12.2 - **Mechanism of Nitrogen Passivation of the SiO_2/SiC(4H-0001) MOS structure: Interface Composition, Physical Stress and Electrical Quality,** X. Li[1], S. S. Lee[2], M. Li[1], A. Ermakov[1], J. Medina-Ramos[2], T. Fister[2], V. Amarasinghe[1], T. Gustafsson[1], E. Garfunkel[1], P. Fenter[2], and L. C. Feldman[1], *[1]Rutgers U., [2]Argonne National Laboratory*

11:00 AM 12.3 - **Scattering mechanisms of free carriers in MOS inversion channel on nitrided 4H-SiC (11-20) a-face investigated by Hall effect measurement,** H. Hirai, T. Hatakeyama, M. Sometani, M. Okamoto, S. Harada, and H. Okumura, *AIST, Japan*

11:20 AM 12.4 - **High Resolution Mapping of Subsurface Defects at SiO_2/SiC Interfaces by Local Deep Level Transient Spectroscopy Based on Time-Resolved Scanning Nonlinear Dielectric Microscopy,** Y. Yamagishi and Y. Cho, *Tohoku U., Japan*

11:40 AM 12.5 - **Exceptional Crystal and Electrical Properties of Atomic Layer Deposited BeO on 4H-SiC,** S. M. Lee[1], J. H. Yum[2], E. S. Larsen[2], C. W. Bielawski[2], and J. Oh[1], *[1]Yonsei U., Korea, [2]IBS and UNIST, Korea*

12:00 PM Adjourn for lunch

Session 13: Memory

Session Chair: P. C. McIntyre

1:30 PM 13.1 *Invited* - **Physics in Charge Injection Induced On-Off Switching Mechanism of Resistive Random Access Memory (ReRAM) and Superlattice GeTe/Sb_2Te_3 Phase Change Memory (iPCM),** K. Shiraishi, *Nagoya U., Japan*

2:05 PM 13.2 - **Experimental and theoretical investigation of RRAM endurance statistical behavior,** D. Alfaro Robayo[1,2], G. Sassine[1], Q. Rafhay[2], G. Ghibaudo[2], G. Molas[1], and E. Nowak[1], *[1]CEA/LETI, France, [2]IMEP LAHC CNRS, France*

2:25 PM 13.3 - **Materials Selection and Non-linear Conduction Mechanism in Chalcogenide Selector Devices,** H. Li[1] and J. Robertson[2], *[1]Tsinghua U., China, [2]Cambridge U., UK*

2:45 PM 13.4 - **DFT Evidence for a Possible Origin of Switching in Chalcogenide Selector Films,** S. V. Barabash, *Intermolecular Inc.*

3:05 PM Closing remarks and adjourn

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