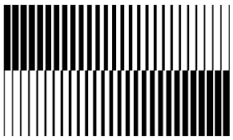

SISC 2019

# 50th IEEE Semiconductor Interface Specialists Conference

December 11–14, 2019
Bahia Resort Hotel, San Diego, CA
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# IEEE SISC 2019

# CONFERENCE PROGRAM

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# SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology," published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author for either an oral or a poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

## 2018 SISC Ed Nicollian Award for Best Student Paper

**Guanyu Zhou**

*UT Dallas*

"High-Mobility (> 700 $cm^2$/V-s) Helical Tellurium Field Effect Transistors Enabled by Transfer-Free, Low-Temperature (120 °C) Direct Growth"

with R. Addou, Q. Wang, S. Honari, C. R. Cormier, L. Cheng, R. Yue, C. M. Smyth, A. Laturia, J. Kim, W. G. Vandenberghe, M. J. Kim, R. M. Wallace, and C. L. Hinkle

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# Wednesday Evening Tutorial

## Wednesday, December 11, 2019, 8:00 PM

First introduced at SISC 2008, the Wednesday evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

**Dr. Jeff Welser,** *IBM Research*

## Building Bits + Neurons + Qubits for the Future of Computing

The building block for all of our computers today, from our phones to the Cloud, is the digital bit. It arose from combining mathematics and information and has driven the digitization of the world for five decades. And while bits have proven exceedingly successful at driving high precision computation, there are emerging workloads and problems that require new approaches.

In the near term, artificial intelligence systems, merging neuron-inspired biology with information, have achieved superhuman accuracy in a range of narrow classification tasks, by learning from labelled data. This has largely been due to the increase availability of that labelled data in digital from, but also from the advances in computing architectures better suited than CPUs to run the deep learning training and inference algorithms required to exploit that data. Most of the progress has been due to GPUs and FPGAs, but there has recently been an increase in custom-designed architectures. Many of these have focused on improved data flow and memory access, as well as the recognition that lower precision calculations can still yield high fidelity results – which can result in increased performance with reduced area and power requirements. This opens the door to creating novel devices, utilizing new materials that enable analog or other non-switch-like behavior. These devices could not only compute the primary calculations more directly, but also could reduce the amount of data that needs to be moved between memory and the processing unit.

Further out, the union of physics and information has led to the development of a quantum bit – the qubit – forming the basis of quantum computers. The qubit can be formed by a variety of techniques, including trapped ions, neutral atoms, in-situ vacancies, or oscillators based on superconducting Josephson Junctions. Most of the recent progress has come from the oscillators, given their solid-state nature and ability to exploit the established semiconductor infrastructure for fabrication and scalability. IBM utilized this technology to release the first 7-qubit cloud-based system in May 2016, and just announced the opening of a full quantum computation center for commercial and research activity – including a new 53-qubit quantum computer – to the expanding ecosystem of developers, engineers, academics, and industry tapping into quantum systems to explore practical applications. For quantum computing to succeed, however, it will require partnerships across diverse organizations, industries and disciplines. Much progress is still needed on the basic materials and structures, as well as understanding of the device physics,

in order to increase the coherence time, decrease the error rates, and increase the circuit depth to enable sufficient quantum volume for tackling problems at scale. Although this technology is still in its early days, quantum computers offer the potential to solve problems which even the most powerful classical computers cannot, particularly in the areas of quantum chemistry, machine learning, and optimization.

The future of computing will look fundamentally different that it has in the past. It will be built upon bits + neurons + qubits, orchestrated through a secure hybrid cloud fabric and intelligent automated programming. And it will continue to be built on the IT foundation that semiconductors have enabled, but now with new challenges and opportunities for innovation at every level from materials to devices to systems, software, programming models, and business implementation.

This tutorial will present an overview of the IBM vision for the future of computing, and then delve in detail into some of the materials and device innovations we are pursuing – new designs to keep bits scaling, new materials and devices to enable analog AI acceleration, and the challenges of developing qubits that have to operate at milli-Kelvin temperatures colder than deep space – to make that vision a reality.

Bio

Dr. Jeffrey Welser is a Vice President in IBM Research, directing Labs based in Almaden, California, as well as Australia, China and Japan. He is also the VP of Exploratory Science research and university partnerships globally, including the MIT–IBM Watson Lab. He oversees exploratory and applied research to advance data technology and analytics for Cloud and AI systems and software, with a strong focus on advanced computing technologies for AI, neuromorphic devices and quantum computing.

After joining IBM Research in 1995, Dr. Welser worked on a broad range of technologies, including novel silicon devices, high-performance CMOS and SOI device design, and next generation system components. He has led teams in both development and research, as well as running industrial, academic and government consortiums, including the SRC Nanoelectronics Research Initiative.

Dr. Welser received his Ph.D. in Electrical Engineering from Stanford University. He holds 21 US Patents and has published over 75 technical papers and presentations. He is a member of the IBM Academy of Technology, an IEEE Fellow, a member of the American Physical Society, Chairman of the Bay Area Science and Innovation Consortium. He serves on several university and industry technical boards, and has participated in numerous Federal agency, National Academies and Congressional panels on advanced semiconductor and computing technology.

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# Conference Agenda Overview

## Wednesday, December 11, 2019

| | | | |
|---|---|---|---|
| **Registration** | 6:00 PM | – | 8:00 PM |
| **Evening Tutorial** | 8:00 PM | – | 10:00 PM |
| **Hospitality Room** | 10:00 PM | – | 12:00 AM |

## Thursday, December 12, 2019

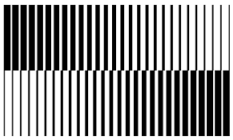
| | | | |
|---|---|---|---|
| **Registration** | 8:00 AM | – | 5:00 PM |
| **Session 1: Quantum Computing & Characterization** | 8:00 AM | – | 9:45 AM |
| **Session 2: Scaling & Novel Materials** | 10:15 AM | – | 12:05 PM |
| **Session 3: Memory & Ferroelectric $HfO_2$ Applications** | 1:30 PM | – | 2:45 PM |
| **Session 4: Poster Preview 1 & Coffee Break** | 2:45 PM | – | 3:40 PM |
| **Session 5: Neuromorphic Computing** | 3:40 PM | – | 5:15 PM |
| **Session 6: Poster Preview 2** | 5:15 PM | – | 5:55 PM |
| **Reception & Poster Session** | 7:15 PM | – | 10:15 PM |
| **Hospitality Suite** | 10:00 PM | – | 12:00 AM |

## Friday, December 13, 2019

| | | | |
|---|---|---|---|
| **Registration** | 8:00 AM | – | 12:00 PM |
| **Session 7: Interfaces** | 8:00 AM | – | 10:00 AM |
| **Session 8: RF Device Materials** | 10:25 AM | – | 12:00 PM |
| **Committee / Invited Speaker Luncheon** | 12:00 PM | – | 1:30 PM |
| **Session 9: Resistive Memory & Ge Materials** | 1:30 PM | – | 2:45 PM |
| **Session 10: Ovonic Materials** | 3:10 PM | – | 4:05 PM |
| **Session 11: Rump Session** | 4:10 PM | – | 6:00 PM |
| **Conference Banquet & Limerick Contest** | 7:00 PM | – | 10:00 PM |
| **Hospitality Suite** | 10:00 PM | – | 12:00 AM |

## Saturday, December 14, 2019

| | | | |
|---|---|---|---|
| **Session 12: Ferroelectric $HfO_2$ Properties** | 8:00 AM | – | 10:00 AM |
| **Session 13: 2D Materials** | 10:20 AM | – | 12:15 PM |
| **Session 14: Wide Gap Materials** | 12:30 PM | – | 1:50 PM |



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## Wednesday, December 11, 2019

### Tutorial

Session Chair: J. Robertson

8:00 PM – 9:30 PM *Tutorial* – **Building Bits + Neurons + Qubits for the Future of Computing,** J. J. Welser, *IBM Research*

9:30 PM – 12:00 AM Hospitality room

## Thursday, December 12, 2019

### Session 1: Quantum Computing & Characterization

Session Chair: P. C. McIntyre

8:00 AM Introduction

8:10 AM 1.1 *Invited* – **Dielectric Interface and Materials Challenges for Quantum Computing,** R. Pillarisetty, *Intel*

8:45 AM 1.2 – **A method to distinguish between interface traps and border traps in MOS systems,** E. Caruso, E. Serriani, J. Lin, K. Cherkaoui, F. Gity, S. Monaghan, and P. K. Hurley, *Tyndall National Institute, Ireland*

9:05 AM 1.3 – **Contributions of electron and hole slow traps to hysteresis in C-V characteristics of $Al_2O_3$/$GeO_x$/p-Ge MOS capacitors,** M. Ke[1], M. Takenaka[2], and S. Takagi[2], [1]*Tokyo U. of Science, Japan,* [2]*U. Tokyo, Japan*

9:25 AM 1.4 – **Near-zero magnetic field spin dependent charge pumping for the study of MOSFET interfaces,** M. A. Anders[1], P. M. Lenahan[2], N. J. Harmon[3], M. E. Flatte[4], and J. T. Ryan[1], [1]*NIST,* [2]*Pennsylvania State U.,* [3]*U. Evansville,* [4]*U. Iowa*

9:45 AM Coffee Break

## Session 2: Scaling & Novel Materials

Session Chair: J. Robertson

10:15 AM 2.1 *Invited* – **Narrow interconnects: The search for new metals,** D. Gall, A. Jog, and E. Milosevic, *Rensselaer Polytechnic Institute*

10:50 AM 2.2 – **Selectivity Comparison of Co & Ru Metal ALD on Cu, Pt, and $SiO_2$,** M. Breeden, S. Wolf, J. Choi, S. Ueda, and A. C. Kummel, *UCSD*

11:10 AM 2.3 – **Impact of atomic layer deposition high-k materials on $Si_{0.78}Ge_{0.22}$ MOS interface properties with TiN gate,** T.-E. Lee, K. Toprasertpong, M. Takenaka, and S. Takagi, *U. Tokyo, Japan*

11:30 AM 2.4 *Invited* – **The Next Era of Scaling in Electronics,** S. Datta, *U. Notre Dame*

12:05 PM Adjourn for Lunch

12:05 PM – 1:30 PM Lunch

## Session 3: Memory & Ferroelectric $HfO_2$ Applications

Session Chair: A. C. Kummel

1:30 PM 3.1 *Invited* – **Hafnium-based Vertical Ferroelectric FET: A New Mass Storage Device,** J. Van Houdt, [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

2:05 PM 3.2 – **Ferroelectricity in undoped $HfO_2$ via nanosecond Laser crystallization,** M. M. Frank, E. A. Cartier, K.-L. Lee, A. Carr, C. Lavoie, J. Bruley, J. L. Jordan-Sweet, O. Gluschenkov, and V. Narayanan, *IBM Research*

2:25 PM 3.3 – **Reliability of Ferroelectric $Hf_xZr_{1-x}O_2$ Thin Films Using 300°C Low Temperature Process with Plasma-Enhanced Atomic Layer Deposition,** T. Onaya[1,2,3], T. Nabatame[3], Y. C. Jung[2], H. Hernandez-Arriaga[2], J. Mohan[2], H. S. Kim[2], A. Khosravi[2], N. Sawamoto[1], T. Nagata[3], R. M. Wallace[2], J. Kim[2], and A. Ogura[1], [1]*Meiji U., Japan,* [2]*UT Dallas,* [3]*National Institute for Materials Science, Japan*

## Session 4: Poster Preview 1

Session Chair: R. M. Wallace

2:45 PM 4.1 – **A New Evaluation Technique for Interface Defect Density on High-$\kappa$/$SiO_2$/Si and $SiO_2$/Si Gate Stacks using Scanning Nonlinear Dielectric Microscopy,** K. Suzuki, K. Yamasue, and Y. Cho, *Tohoku U., Japan*

2:46 PM 4.2 – **Improvement of the Interface and Bulk Properties of TiN/$HfO_2$/$SiO_2$/Si Gate Stacks using Flash Lamp Annealing combined with Low Temperature Heating in an $NH_3$ Ambient,** H. Kawarazaki[1], A. Ueda[1], T. Aoyama[1], S. Kato[1], Y. Nozaki[1], K. Shuto[2], T. Yoshinaka[2], and Y. Nara[2], [1]*SCREEN Semiconductor Solutions Co., Japan,* [2]*U. Hyogo, Japan*

2:47 PM 4.3 – **Involvement of Si/$SiO_2$ Interface Defects in Leakage Currents through Thin $SiO_2$,** S. J. Moxim[1], J. P. Ashton[1], P. M. Lenahan[1], and S. W. King[2], [1]*Pennsylvania State U.,* [2]*Intel*

2:48 PM 4.4 – **Effective Work Function Tuning of Stacked $WN_x$ Films by Sputtering,** C.-E. Tsai, C.-H. Huang, Y.-R. Chen, Y.-C. Liu, and C. W. Liu, *National Taiwan U., Taiwan*

2:49 PM 4.5 – **Investigating the Structural and Electronic properties of Polycrystalline GaSb Thin Films grown on $SiO_2$,** A. Curran, F. Gity, A. Gocalinska, E. Mura, R. E. Nagle, M. Schmidt, B. Sheehan, E. Pelucchi, C. O'Dwyer[1,2], and P. K. Hurley, [1]*Tyndall National Institute, Ireland,* [2]*U. College Cork, Ireland*

2:50 PM 4.6 – **Determining Parameters for Transport Through Defects in Stressed MOS Devices,** S. R. McMillan[1], N. J. Harmon[2], J. P. Ashton[3], P. M. Lenahan[3], and M. E. Flatte[1,4], [1]*U. Iowa,* [2]*U. Evansville,* [3]*Pennsylvania State U.,* [4]*U. Chicago*

2:51 PM 4.7 – **Channel Length Scaling in Laterally Diffused Metal-Oxide-Semiconductor Field-Effect Transistors: A Semiclassical and Quantum Transport Study,** A. Saadat[1], P. B. Vyas[1], M. L. Van de Put[1], M. V. Fischetti[1], H. Edwards[2], and W. G. Vandenberghe[1], [1]*UT Dallas,* [2]*Texas Instruments Inc.*

2:52 PM 4.8 – **Low-temperature cleaning and oxidation of silicon surfaces,** Z. J. Rad[1], I. Mack[2], J.-P. Lehtiö[1], I. T. S. Heikkinen[2], V. Vähänissi[2], M. Kuzmin[1], M. P. J. Punkkinen[1], R. Punkkinen[1], H.-P. Hedman[1], P. Laukkanen[1], H. Savin[2], and K. Kokko[1], [1]*U. Turku, Finland,* [2]*Aalto U., Finland*

2:53 PM 4.9 – **Self Assembled Monolayer Treatment of Tunneling $SiO_2$ for Improved Adhesion of Passivated Contact for Silicon Solar Cells,** W. Nemeth[1], M. Hartenstein[2], S. P. Harvey[1], D. L. Young[1], M. R. Page[1], S. Theingi[1], V. LaSalvia[1], S. Agarwal[2], and P. Stradins[1], [1]*National Renewable Energy Lab,* [2]*Colorado School of Mines*

2:54 PM 4.10 – **Precision Defect Engineering of Metal/Insulator/Metal (MIM) Diodes using Localized ALD Transition Metal Impurities,** K. E. K. Holden, Y. Qi, M. A. Jenkins, and J. F. Conley Jr, *Oregon State U.*

2:55 PM 4.11 – **Dependence of Breakdown Voltage Enhancement on Buffer Acceptor Density and Gate-to-Drain Distance in AlGaN/GaN HEMTs with High-k Passivation Layer,** R. Tomita, S. Ueda, Y. Kawada, and K. Horio, *Shibaura Institute of Technology, Japan*

2:56 PM 4.12 – **Ultraviolet Radiation Effect on the Electrical Characteristics of Nanowire FETs with Ferroelectric $HfZrO_2$ (HZO) Dielectric,** R. W. Chuang[1], Y.-L. Lee[1], Y.-J. Lee[2], P.-J. Sung[2], and C.-J. Su[2], [1]*National Cheng Kung U., Taiwan,* [2]*Taiwan Semiconductor Research Institute, Taiwan*

2:57 PM 4.13 – **Atomic and Electronic structure of Quantum Dot Super Lattice,** M. S. Kavrik[1], W. Ko[2], J. A. Hachtel[2], C. Qian[3], A. Abelson[3], H. Kashyap[1], A. Li[2], J. Idrobo[2], M. Law[3], and A. C. Kummel[1], [1]*UCSD,* [2]*Oak Ridge National Laboratory,* [3]*UC Irvine*

2:58 PM 4.14 – **Transition from the (100)-Oriented Grain-Boundary Free Lateral Growth to Randomly Oriented Nano-Crystal Growth at Higher Laser Power in the CW Laser Crystallization of a-Si Thin Films on Insulator,** N. Sasaki[1,2,3], M. Arif[2], Y. Uraoka[2], J. Gotoh[3], and S. Sugimoto[3], [1]*Sasaki Consulting, Japan,* [2]*NAIST, Japan,* [3]*V-Technology, Japan*

2:59 PM 4.15 – **Reducing leakage current in Si-based photodetectors with a novel sidewall passivation method,** J.-P. Lehtiö, Z. J. Rad, M. Kuzmin, M. P. J. Punkkinen, P. Laukkanen, K. Kokko, R. Punkkinen, and H.-P. Hedman, *U. Turku, Finland*

3:00 PM 4.16 – **Electro-optical co-integration of chip-components for optical and wireless communication in high-performance computing systems,** K. Nieweglowski, L. Lorenz, F. Ellinger, G. P. Fettweis, and K. Bock, *TU Dresden, Germany*

3:01 PM 4.17 – **Study of $^{60}$Co Gamma-ray Radiation Effect on $HfZrO_x$-based FeFET Memory Performance,** C.-Y. Chan, K.-Y. Chen, C.-P. Chou, Y.-X. Lin, Y.-K. Huang, and Y.-H. Wu, *National Tsing Hua U., Taiwan*

3:02 PM 4.18 – **Reliability of Poly-GeSn based Ferroelectric Devices on Flexible Substrate,** Y.-K. Huang, C.-P. Chou, Y.-X. Lin, C.-Y. Chan, and Y.-H. Wu, *National Tsing Hua U., Taiwan*

3:03 PM 4.19 – **Analysis of anti-ferroelectric and ferroelectric $Hf_{1-X}Zr_XO_2$ crystal phases using ACOM-TEM,** K. Kurushima[1], M. Yasuda[1], Y. Tanahashi[1], K. Okada[1], H. Hashimoto[1], and S. Migita[2], [1]*Toray Research Center, Inc., Japan,* [2]*AIST, Japan*

3:04 PM 4.20 – **Ferroelectric dipole relaxation with scaling of $Hf_{0.5}Zr_{0.5}O_2$ on Silicon,** J. Mohan[1], Y. C. Jung[1], H. Hernandez-Arriaga[1], T. Onaya[1,2], H. S. Kim[1], A. Khosravi[1], R. M. Wallace[1], A. Ogura[2], and J. Kim[1], [1]*UT Dallas,* [2]*Meiji U., Japan*

3:05 PM 4.21 – **Memory Window Improvement of HZO-Based FeFETs with $HfO_2$ interlayer,** Z. Yu, F. Huang, Y. Nishi, S. Wong, and P. C. McIntyre, *Stanford U.*

3:06 PM 4.22 – **The Evaluation of the TDDB and the SILC Behaviors in Thin $GeO_2$/Ge Gate Stacks Fabricated by Thermal Oxidation,** S. Yuan, Z. Chen, J. Li, and R. Zhang, *Zhejiang U., China*

3:07 PM 4.23 – **Comparative studies of (001), (110) and (111) epi-Ge surfaces oxidation by in-situ high-resolution synchrotron radiation photoemission,** Y. T. Cheng[1], H. W. Wan[1], C. P. Cheng[2], T. W. Pi[3], J. Kwo[4], and M. Hong[1], [1]*National Taiwan U., Taiwan,* [2]*National Chiayi U., Taiwan,* [3]*National Synchrotron Radiation Research Center, Taiwan,* [4]*National Tsing Hua U., Taiwan*

3:08 PM 4.24 – **Thin Si-capped Ge(100), (110), and (111) Gate Stacks – Attainment of Low Interfacial Trap Density for FinFET Application and the Reliability,** H. W. Wan[1], Y. T. Cheng[1], C. K. Cheng[1], Y. J. Hong[1], T. Y. Chu[1], C. T. Wu[2], J. Kwo[3], and M. Hong[1], [1]*National Taiwan U., Taiwan,* [2]*Taiwan Semiconductor Research Institute, Taiwan,* [3]*National Tsing Hua U., Taiwan*

3:09 PM 4.25 – **Modulated phase transition properties of Ge-doped $VO_2$ thin films grown by ALD,** G. Bai, K. M. Niang, and J. Robertson, *U. Cambridge, UK*

3:10 PM 4.26 – **Experimental Study of Low-temperature Oxidation of SiGe by Ozone,** X. L. Ma and X. L. Wang, *Chinese Academy of Sciences, China*

3:15 PM Coffee Break

## Session 5: Neuromorphic Computing

### Session Chair: M. M. Frank

3:40 PM 5.1 *Invited* – **Hardware Implementation of RRAM based Binarized Neural Networks,** Z. Zhou[1], P. Huang[1], Y. Z. Zhang[1], Y. C. Xiang[1], W. S. Shen[1], Y. D. Zhao[1], Y. L. Feng[1], B. Gao[2], H. Q. Wu[2], H. Qian[2], L. F. Liu[1], X. Zhang[1], X. Y. Liu[1], and J. F. Kang[1], [1]*Peking U., China,* [2]*Tsinghua U., China*

4:15 PM 5.2 – **Evaluation of SONOS based Analog Non-Volatile Memory cell for Neuromorphic Computing,** V. Prabhakar, K. Ramkumar, V. Agrawal, L. Hinh, S. Saha, S. Samanta, and R. M. Kapre, *Cypress Semiconductor*

4:35 PM 5.3 – **Re-doped and Nb-doped $MoS_2$ synaptic transistors for neuromorphic computing,** S. Bhattacharjee[1], R. Wigchering[1], H. Manning[2], J. J. Boland[2], and P. K. Hurley[1], [1]*Tyndall National Institute, Ireland,* [2]*Trinity College Dublin, Ireland*

4:55 PM 5.4 – **Hybrid Selector for Cross-point Memory Array with Excellent Read-out Margin ($>$90%, $>10^{12}$ word lines) and Fast Operating System,** J. Park, J. Yoo, and H. Hwang, *Pohang U. of Science and Technology, Korea*

## Session 6: Poster Preview 2

Session Chair: C. L. Hinkle

5:15 PM 6.1 – **Dark current reduction for the chemically doped graphene/p-Si Schottky photodetector,** T. J. Yoo, S. Y. Kim, C. Kim, M. G. Kwon, K. E. Chang, H. J. Hwang, and B. H. Lee, *GIST, Korea*

5:16 PM 6.2 – **Fermi Level Pinning between Molybdenum Dichalcogenides and Bulk Metal Contacts: Interface Chemistry and Band Alignment,** C. M. Smyth, R. Addou[1,2], C. L. Hinkle[1,3], and R. M. Wallace, [1]*UT Dallas,* [2]*Oregon State U.,* [3]*Notre Dame U.*

5:17 PM 6.3 – **Robust ferromagnetism in Cr-doped semiconducting $MoTe_2$,** L. Yang, H. Wu, X. Wen, Z. Xie, Y. Liu, H. Chang, and W. Zhang, *Huazhong U. of Science and Technology, China*

5:18 PM 6.4 – **Ab-initio Study of Magnetic Order and Stability of Intercalated $WSe_2$,** P. Reyntjens, S. Tiwari, M. L. Van de Put, B. Sorée[2,3,4], and W. G. Vandenberghe, [1]*UT Dallas,* [2]*imec, Belgium,* [3]*U. Leuven, Belgium,* [4]*U. Antwerpen, Belgium*

5:19 PM 6.5 – **Non-linear conduction processes in Chalcogenide Selector device,** Y. Guo[1], H. Li[2], and J. Robertson[3], [1]*Wuhan U., China,* [2]*Tsinghua U., China,* [3]*U. Cambridge, UK*

5:20 PM 6.6 – **Performance of Helical Tellurium double-gate MOSFETs from first principles,** Y. Yin, C. Shao, and Y. Guo, *Wuhan U., China*

5:21 PM 6.7 – **Ferromagnetism and Exchange in Fe-Doped $WSe_2$,** G. Zhou[1], V. Nguyen[2], C. M. Smyth[3], R. M. Wallace[3], J. Heron[2], and C. L. Hinkle[1], [1]*Notre Dame U.,* [2]*U. Michigan,* [3]*UT Dallas*

5:22 PM 6.8 – **Variations of paramagnetic defects and dopants in geo-$MoS_2$ from diverse localities probed by ESR,** A. Stesmans, B. Schoenaers, and V. V. Afanas'ev, *U. Leuven, Belgium*

5:23 PM 6.9 – **The anisotropic electrical property of antimonene,** Y. Yin, C. Shao, and Y. Guo, *Wuhan U., China*

5:24 PM 6.10 – **Investigating the Temperature Dependence of Carrier Mobility in $MoS_2$ grown by Chemical Vapour Deposition.,** E. Coleman[1], S. Monaghan[1], J. Lin[1], F. Gity[1], M. Schmidt[1], J. Connolly[1], L. Walsh[1], K. Cherkaoui[1], K. O'Neill[2], N. McEvoy[2], C. O'Coileain[2], C. O'Dwyer[3], G. Duesberg[4], I. M. Povey[1], and P. K. Hurley[1], [1]*Tyndall National Institute, Ireland,* [2]*Trinity College Dublin, Ireland,* [3]*U. College Cork, Ireland,* [4]*U. Bundeswehr Munchen, Germany*

5:25 PM 6.11 – **Dual Channel Ternary Graphene Barristor with Tunable Schottky Barrier Height controlled by Chemical Doping,** S. Y. Kim, Y. Lee, C. Kim, H. I. Lee, K. Kim, H. J. Hwang, and B. H. Lee, *GIST, Korea*

5:26 PM 6.12 – **Influence of phase on Schottky barrier heights of Ge-Sb-Te based materials,** Z. Zhang[1], Y. Guo[2], and J. Robertson[1], [1]*U. Cambridge, UK,* [2]*Swansea U., UK*

5:27 PM 6.13 – **Intermixing-protected interfacial phase-change memory with Weyl semimetal phase,** J. Tominaga[1], N. Miyata[1], S. Sumi[2], H. Awano[2], and S. Murakami[3], [1]*AIST, Japan,* [2]*Toyota Technological Institute, Japan,* [3]*Tokyo Institute of Technology, Japan*

5:28 PM 6.14 – **Passivation mechanism of $SiO_2$/4H-SiC(0001) interface with defects,** Z. Wang, C. Shao, and Y. Guo, *Wuhan U., China*

5:29 PM 6.15 – **Influence of surface pre-conditioning and post-deposition annealing on $V_{th}$ instability under positive gate bias operation in AlGaN/GaN MIS-HEMTs,** A. Calzolaro, R. Hentschel, N. Szabó, A. Großer, J. Gärtner, A. Wachowiak, and T. Mikolajick[1,2], [1]*NaMLab gGmbH, Germany,* [2]*Institute of Semiconductors and Microsystems, Germany*

5:30 PM 6.16 – **Improved Growth of Low-Temperature GaN for BEOL Technologies,** T. Sun, G. Zhou, and C. L. Hinkle, *Notre Dame U.*

5:31 PM 6.17 – **The role of oxygen ambient anneal for Ba-incorporated $SiO_2$/SiC interface,** Y. Terao[1], H. Tsuji[1], T. Hosoi[2], X. Zhang[3], H. Yano[3], T. Shimura[2], and H. Watanabe[2], [1]*Fuji Electric Co., Japan,* [2]*Osaka U., Japan,* [3]*U. Tsukuba, Japan*

5:32 PM 6.18 – **Schottky barrier diode on nonpolar AlN crystal grown by physical vapor transport: Barrier inhomogeneity analysis,** B. Li[1], Q. Zhou[1], H. Wu[1], X. Tang[1], R. Zheng[1], H. Li[2], and J. Wang[2], [1]*Shenzhen U., China,* [2]*Hong Kong U. of Science and Technology, China*

5:33 PM 6.19 – **Investigation of Gate Degradation by High Positive Gate Bias in p-GaN Gate AlGaN/GaN HEMTs,** M.-Y. Tsai, Y.-C. Lai, Y.-N. Zhong, and Y.-M. Hsin, *National Central U., Taiwan*

5:34 PM 6.20 – **Band alignment calculation of dielectric films on GaN,** Z. Zhang[1], Y. Guo[2], and J. Robertson[1], [1]*U. Cambridge, UK,* [2]*Swansea U., UK*

5:35 PM 6.21 – **Testing Semiconductor Band Offset models using ZnO interfaces,** J. Chen[1], Y. Guo[2], Z. Zhang[1], and J. Robertson[1], [1]*U. Cambridge, UK,* [2]*Swansea U., UK*

5:36 PM 6.22 – **2D Interface Defect Density Evaluation on Macrostepped $SiO_2$/SiC Using Local Deep Level Transient Spectroscopy Based on Scanning Nonlinear Dielectric Microscopy,** A. Hosaka[1], K. Yamasue[1], J. Woerle[2,3] , G. Ferro[4], U. Grossner[2], M. Camarda[3,2], and Y. Cho[1], [1]*Tohoku U., Japan,* [2]*ETH Zurich, Switzerland,* [3]*Paul Scherrer Institute, Switzerland,* [4]*Université de Lyon Villeurbanne, France*

5:37 PM 6.23 – **Investigation of Processing Effects on the 4H-SiC/$SiO_2$ Interface Using Electrically Detected Magnetic Resonance: Barium Interfacial Layer vs. NO Annealing,** J. P. Ashton[1], P. M. Lenahan[1], D. J. Lichtenwalner[2], and A. J. Lelis[3], [1]*Pennsylvania State U.,* [2]*Wolfspeed,* [3]*U.S. Army Research Laboratory*

5:38 PM 6.24 – **Processes for Low Temperature Crystalline Aluminum Nitride Atomic Layer Deposition,** A. McLeod, S. T. Ueda, V. Wang, and A. C. Kummel, *UCSD*

5:39 PM 6.25 – **Assessment of Models of RRAM for analog compute applications,** R. Muralidhar, T. Ando, Y. Kim, J. Tersoff, and V. Narayanan, *IBM Research*

5:40 PM 6.26 – **Analysis of Interface Trap (Nit) Recovery Mechanism in 3D NAND Flash Memories,** S. Kim and H. Shin, *Seoul National U., Korea*

5:41 PM 6.27 – **Engineering Ag Doping Profile for Investigating Volatile Switching Characteristics to Reduce $V_{th}$ Variability on CBRAM-type Selectors for Cross-point Array Application,** H. S. Kim, A. Sahota, J. Mohan, Y. C. Jung, and J. Kim, *UT Dallas*

5:42 PM 6.28 – **Gate-tunable memristor using two-dimensional $SnO_x$ nanosheet,** C.-H. Huang and K. Nomura, *UCSD*

5:43 PM 6.29 – **First principles investigation of current-induced magnetization switching in STT-MRAM,** M. Araidai[1], T. Yamamoto[2], and K. Shiraishi[1], [1]*Nagoya U., Japan,* [2]*Tokyo U. of Science, Japan*

5:44 PM 6.30 – **Heterodyne sensing of neuropeptide Y using graphene field-effect transistor,** A. E. Islam[1,2], R. Martineau[1,2], S. S. Kim, B. Maruyama, and L. F. Drummy, [1]*Air Force Research Laboratory,* [2]*UES Inc.*

5:45 PM 6.31 – **Digital Nanopore For Single Molecule Quantification: Pathway Towards Noise-Robustness, Ultra Sensitivity, Selectivity and Fast Response,** Z. Tang, R. Nouri, G. Choi, and W. Guan, *Pennsylvania State U.*

5:46 PM 6.32 – **VLSI compatible SiON finFET sensors for biosensing applications: 2D/3D TCAD simulations and experimental verification of pH dependency,** S. Santermans[1,2], K. Martens, G. Hellings, D. Ruic, M. Gupta[1,2], W. Van Roy, B. Du Bois, S. Severi, and M. Heyns[1,2], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

5:47 PM 6.33 – **Selective Water-Free Deposition of $TiO_2$,** C. Ahles[1], J. Choi[1], Y. Cho[1], K. Wong[2], S. Nemani[2], and A. C. Kummel[1], [1]*UCSD,* [2]*Applied Materials*

5:48 PM 6.34 – **Vapor Phase Passivation for Selective ALD and CVD of Metals, Metal Oxides, and Metal Silicides,** A. Anurag, M. Breeden, Y. Cho, C. Ahles, J. Choi, and A. C. Kummel, *UCSD*

5:49 PM 6.35 – **Atomic Layer Deposited Ultrathin and Transparent Cu2O-based Solar Blind Ultraviolet Light Photodetector with a Novel Copper Precursor,** H. Bae, M. Si, J. Noh, G. Qiu, A. R. Charnas, W. Chung, X. Lyu, S. Alghamdi, and P. D. Ye, *Purdue U.*

5:50 PM 6.36 – **Formation of Electronically And Chemically Passive Termination on PbSe Quantum Dot Superlattices,** S. T. Ueda[1], I. Kwak[1], A. Abelson[2], S. Wolf[1], C. Qian[2], M. Law[2], and A. C. Kummel[1], [1]*UCSD,* [2]*UC Irvine*

5:51 PM 6.37 – **Surface chemistry in plasma-free ALD of Indium and Zinc oxides,** O. Madia[1], A. Illiberi[1], T. Ivanova[2], P. Sippola[2], and M. E. Givens[2], [1]*ASM Belgium, Belgium,* [2]*ASM Microchemistry, Finland*

5:55 PM End

7:15 PM – 10:15 PM Reception/Poster Session

10:00 PM – 12:00 AM Hospitality suite

# Friday, December 13, 2019

## Session 7: Interfaces

Session Chair: P. D. Ye

8:00 AM Announcements

8:05 AM 7.1 *Invited* – **Recent progress towards ternary logic devices for extreme low power architecture,** B. H. Lee[1], S. Kim[1], K. Kim[1], H. Lee[1], S. Kang[2], and M. M. Sung[3], [1]*GIST, Korea,* [2]*Pohang Institute of Science and Technology, Korea,* [3]*Hanyang U., Korea*

8:40 AM 7.2 – **On the Impact of Reduced Thermal Budget on $HfO_2$ electron trap and $SiO_2$ hole trap defect bands in RMG Gate Stacks for Sequential 3D CMOS integration,** J. Franco, Z. Wu[1,2], D. Claes[1,2], A. Vandooren, N. Horiguchi, D. Linten, T. Grasser[3], and B. Kaczer, [1]*imec, Belgium,* [2]*U. Leuven, Belgium,* [3]*T.U. Wien, Austria*

9:00 AM 7.3 – **How to De-pin the Fermi level of Schottky Barriers for improved contacts,** J. Robertson[1], Z. Zhang[1], and Y. Guo[2], [1]*U. Cambridge, UK,* [2]*Wuhan U., China*

9:20 AM 7.4 – **Fermi level pinning at interfaces of atomic-layer deposited $SrTiO_x$ with metals,** V. V. Afanas'ev, M. Houssa, and A. Stesmans, *U. Leuven, Belgium*

9:40 AM 7.5 – **A novel $MX_2$ MOS capacitor model to investigate CVD $MoS_2$ – $SrTiO_3$ interface,** A. Gaur[1,2], B. Groven, M. Popovici, D. H. C. Lin, I. Asselberghs, M. Heyns[1,2], and I. Radu, [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

10:00 AM Coffee Break

## Session 8: RF Device Materials

Session Chair: S. Datta

10:25 AM 8.1 *Invited* – **Future Directions in $>$ 100 GHz Devices.,** M. J. W. Rodwell, B. Markman, and Y. Fang, *UCSB*

11:00 AM 8.2 – **Measurements of Interface Trap Density on GaN MOS-HEMTs with Epitaxial MgCaO and Amorphous $Al_2O_3$ Gate Stacks by Single Pulse Charge Pumping,** S. Alghamdi[1,2], M. Si, H. Bae, H. Zhou, and P. D. Ye, [1]*Purdue U.,* [2]*King Abdulaziz U., Saudi Arabia*

11:20 AM 8.3 – **Comprehensive Study of Local Electro-Thermal Effect in $\beta$-$Ga_2O_3$ Field-Effect Transistors,** J. Noh[1], H. Bae[1], S. Alajlouni[1], K. Maize[1], M. J. Tadjer[2], A. Shakouri[1], and P. D. Ye[1], [1]*Purdue U.,* [2]*U.S. Naval Research Laboratory*

11:40 AM 8.4 – **Room Temperature Electroluminescence from Tensile-strained GeSn Lateral PIN Structures Fabricated by Nucleation-controlled Liquid-phase Crystallization,** Y. Wada, T. Hosoi, T. Shimura, and H. Watanabe, *Osaka U., Japan*

12:00 PM Adjourn for Lunch

12:00 PM – 1:30 PM Committee/Invited Speakers Luncheon

## Session 9: Resistive Memory & Ge Materials

Session Chair: M. Houssa

1:30 PM 9.1 *Invited* – **Engineering High Performance Oxide Memristors,** J. L. MacManus-Driscoll, *U. Cambridge, UK*

2:05 PM 9.2 – **Low-Temperature Ultra-Thin Epitaxial Si Cap Enabling Highly Reliable Ge MOS,** H. W. Wan[1], Y. J. Hong[1], Y. T. Cheng[1], C. K. Cheng[1], L. B. Young[1], C. T. Wu[2], J. Kwo[3], and M. Hong[1], [1]*National Taiwan U., Taiwan,* [2]*Taiwan Semiconductor Research Institute, Taiwan,* [3]*National Tsing Hua U., Taiwan*

2:25 PM 9.3 – **Engineering HfN Interface Layer in Gate Stack toward High Performance Ge nFETs,** C.-W. Liu[1], D.-B. Ruan[1], K.-S. Chang-Liao[1], S.-H. Yi[1], H.-I. Yeh[1], W.-Y. Hsu[1], and Y.-J. Lee[2], [1]*National Tsing Hua U., Taiwan,* [2]*Taiwan Semiconductor Research Institute, Taiwan*

2:45 PM Coffee Break

## Session 10: Ovonic Materials

Session Chair: D. Triyoso

3:10 PM 10.1 *Invited* – **Intermixing-protected interfacial phase-change memory to make better superlattices for future PCM,** J. Tominaga, *AIST, Japan*

3:45 PM 10.2 – **Fast and slow defects in $Ge_xSe_{1-x}$ OTS selectors,** W. Zhang, Z. Chai, and F. Hatem, *Liverpool John Moores U., UK*

4:05 PM Adjourn

## Session 11: Rump Session

Session Chair: R. M. Wallace

4:10 PM – 6:00 PM Rump Session

7:00 PM – 10:00 PM Dinner

10:00 PM – 12:00 AM Hospitality Suite

# Saturday, December 14, 2019

## Session 12: Ferroelectric $HfO_2$ Properties

Session Chair: A. C. Kummel

8:00 AM 12.1 – **'Negative Capacitance' Behavior Caused by Leaky and Trappy Ferroelectric,** Z. Liu, H. Jiang, B. Ordway, and T. P. Ma, *Yale U.*

8:20 AM 12.2 – **Polarization Enhancement in Ferroelectric/Dielectric HZO/$Al_2O_3$ Superlattice,** X. Lyu, M. Si, and P. D. Ye, *Purdue U.*

8:40 AM 12.3 – **Reduced Wake-Up Effect in $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric Capacitors with $HfO_2$ Buffer Layers,** F. Huang, Z. C. W. Yu, P. C. McIntyre, and S. S. Wong, *Stanford U.*

9:00 AM 12.4 – **Multi-States Partial Polarization Switching in Ferroelectric Hafnium Zirconium Oxide,** M. Si, X. Lyu, and P. D. Ye, *Purdue U.*

9:20 AM 12.5 – **Could we define the negative capacitance based on the viewpoint of Gibbs free energy?,** Y. Y. Zhang, X. L. Wang, X. L. Ma, J. J. Xiang, and W. W. Wang, *Chinese Academy of Sciences, China*

9:40 AM 12.6 – **DFT models of ferroelectric-paraelectric and ferroelectric-antiferroelectric boundaries in hafnium-zirconium oxides,** K. Chae[1,2], K. Cho[2], and A. C. Kummel[1], [1]*UCSD,* [2]*UT Dallas*

10:00 AM Coffee Break

## Session 13: 2D Materials

Session Chair: W. Zhu

10:20 AM 13.1 *Invited* – **Growth of Topological Insulators and Related Heterostructures,** C. L. Hinkle, *U. Notre Dame*

10:55 AM 13.2 – **Interface Dependence of Thermal Properties in Two-Dimensional $MoS_2$,** A. J. Gabourie and E. Pop, *Stanford U.*

11:15 AM 13.3 – **A new opportunity for two-dimensional van der Waals heterostructures: making steep-slope transistors,** J. Lu[1], J. Pei[1], Y. Guo[2], J. Gong[3], and H. Li[1], [1]*Tsinghua U., China,* [2]*Wuhan U., China,* [3]*Inner Mongolia U., China*

11:35 AM 13.4 – **Dual-Gate $MoS_2$ FETs with Sub-60 mV/dec Subthreshold Swing due to Charge Trapping,** P. Bolshakov[1], A. Khosravi[1], P. Zhao[1], A. Azcatl[1], G. Mirabelli[2], P. K. Hurley[2], C. L. Hinkle[1,3], R. M. Wallace[1], and C. D. Young[1], [1]*UT Dallas,* [2]*Tyndall National Institute, Ireland,* [3]*Notre Dame U.*

11:55 AM 13.5 – **Transforming Electronic and Photonic Devices Using van der Waals Metallic Alloy Contacts,** K. Xu, Z. Zhao, X. Wu, and W. Zhu, *UIUC*

12:15 PM Break

## Session 14: Wide Gap Materials

Session Chair: H. Watanabe

12:30 PM 14.1 – **Difference of dominant scattering mechanisms on n-MOS channels between a-, m-, and Si-faces 4H-SiC characterized by Hall effect measurement,** H. Hirai, T. Hatakeyama, M. Sometani, M. Okamoto, S. Harada, and H. Okumura, *AIST, Japan*

12:50 PM 14.2 – **High-temperature $CO_2$ Process for Improvement of SiC MOS Characteristics,** T. Hosoi, M. Ohsako, T. Shimura, and H. Watanabe, *Osaka U., Japan*

1:10 PM 14.3 – **Low-Temperature PEALD $SiN_x$ on GaN MIS-HEMTs with Crystalline Interfacial Layer,** S. M. Hwang[1], X. Meng[1], S. J. Kim[2], A. Ravichandran[1], A. T. Lucero[1], J. Lee[3], B. K. Hwang[4], and J. Kim[1], [1]*UT Dallas,* [2]*Kangwon National U., Korea,* [3]*Kookmin U., Korea,* [4]*Dupont*

1:30 PM 14.4 – **Dependence of Reliability of Ferroelectric $HfZrO_x$ on Crystallinity of Underlying GeSn Film,** C.-P. Chou, Y.-X. Lin, Y.-K. Huang, C.-Y. Chan, and Y.-H. Wu, *National Tsing Hua U., Taiwan*

1:50 PM Close

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# Affiliation Index