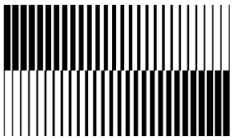

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SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology," published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author for either an oral or a poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

2019 SISC Ed Nicollian Award for Best Student Paper

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"A novel MX_2 MOS capacitor model to investigate CVD MoS_2 - $SrTiO_3$ interface"

with B. Groven, M. Popovici, D. H. C. Lin, I. Asselberghs, M. Heyns, and I. Radu

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Wednesday Evening Tutorial

Wednesday, December 16, 2020, 15:30 PST

First introduced at SISC 2008, the Wednesday Evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

Prof. Philip Wong, Haitong Li, and Weier Wan, *Stanford University*

In- and Near-Memory Computing Using 2D/3D Resistive Memories

In- and Near-Memory Computing Using 2D/3D Resistive Memories

Haitong Li, Weier Wan and H.-S. Philip Wong

Department of Electrical Engineering and Stanford SystemX Alliance, Stanford University

The growing demands of ubiquitous artificial intelligence (AI) applications call for new energy-efficient hardware solutions that can offer sustainable benefits with technology, architecture, and system advancements. As illustrated in Figure 1, we envision that 3D integrated systems with tight integration of logic and memory, through end-to-end technology-system co-optimization, will be the key enabler going forward [1]. Particularly, high-density, on-chip non-volatile memories (NVMs) play an important role [2], enabling three major features: (1) high-capacity, high-bandwidth on-chip data storage, (2) near-memory computing capabilities with domain-specific accelerators on chip, (3) in-memory computing capabilities utilizing unique device properties. In this tutorial, we will discuss on the essential characteristics of in-memory and near-memory computing using 2D and 3D vertical resistive RAM (RRAM).

We start with a high-level overview and discussion of both application and technology trends towards energy-efficient AI hardware. Then, at device level, we will focus on the RRAM technologies and provide backgrounds from device physics and operations to 3D structures and integration. At circuit and architecture level, we will dive into the basic ideas, designs, and system analysis of leveraging RRAM for near-memory and in-memory computing, using various case studies.

The new design space created by the logic-memory integration with RRAMs and other NVMs on chip can provide new insights and augment domain-specific accelerator optimizations where computations need to be close to memories [3]. Utilizing the device-level and circuit-level properties allows us to move neural network computations into RRAMs [4], and further support brain-inspired learning models with native compute kernels in 3D structures [5].

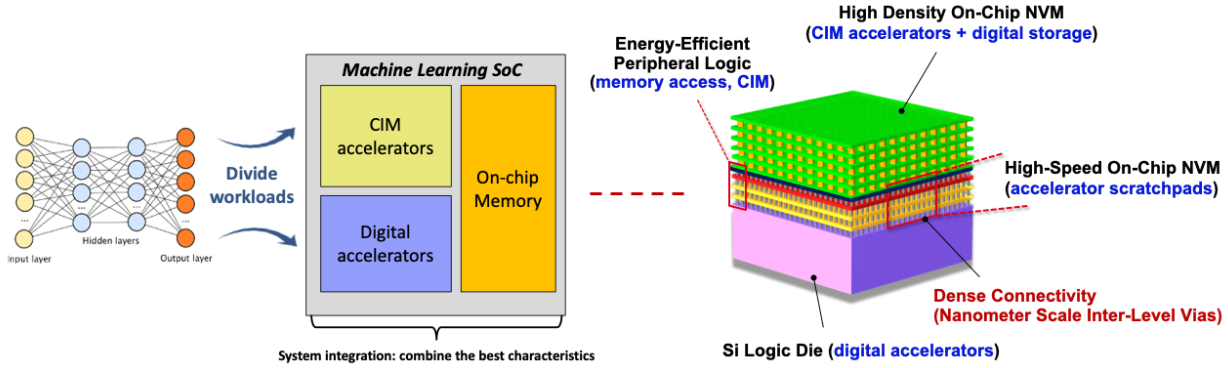

Figure 1. End-to-end technology-system co-optimization with on-chip NVM (e.g., RRAM) for energy-efficient machine intelligence.

References:

[1] M.M. Aly, *et al.*, "The N3XT approach to energy-efficient abundant-data computing," *Proc. IEEE*, 2018
[2] H.-S. P. Wong, *et al.*, "Memory leads the way to better computing," *Nature Nanotech.*, 2015
[3] H. Li, *et al.*, "On-chip memory technology design space explorations for mobile deep neural network accelerators," *DAC*, 2019
[4] W. Wan *et al.*, "A 74 TMACS/W CMOS-RRAM neurosynaptic core with dynamically reconfigurable dataflow and in-situ transposable weights for probabilistic graphical models," *ISSCC*, 2020
[5] H. Li., *et al.*, "Hyperdimensional computing with 3D VRRAM in-memory kernels: Device-architecture co-design for energy-efficient, error-resilient language recognition," *IEDM*, 2016

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IEEE ELECTRON DEVICES SOCIETY

Conference Agenda Overview

Wednesday, December 16, 2020

Session 1: Ferroelectrics	11:00 – 12:50
Session 2: 2D Materials	13:15 – 15:10
Session 3: Wednesday Evening Tutorial	15:30 – 17:00
Session 4: Advanced Semiconductor Devices	17:25 – 19:40

Thursday, December 17, 2020

Session 5: 2D Materials	6:00 – 7:40
Session 6: Interfaces	8:05 – 9:25
Session 7: Poster Session I Presentation	9:25 – 9:45
Session 7: Poster Session I Discussion	10:05 – 11:05
Session 8: Wide Bandgap Materials	11:35 – 13:10
Session 9: Advanced Electronics	13:35 – 15:10
Session 10: Ferroelectrics	15:35 – 16:55
Session 11: Reliability and Stability	17:20 – 19:20

Friday, December 18, 2020

Session 12: Interfaces and Defects	6:00 – 7:40
Session 13: Semiconductor Memory	8:05 – 9:40
Session 14: Wide Bandgap Materials	11:00 – 12:35
Session 15: 2D Materials	13:00 – 14:40
Session 16: Wide Bandgap Materials	15:05 – 16:40
Session 17: Poster Session II Presentation	16:40 – 17:00
Session 17: Poster Session II Discussion	17:20 – 18:20

All times are PST (Pacific Standard Time)

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Wednesday, December 16, 2020

Session 1: Ferroelectrics

Session Chair: M. Frank

11:00 Introduction

11:15 1.1 *Invited* – **Interface Effects on the Reliability of Hafnium Oxide-Based Ferroelectric Memories,** P. C. McIntyre , *Stanford U.*

11:50 1.2 – **Ultrathin PVD-Grown In_2Se_3 Ferroelectric Semiconductor Field-Effect Transistors,** D. Zheng, M. Si, Z. Zhang, and P. D. Ye, *Purdue U.*

12:10 1.3 – **DFT models on interfaces of ferroelectric and antiferroelectric hafnium-zirconium oxides to dielectric oxides and semiconductor,** K. Chae[1,2], A. C. Kummel[1], and K. J. Cho[2], [1]*UCSD,* [2]*UT Dallas*

12:30 1.4 – **A Reliability Study of Thickness Dependence of HfO_2-based 3D-FeRAM Cell,** O. Maher, H. Jiang, Z. Liu, and T. P. Ma, *Yale U.*

12:50 Coffee Break

Session 2: 2D Materials

Session Chair: P. D. Ye

13:15 2.1 *Invited* – **Van der Waals Integration beyond 2D Materials,** X. Duan, *UCLA*

13:50 2.2 – **Electronic and Photonic Devices Based on Monolayer Ternary Telluride Heterostructures Synthesized by Chemical Vapor Deposition,** K. Xu, J. Kang, Z. Hao, and W. Zhu, *UIUC*

14:10 2.3 – **Magnetism and Magnetic Dopant Solubility in Transition Metal Dichalcogenides,** R. Younas[1], G. Zhou[1], S. Tawari[2], M. L. Van de Put[2], W. G. Vandenberghe[2], and C. L. Hinkle[1], [1]*U. Notre Dame,* [2]*UT Dallas*

14:30 2.4 – **Interface Chemistry Study of Ni and Ag contacts on MoS_2,** X. Wang, S. Yeoul Kim, and R. M. Wallace, *UT Dallas*

14:50 2.5 – **Improved Low-Temperature Growth of 3D Semiconductors Using 2D Intermediate Layers,** G. Zhou and C. L. Hinkle, *U. Notre Dame*

15:10 Coffee Break

All times are PST (Pacific Standard Time)

Session 3: Tutorial

Session Chair: W. Zhu

15:30 – 17:00 *Tutorial* – **In- and Near-Memory Computing Using 2D/3D Resistive Memories,** H.-S. P. Wong, H. Li, and W. Wan, *Stanford U.*

Session 4: Advanced Semiconductor Devices

Session Chair: Y. Lee

17:25 4.1 *Invited* – **Progress and issue in oxide semiconductors,** H. Hosono[1,2], [1]*Tokyo Institute of Technology, Japan,* [2]*National Institute for Materials Science, Japan*

18:00 4.2 – **Nanoscale comparison of bias dependent carrier distributions in mechanically exfoliated WSe_2/SiO_2 and suspended WSe_2 by scanning nonlinear dielectric microscopy,** K. Takano, K. Yamasue, T. Kato, T. Kaneko, and Y. Cho, *Tohoku U., Japan*

18:20 4.3 – **Tellurium Nanowire Gate – All-Around MOSFETs for Sub-5 nm Applications,** Y. Yin[1], J. Robertson[2], and Y. Guo[1,2], [1]*Wuhan U., China,* [2]*Cambridge U., UK*

18:40 4.4 – **Neuromorphic characteristics of MoS_2-based CBRAM using thin Ti layer for future artificial intelligence applications,** S. Maikap[1,2], S. Ginnaram[1], M. Seal[1], and A. Senapati[1], [1]*Chang Gung U., Taiwan,* [2]*Keelung Chang Gung Memorial Hospital, Taiwan*

19:00 4.5 – **Negative Differential Resistance in Photocurrent Across a Vertical van der Waals Heterostructure Driven by Energy Transfer,** M. Dandu and K. Majumdar, *IIS Bangalore, India*

19:20 4.6 – **Surface electronic structure of strained $Si_{1-x}Ge_x$ layers grown on Ge(001) and Si(001),** H. W. Wan[1], Y. T. Cheng[1], C. K. Cheng[1], C. P. Cheng[2], J. Kwo[3], T. W. Pi[4], and M. Hong[1], [1]*National Taiwan U., Taiwan,* [2]*National Chiayi U., Taiwan,* [3]*National Tsing Hua U., Taiwan,* [4]*National Synchrotron Radiation Research Center, Taiwan*

19:40 End

Thursday, December 17, 2020

Session 5: 2D Materials

Session Chair: W. Vandenberghe

6:00 Introduction

6:05 5.1 *Invited* – **Insulators for 2D Nanoelectronics: Expectations vs. Reality,** Y. Y. Illarionov[1,2], T. Knobloch[1], and T. Grasser[1], [1]*TU Wien, Austria,* [2]*Ioffe Institute, Russia*

6:40 5.2 – **300 mm wafer level WS_2 p-MOS capacitor Characterization, Simulation, and Analysis,** V. Mootheri[1,2], A. Gaur[1,2], A. Okuyama[3], Q. Smets[1], T. Schram[1], I. Asselberghs[1], M. Heyns[1,2], I. Radu[1], and D. H. C. Lin[1], [1]*imec, Belgium,* [2]*U. Leuven, Belgium,* [3]*Sony Semiconductor Solutions, Japan*

7:00 5.3 – **Band Alignment at Monolayer WS_2/SiO_2 Interface: Impact of the Layer Transfer,** G. Delie[1], D. Chiappe[2,3], I. Asselberghs[2], C. Huyghebaert[2], I. Radu[2], S. Banerjee[2], B. Groven[2], S. Brems[2], and V. V. Afanas'ev[1], [1]*U. Leuven, Belgium,* [2]*imec, Belgium,* [3]*ASM Microchemistry, Finland*

7:20 5.4 – **Stoner ferromagnetism in cadmium dihalides,** R. Meng[1], M. Houssa[1], K. Iordanidou[2], V. V. Afanas'ev[1], and A. Stesmans[1], [1]*U. Leuven, Belgium,* [2]*U. Oslo, Norway*

7:40 Coffee Break

Session 6: Interfaces

Session Chair: A. Stesmans

8:05 6.1 – **Liquid-Gated Silicon Nanowire Field-Effect Transistors Covered with Ultrathin Diamond-Like Tetrahedral Amorphous Carbon,** N. Boichuk[1], Y. Kutovyi[1], J. Lie[1], G. Beltramo[1], V. Weihnacht[2], and S. Vitusevich[1], [1]*Forschungszentrum Jülich, Germany,* [2]*Fraunhofer Institute, Germany*

8:25 6.2 – **Alternatives to Ga in In-Ga-Zn-O_4 amorphous oxide semiconductors,** Z. Zhang[1], Y. Guo[2], and J. Robertson[1], [1]*Cambridge U., UK,* [2]*Swansea U., UK*

8:45 6.3 – **Ab-initio Calculation of Quantum Tunneling Property of Thin Oxide Josephson Junctions Using Density Functional Theory and Machine-Learning,** C. E. Kim, K. G. Ray, and V. Lordi, *Lawrence Livermore National Laboratory*

9:05 6.4 – **Origin of Apparent Fermi Level De-Pinning of Metal Silicides/Si Interfaces,** J. Robertson[1], Z. Zhang[1], and Y. Guo[2], [1]*Cambridge U., UK,* [2]*Swansea U., UK*

Session 7: Poster Session I

Session Chair: W. Vandenberghe

9:25 7.1 – **Impact of termination on Fermi level pinning at rare-earth arsenide/GaAs interfaces,** Z. Zhang[1], Y. Guo[2], and J. Robertson[1], [1]*Cambridge U., UK,* [2]*Swansea U., UK*

9:26 7.2 – **Mobility of Near Surface InGaAs/InP Quantum Wells,** L. Södergren, N. S. Garigapati, and E. Lind, *Lund U., Sweden*

9:27 7.3 – **Fast Low Temperature Oxidation of 4H-SiC,** G. Fleckl, G. Pfusterschmied, and U. Schmid, *TU Wien, Austria*

9:28 7.4 – **Study on Ti:AlO_x as high-κ dielectric for MISHEMTs,** S. Seidel, A. Schmid, N. Siebdrath, and J. Heitmann, *TU Bergakademie Freiberg, Germany*

9:29 7.5 – **On the origin of stochasticity in Cu/SiO_2/W CBRAM devices: model and experimental study,** F. Maudet[1], V. Deshpande[1], and C. Dubourdieu[1,2], [1]*Helmholtz-Zentrum Berlin, Germany,* [2]*Free U. Berlin, Germany*

9:30 7.6 – **Modification of chemical oxide passivation of silicon by ultrahigh-vacuum low-temperature treatments,** Z. J. Rad[1], K. Chen[2], J.-P. Lehtiö[1], I. Mack[2], E. Vuorinen[1], V. Vähänissi[2], M. Kuzmin[1], M. Punkkinen[1], P. Laukkanen[1], H. Savin[2], and K. Kokko[1], [1]*U. Turku, Finland,* [2]*Aalto U., Finland*

9:31 7.7 – **Humidity-mediated oxidation of hexanethiol-passivated Ge(100) surfaces,** S. Garvey[1], A. Serino[2], J. D. Holmes[1], N. Draeger[2], and B. Long[1], [1]*U. College Cork, Ireland,* [2]*Lam Research*

9:32 7.8 – **Electron spin relaxation and coherence of Pb-centers at the Si/SiO_2 interface in Silicon nanowires,** M. Fanciulli[1,2], M. Belli[2], and R. de Sousa[3], [1]*U. Milano-Bicocca, Italy,* [2]*IMM-CNR, Italy,* [3]*U. Victoria, Canada*

9:33 7.9 – **Electrical measurements of gate-controlled diodes and MOS capacitors irradiated with ^{60}Co-γ,** P. Asenov, P. Assiouras, A. Kyriakis, and D. Loukas, *NCSR Demokritos, Greece*

All times are PST (Pacific Standard Time)

9:34 7.10 – **Fabrication of Biologically Sensitive Si Nanowire Field-Effect-Transistors applied to Electrical Label-Free DNA Hybridization Detection,** R. Midahuen[1], T. Magis[1], V. Mathieu[1], F. Laulagnet[1], J. A. Dallery[3], B. Previtali[1], V. Stambouli[2], and S. Barraud[1], [1]*CEA-LETI, France,* [2]*CNRS, France,* [3]*VISTEC Electron Beam, Germany*

9:35 7.11 – **Effect of Electron Affinity on ALD MI2M Resonant Tunneling Rectifiers,** S. B. Tekin, N. Sedghi, S. Hall, P. R. Chalker, and I. Z. Mitrovic, *U. Liverpool, UK*

9:36 7.12 – **Metal/HfO_2/SiO_x/Si and Metal/HfO_2/Metal memory cell stacks,** S. Kalem[1], S. B. Tekin[2], E. Kaya[3], E. Jalaguier[4], R. Roelofs[5], S. Yildirim[6], and O. Yavuzcetin[7], [1]*Bahcesehir U., Turkey,* [2]*U. Liverpool, UK,* [3]*TUBITAK-BILGEM, Turkey,* [4]*CEA-LETI, France,* [5]*ASM, Belgium,* [6]*Istanbul U., Turkey,* [7]*U. Wisconsin*

9:37 7.13 – **How ALD gas phase chemistry changes the oxidation state and conductivity of TiO_2 thin films,** A. Babadi and P. C. McIntyre, *Stanford U.*

9:38 7.14 – **Toward electronic isolation of immune cells from blood for COVID immunity testing,** S. Yosinski, P. Han, Z. A. Kobos, R. Chaudhury, J. S. Lee, T. M. Fahmy, and M. A. Reed, *Yale U.*

9:39 7.15 – **Precursor Comparison for Selective Low Resitivity Selective Ru Atomic Layer Deposition,** V. Wang, M. Breeden, and A. C. Kummel, *UCSD*

9:40 7.16 – **Selective Pulsed Chemical Vapor Deposition of TiO_2/Al_2O_3 Nanolaminates on Si and SiO_2 in Preference to SiCOH,** J. Huang, Y. Cho, and A. C. Kummel, *UCSD*

9:41 7.17 – **Bias-Enhanced Atomic Layer Annealing for the Deposition of High-Quality Aluminum Nitride Thin Films On Silicon,** A. J. McLeod, S. T. Ueda, and A. C. Kummel, *UCSD*

9:42 7.18 – **High Tunneling Electroresistance Ratio in Ferroelectric tunneling Junctions based on Hafnium Zirconium Oxide,** H. Ryu and W. Zhu, *UIUC*

9:43 7.19 – **The role of dielectric screening and remote phonon scattering in monolayer MoS_2,** M. L. Van de Put[1], G. Gaddemane[2], S. Gopalan[1], and M. V. Fischetti[1], [1]*UT Dallas,* [2]*imec, Belgium*

9:44 7.20 – **Effect of Deposition Temperature on 5 nm Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Capacitors,** Z. Yu, F. Huang, W. Tsai, and P. C. McIntyre, *Stanford U.*

9:45 7.21 – **Effect of WRITE pulse width on data retention properties of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ MIM capacitors,** J. Mohan[1], S. J. Kim[2], H. Hernandez-Arriaga[1], Y. C. Jung[1], C. D. Young[1], S. R. Summerfelt[3], and J. Kim[1], [1]*UT Dallas,* [2]*Kangwon National U., Korea,* [3]*Texas Instruments*

9:45 – 10:05 Coffee Break and Setup Gather Town

10:05 – 11:05 Poster Discussion at Gather Town

Session 8: Wide Bandgap Materials

Session Chair: J. Rozen

11:35 8.1 *Invited* – **Discovery and transistor applications of polarization-induced 2D hole gases at polar semiconductor heterojunctions,** D. Jena, R. Chaudhuri, S. Bader, K. Nomoto, and H. Xing, *Cornell U.*

12:10 8.2 – **Capacitance and Transport Properties of GaN/ScAlN/GaN Heterostructure Barrier Diodes,** T. Maeda, J. Casamento, K. Nomoto, H. G. Grace, and D. Jena, *Cornell U.*

12:30 8.3 – **Electronic properties of epitaxial NbN/GaN interfaces,** J. G. Wright[1], G. Khalsa[1], T. Yu[2], V. Strocov[2], H. G. Xing[1], and D. Jena[1], [1]*Cornell U.,* [2]*Paul Scherrer Institute, Switzerland*

12:50 8.4 – **Why an Ideal GaN Fe-HEMT is Hard to Achieve?,** Z. Lin, M. Si, J. Noh, X. Lyu, and P. D. Ye, *Purdue U.*

13:10 Coffee Break

Session 9: Advanced Electronics

Session Chair: J. Wrench

13:35 9.1 *Invited* – **Reliability Physics of Post-Moore Era Electronic Devices,** M. A. Alam, *Purdue U.*

14:10 9.2 – **Deposition Mechanism of Sub 1nm EOT Bilayer Gate Oxides on Inert Carbon Surfaces Via Lateral growth of Al_2O_3 Nucleation Layers,** Z. Zhang[1], C. Kuo[1], J. Spiegelman[1], H. Kashyap[1], G. Pitner[2], M. Passlack[2], Q. Lin[3], H.-S. P. Wong[3], A. C. Kummel[1], and P. Bandaru[1], [1]*UCSD,* [2]*TSMC,* [3]*Stanford U.*

14:30 9.3 – **Selective Pulsed CVD of HfO_2/TiO_2 Nanolaminate for Nanoscale Patterning,** Y. Cho, J. Huang, C. Ahles, and A. C. Kummel, *UCSD*

14:50 9.4 – **Uncovering High Mobility Post-Cu Interconnect Materials Through Screening Thousands of Candidate Materials,** E. R. Antoniuk, A. Ramdas, and E. J. Reed, *Stanford U.*

15:10 Coffee Break

Session 10: Ferroelectrics

Session Chair: P. McIntyre

15:35 10.1 – **Charging-induced Stabilization of Ferroelectric Orthorhombic HfO_2 Phase; Key Growth Processes based on First-principles Study,** T. Nakayama[1], K. Arai[1], Y. Shiraishi[1], R. Nagasawa[1], M. Araidai[2], and K. Shiraishi[2], [1]*Chiba U., Japan,* [2]*Nagoya U., Japan*

15:55 10.2 – **Crystalline Phase Formation and Transition Kinetics in Ferroelectric HfO_2 Thin Films,** T. Cui[1], M. Li[2], S. S. Lee[3], Y. Fan[1], T. Fister[3], J. Liu[1], P. Fenter[3], and X. Li[1], [1]*Shanghai Jiao Tong U., China,* [2]*Rutgers U.,* [3]*Argonne National Laboratory*

16:15 10.3 – **Remnant Polarization and Junction Current Enhancement of Ferroelectric $HfZrO_2$ with Molybdenum Capping Electrode,** K.-Y. Hsiang[1,2], K.-T. Chen[1,3], C.-Y. Liao[1], T.-M. Wu[1], J.-H. Liu[1], S.-H. Chang[1], F.-C. Hsieh[1], S.-H. Chiang[1], H. Liang[1], Y.-D. Lin[4], P.-C. Yeh[4], C.-Y. Wang[4], H.-Y. Yang[4], P.-J. Tzeng[4], S. T. Chang[3], Y.-T. Tang[5], and M. H. Lee[1]., [1]*National Taiwan Normal U., Taiwan,* [2]*National Chiao Tung U., Taiwan,* [3]*National Chung Hsing U., Taiwan,* [4]*Industrial Technology Research Institute, Taiwan,* [5]*Taiwan Semiconductor Research Institute, Taiwan*

16:35 10.4 – **Possibility of Above 20-nm-Thick $Hf_xZr_{1-x}O_2/ZrO_2$ and $Hf_xZr_{1-x}O_2/HfO_2$ Bilayers for High Polarization and Breakdown Voltage,** T. Onaya[1,2,3,4], T. Nabatame[2], M. Inoue[2], Y. C. Jung[3], H. Hernandez-Arriaga[3], J. Mohan[3], H. S. Kim[3], N. Sawamoto[5], T. Nagata[2], J. Kim[3], and A. Ogura[1,5], [1]*Meiji U., Japan,* [2]*NIMS, Japan,* [3]*UT Dallas,* [4]*JSPS, Japan,* [5]*MREL, Japan*

16:55 Coffee Break

Session 11: Reliability and Stability

Session Chair: S. Takagi

17:20 11.1 – **Nanoscale Evaluation of DC Bias Stress Induced Interface Defect Density of a High-κ/SiO_2/Si Gate Stacks using Time-Resolved Scanning Nonlinear Dielectric Microscopy,** K. Suzuki, K. Yamasue, and Y. Cho, *Tohoku U., Japan*

17:40 11.2 – **Revision of conductance method for evaluating interface state density at MFIS interfaces,** T.-E. Lee, Z. Lin, K. Toprasertpong, M. Takenaka, and S. Takagi, *U. Tokyo, Japan*

18:00 11.3 – **Origin of low channel mobility of 4H-SiC(0001)/SiO_2 MOSFETs: Impact of interfacial carbon-carbon defects,** Z. Wang[1], Z. Zhang[2], Y. Guo[1], and J. Robertson[2], [1]*Wuhan U., China,* [2]*Cambridge U., UK*

18:20 11.4 – **Microscopic capacitance-voltage characteristics measurement of a SiO_2/SiC MOS structure by time-resolved scanning nonlinear dielectric microscopy,** K. Yamasue and Y. Cho, *Tohoku U., Japan*

18:40 11.5 – **ALD-TiN metal gate on in-situ prepared Al_2O_3/Y_2O_3/n-GaAs with high-temperature thermal stability and low interface state density,** Y. H. Lin[1], J. Liu[1], Y. J. Hong[1], H. W. Wan[1], L. B. Young[1], J. Kwo[2], and M. Hong[1], [1]*National Taiwan U., Taiwan,* [2]*National Tsing Hua U., Taiwan*

19:00 11.6 – **Enhanced Reliability and Uniformity for Ge pMOSFET with Low Temperature Supercritical Fluid Treatment,** D.-B. Ruan[1], K.-S. Chang-Liao[1], J.-S. Li[1], Z.-Q. Hong[1], G.-T. Liu[1], and P.-T. Liu[2], [1]*National Tsing Hua U., Taiwan,* [2]*National Chiao Tung U., Taiwan*

19:20 End

Friday, December 18, 2020

Session 12: Defects and Interfaces

Session Chair: C. Fenouillet-Beranger

6:00 Announcements

6:05 12.1 *Invited* – **Discovery and Understanding of Single-Atom Memory Effect in 2D Atomic Sheets,** D. Akinwande, *UT Austin*

6:40 12.2 – **Static charge formation in Si/high-κ material interfaces,** J.-P. Lehtiö[1], Z. J. Rad[1], S. Granroth[1], M. Yasir[1], M. Punkkinen[1], R. Punkkinen[1], H.-P. Hedman[1], J. P. Rueff[2], P. Laukkanen[1], and K. Kokko[1], [1]*U. Turku, Finland,* [2]*SOLEIL Synchrotron, France*

7:00 12.3 – **Nature of Mobility Reducing Defects in SiC MOSFETs,** J. Robertson[1], Z. Zhang[1], and Y. Guo[2], [1]*Cambridge U., UK,* [2]*Swansea U., UK*

7:20 12.4 – **Enhancing the Quality of Low Temperature SiO_2 by Atomic Hydrogen Exposure for Excellent NBTI Reliability,** J. Franco[1], J.-F. de Marneffe[1], A. Vandooren[1], Y. Kimura[1], L. Nyns[1], Z. Wu[1,2], A.-M. El-Sayed[3], M. Jech[3], D. Waldhoer[3], D. Claes[1,2], H. Arimura[1], L.-Å. Ragnarsson[1], V. V. Afanas'ev[2], A. Stesmans[2], N. Horiguchi[1], D. Linten[1], T. Grasser[3], and B. Kaczer[1], [1]*imec, Belgium,* [2]*U. Leuven, Belgium,* [3]*TU Wien, Austria*

7:40 Coffee Break

Session 13: Semiconductor Memory

Session Chair: A. Kummel

8:05 13.1 *Invited* – **65K-RRAM-Array Analog Conductance Relaxation Characterization For Neural Network Inference,** W. Wan and H.-S. P. Wong, *Stanford U.*

8:40 13.2 – **Atomic-Layer-Deposited Nanometer Thick In_2O_3 1T1R FET with High $I_{ON}/I_{OFF} > 10^{10}$ at V_{GS}=0 V, Large Memory Window > 10 V and Deep Sub-60 mV/dec Subthreshold Slope,** M. Si, Z. Lin, X. Lyu, and P. D. Ye, *Purdue U.*

9:00 13.3 – **Modeling of Temperature Distribution in 2D MoS_2-based Non-volatile Resistance Switching Devices,** Y. Huang, X. Wu, R. Ge, D. Akinwande, and J. C. Lee, *UT Austin*

9:20 13.4 – **Erase Behavior of Charge Trap Flash Memory Devices using High-k Dielectric as Blocking Oxide Liner,** S. Ramesh, A. Ajaykumar, J. Bastos, L. Breuil, A. Arreghini, L. Nyns, J.-Ph. Soulié, L.-Å. Ragnarsson, F. Schleicher, N. Jossart, J. Stiers, G. Van den bosch, and M. Rosmeulen, *imec, Belgium*

9:40 Coffee Break

10:05 – 10:35 TPC Committee Meeting

Session 14: Wide Bandgap Materials

Session Chair: C. Hinkle

11:00 14.1 *Invited* – **Dielectric–Diamond Interfaces,** Y. Yang, Y. Yao, X. Wang, F. A. Koeck, and R. J. Nemanich, *Arizona State U.*

11:35 14.2 – **Single and Multi-fin Normally-Off Lateral β-Ga_2O_3 Transistors on (010) Ga_2O_3 Substrates with Threshold Voltage Modulation by Fin Width Design,** K. Smith, E. Long, W. Li, K. Nomoto, D. Jena, and H. G. Xing, *Cornell U.*

11:55 14.3 – **Dynamic Behavior of Nitrogen-Implanted Ga_2O_3 in β-Ga_2O_3 Schottky Barrier Diodes,** W. Li[1,2], B. Cromer[1], K. Smith[1], K. Nomoto[1], N. Hendricks[3], A. Green[4], K. Chabak[4],D. Jena[1], and H. G. Xing[1], [1]*Cornell U.,* [2]*UC Berkeley,* [3]*UCSB,* [4]*Air Force Research Laboratory*

12:15 14.4 – **Anomalously Low Dynamic On-resistance in Ga_2O_3 Trench-MOS Schottky Barrier Diodes: Role of Sidewall Interface Trapping,** W. Li, K. Nomoto, Z. Hu, D. Jena, and H. G. Xing, *Cornell U.*

12:35 Coffee Break

Session 15: 2D Materials

Session Chair: T. Gougousi

13:00 15.1 – **Magnetic order and critical temperature of substitutionally doped monolayer TMDs,** S. Tiwari[1,2], M. L. Van de Put[1], B. Soree[2], and W. G. Vandenberghe[1], [1]*UT Dallas,* [2]*imec, Belgium*

13:20 15.2 – **Telluride Superlattices Grown by Chemical Vapor Deposition: Toward Spatial Modulation of Bandgaps,** Z. Hao and W. Zhu, *UIUC*

13:40 15.3 – **Demonstration of High Edge Conduction in Tellurene Nanoribbon Transistor,** Z. Zhang, C. Niu, M. Si, J. Li, G. Qiu, and P. D. Ye, *Purdue U.*

14:00 15.4 – **Contact Engineering with Self-assembled Monolayers in $MoTe_2$ Transistors,** Z. Zhao, S. Li, Y. Diao, C. Schroeder, and W. Zhu, *UIUC*

All times are PST (Pacific Standard Time)

14:20 15.5 – **A Computational Study of Hole Transport in Hexagonal Boron Nitride Monolayers,** M. M. Khatami[1,2], M. L. Van de Put[2], M. K. Moravvej-Farshi[1], and W. G. Vandenberghe[2], [1]*Tarbiat Modares U., Iran,* [2]*UT Dallas*

14:40 Coffee Break

Session 16: Wide Bandgap Materials

Session Chair: R. Nemanich

15:05 16.1 *Invited* – **MOCVD based dielectrics on GaN: Impact of growth conditions, composition and polarity,** I. Sayed and U. Mishra, *UCSB*

15:40 16.2 – **Initial Studies of Bias Temperature Instability of Vertical III-V Nanowire MOSFETs,** M. Hellenbrand[1], V. Putcha[2], O.-P. Kilpi[1], J. Franco[2], and L.-E. Wernersson[1], [1]*Lund U., Sweden,* [2]*imec, Belgium*

16:00 16.3 – **Atomic Layer Deposition of Hafnium Oxide on InAs: new insight by time-resolved in situ studies,** G. D'Acunto, A. Troian, E. Kokkonen, F. Rehman, Y. P. Liu, E. Lind, J. Schnadt, and R. Timm, *Lund U., Sweden*

16:20 16.4 – **Implementing a nanowire-based optoelectronic recurrent neural circuit from the bee brain,** D. O. Winge[1], S. Limpert[1], H. Linke[1], M. T. Borgström[1], B. Webb[2], S. Heinze[1], and A. Mikkelsen[1], [1]*Lund U., Sweden,* [2]*U. Edinburgh, UK*

Session 17: Poster Session II

Session Chair: W. Zhu

16:40 17.1 – **First-principles calculations on the atomic and electronic structures at the GaN/$(Al_2O_3)_{1-x}(SiO_2)_x$ interfaces,** K. Chokawa, K. Shiraishi, and A. Oshiyama, *Nagoya U., Japan*

16:41 17.2 – **Process optimization and thermal stability study for hydrogen-terminated nitrided 4H-SiC(0001) surface,** K. Murata, K. Betsuyaku, and H. Tsuchida, *CRIEPI, Japan*

16:42 17.3 – **Explicit Gain Equation for Single Crystalline Silicon Nanowire Photoconductors,** J. J. He and Y. P. Dan, *Shanghai Jiao Tong U., China*

16:43 17.4 – **Effect of Nitrogen Impurity Atoms at Fe/MgO Interface on Perpendicular Magnetic Anisotropy Energy,** Y. Ogawa[1], M. Araidai[1], T. Endoh[2], and K. Shiraishi[1,2], [1]*Nagoya U., Japan,* [2]*Tohoku U., Japan*

16:44 17.5 – **Consequential effect of MWA and dielectric insertion on schottky barrier height in Ge MIS structure,** A. Kumar, P. Divya[2], and W. H. Lee, *National Cheng Kung U., Taiwan*

16:45 17.6 – **The study of sub threshold characteristics of 4-H SiC NMOSFET after ionizing dose for space application,** W. Ali, Y. Qingkui, C. Shuang, and W. He, *China Academy of Space Technology, China*

16:46 17.7 – **Novel Methods for Effective Design for Reliability Practices in SEMI Industries,** S. P. Panchangam, A. K. Rajendran, K. Gowdaru, and P. Kolgiri, *Lam Research, India*

16:47 17.8 – **Atomic Layer Deposited Metal Oxide Bilayers for Metal-Insulator-Semiconductor Photovoltaics,** B. E. Davis and N. C. Strandwitz, *Lehigh U.*

16:48 17.9 – **Exploiting Fixed Charge to Control Schottky Barrier Height in Si|Al_2O_3|MoO_x - based Tunnel Diodes,** B. M. Garland, B. E. Davis, and N. C. Strandwitz, *Lehigh U.*

16:49 17.10 – **Novel Revelations on Silicon Carbide Wet Oxidation,** G. H. S. Dartora, P. Silveira, and F. C. Stedile, *UFRGS, Brazil*

16:50 17.11 – **Critical inspection of semiconductor interfaces via camera-less terahertz 3D imaging,** A. Rahman, *Applied Research & Photonics*

16:51 17.12 – **Engineering Ag-based ZnO Thin Films to Reduce V_{th} Variability in Filament-type Threshold Switching Selectors for 3D Cross-point Memory Application,** A. Sahota, H. S. Kim, J. Mohan, and Y. C. Jung, *UT Dallas*

16:52 17.13 – **The effects of annealing graphene in nitric oxide – doping and etching,** G. K. Rolim, G. V. Soares, H. I. Boudinov, and C. Radtke, *UFRGS, Brazil*

16:53 17.14 – **Electron transport in topological semi-metal Molybdenum Phosphide,** S. Kumar and R. Sundararaman, *Rensselaer Polytechnic Institute*

16:54 17.15 – **Tunable plasmonic hot carrier dynamics in noble metal alloys,** A. Habib and R. Sundararaman, *Rensselaer Polytechnic Institute*

16:55 17.16 – **Electroforming Polarity on Bilayer Self-Selective RRAM for Energy Efficient High-Density Crossbar Array Applications,** Y.-C. Chen, *Northern Arizona U.*

16:56 17.17 – **Novel Layered Dielectrics: a First Principles Study of 32 large gap van der Waals materials,** M. Rostami Osanloo, M. L. Van de Put, A. Saadat, and W. G. Vandenberghe, *UT Dallas*

16:57 17.18 – **Ferroelectric HZO capacitor with W/TiN bottom electrode with no wakeup,** H. Kashyap[1], M. S. Kavrik[1], C. Kuo[1], T. Weiss[1], A. Yadav[2], and A. C. Kummel[1], [1]*UCSD,* [2]*Applied Materials*

16:58 17.19 – **Low Resistivity Titanium Nitride Thin Film Fabricated by Atomic Layer Deposition on Silicon,** C. Kuo[1], V. Wang[1], Z. Chang[1], H. Kashyap[1], D. Alvarez[2], and A. C. Kummel[1], [1]*UCSD,* [2]*RASIRC*

16:59 17.20 – **Synthesis of Atomically Thin Ternary Telluride Alloys via Sodium Chloride,** J. Kang and W. Zhu, *UIUC*

17:00 17.21 – **Probing the Thermal Transport in h-BN/MoS_2/h-BN Heterostructure,** F. Ye[1], P. X.-L. Feng[1], and X. Zhang[2], [1]*Case Western Reserve U.,* [2]*Stevens Institute of Technology*

17:00 – 17:20 Coffee Break and Setup Gather Town

17:20 – 18:20 Poster Discussion at Gather Town

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