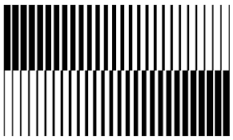

SISC 2021

52nd IEEE Semiconductor Interface Specialists Conference

December 8–11, 2021
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SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology," published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author for either an oral or a poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

2020 SISC Ed Nicollian Award for Best Student Paper

John Wright

Cornell University

"Electronic properties of epitaxial NbN/GaN interfaces"
with G. Khalsa, T. Yu, V. Strocov, H. G. Xing, and D. Jena

SISC T. P. Ma Award for Best Student Poster

In 2021, the SISC added an award for the best student poster in honor of Professor T. P. Ma, Yale University. Professor Ma was an internationally recognized pioneer for his contributions to semiconductor science and technology — in particular, breakthroughs in advanced gate dielectrics, which paved the path for high-k dielectrics and extended the scaling of CMOS technology. His research also generated fundamental and lasting impacts on many other applied physics fields, notably ferroelectrics and ionizing radiation sciences.

The SISC T. P. Ma Award will be presented to the lead student author for a poster presentation. The winner will be chosen by members of the technical program committee at the end of the SISC. The award will consist of a plaque, an honorarium, and a permanent mention on the conference web site.

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Wednesday Evening Tutorial

Wednesday, December 8, 2021, 8:00 PM

First introduced at SISC 2008, the Wednesday Evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

Prof. Robert M. Wallace, *UT Dallas*

Physical Characterization of Advanced Device Materials

A variety of materials are now under investigation for advanced device concepts and applications. In addition to establishing materials properties in the context of device physics and potential performance, an understanding of the integration constraints and the impact on the materials interfaces must also be addressed, as interfaces with contacts and dielectrics dominate device characteristics. This tutorial will focus on the surface/interface physical characterization aspects of such advanced device materials, such as high-mobility and 2D materials, complex oxides, and nitrides, as well as the role of impurities and defects in these materials. Topics in advanced device materials development and metrology to be covered include:

1. Detection limits of characterization techniques
2. In-situ vs. ex-situ characterization
3. Surface and interface analysis methods
4. Electron and ion mass spectrometry methods

The physics of the characterization/metrology techniques will be discussed, and examples of correlating such physical and chemical materials characterization to device behavior will also be presented.

Biography

Robert ("Bob") M. Wallace (IEEE Fellow) is a Professor of Materials Science and Engineering and holds the Erik Jonsson Distinguished Chair in the Erik Jonsson School of Engineering and Computer Science at the University of Texas at Dallas. He received his Ph. D. in Physics at the University of Pittsburgh in 1988. After postdoctoral studies in Surface Chemistry at Pitt, Wallace joined the Central Research Labs at Texas Instruments in Dallas, where he performed and led advanced device materials characterization and development, including pioneering work on hafnium and zirconium-based high-k gate dielectrics. In 2003, he joined the faculty at the University of Texas at Dallas, was a founding member of the Materials Science and Engineering department. Wallace also has appointments in the Departments of Electrical Engineering, Mechanical Engineering, and Physics.

Wallace's research program focuses on nanoelectronic materials and interfaces, and he currently leads the materials benchmarking and characterization research in the US nCORE NEWLIMITS Center. He has authored or co-authored over 340 publications in peer reviewed journals and proceedings resulting in over 30,000 citations, more than 290 contributed and 100 invited talks at international meetings and symposia, as well as 47 US and 30 international patents/applications. He was named Fellow of the AVS in 2007 and an IEEE Fellow in 2009 for his contributions to the field of high-k dielectrics in integrated circuits. He has attended SISC since 1996 and served on the Program and Executive Committees. He was also a winner of the SISC 1998 Limerick Contest.

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Conference Agenda Overview

Wednesday, December 8, 2021

Registration	6:00 PM – 8:00 PM
Evening Tutorial	8:00 PM – 9:30 PM

Thursday, December 9, 2021

Registration	8:00 AM – 5:00 PM
Session 1: Ferroelectrics I	8:00 AM – 9:40 AM
Session 2: Tribute to Mark Reed	10:00 AM – 11:45 AM
Session 3: III–V	1:30 PM – 3:05 PM
Session 4: Poster Preview I & Coffee Break	3:15 PM – 3:40 PM
Session 5: Back-end-of-line Technologies	3:40 PM – 5:15 PM
Session 6: Poster Preview II	5:35 PM – 6:05 PM
Virtual Poster Session on Zoom	6:30 PM – 7:30 PM
Reception & Poster Session	7:00 PM – 11:00 PM

Friday, December 10, 2021

Registration	8:00 AM – 12:00 PM
Session 7: Ferroelectrics II	8:15 AM – 9:30 AM
Session 8: Tribute to T. P. Ma	10:00 AM – 11:45 AM
Committee / Invited Speaker Luncheon	12:00 PM – 1:30 PM
Session 9: 2D Materials	1:30 PM – 3:10 PM
Session 10: Memory	3:25 PM – 5:35 PM
Conference Banquet & Limerick Contest	7:00 PM – 10:00 PM

Saturday, December 11, 2021

Session 11: Ferroelectrics III	8:00 AM – 9:20 AM
Session 12: High-Temperature & Power Electronics	9:35 AM – 11:30 AM
Session 13: Extreme Conditions	11:45 AM – 12:25 PM

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Wednesday, December 8, 2021

Tutorial

Session Chair: W. G. Vandenberghe

8:00 PM – 9:30 PM *Tutorial* – **Physical Characterization of Advanced Materials,** R. M. Wallace, *UT Dallas*

Thursday, December 9, 2021

Session 1: Ferroelectrics I

Session Chair: P. C. McIntyre

8:00 AM Introduction

8:05 AM 1.1 *Invited* – **Hafnia-based Ferroelectrics,** S. Slesazeck[1], S. Lancaster[1], M. Engl[1], and T. Mikolajick[1,2], [1]*NaMLab gGmbH, Germany,* [2]*TU Dresden, Germany*

8:40 AM 1.2 – **Why is hysteresis-free switching impossible in ferroelectrics?,** J. Van Houdt[1,2], P. Roussel[1], S. Clima[1], M. N. K. Alam[1,2], and V. V. Afanas'ev[2], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

9:00 AM 1.3 – **Isovalent doping in hafnium-zirconium oxides to lower polarization switching voltage,** K. Chae[1,2], A. C. Kummel[2], and K. Cho[3], [1]*UCSD,* [2]*UT Dallas*

9:20 AM 1.4 – **Thermodynamic process of transient negative capacitance in ferroelectric capacitors,** Y. Y. Zhang[1], X. L. Wang[2], J. S. Chai[2], J. J. Xiang[2], W. W. Wang[2], and J. Xu[1], [1]*Tsinghua U., China,* [2]*Chinese Academy of Sciences, China*

9:40 AM – 10:00 AM Coffee Break

Session 2: Tribute to Mark Reed

Session Chair: R. M. Wallace

10:00 AM 2.1 *Invited* – **Mark Reed and the Birth of Nanoelectronics,** A. Seabaugh[1], W. R. Frensley[2], and J. N. Randall[3], [1]*U. Notre Dame,* [2]*UT Dallas,* [3]*Zyvex Labs*

10:35 AM 2.2 *Invited* – **Mark Reed and the Birth of Molecular Electronics,** J. M. Tour, *Rice U.*

11:10 AM 2.3 *Invited* – **A New Era of Integrated Molecular Electronics: A Programmable Single-Molecule Biosensor on a Semiconductor Chip,** B. Merriman, *Roswell Biotechnologies*

Session 3: III–V

Session Chair: A. C. Kummel

1:30 PM — 3.1 *Invited* – **Functional Integration on III–V Nanowires,** L.-E. Wernersson, *Lund U., Sweden*

2:05 PM — 3.2 – **In-situ deposited Y_2O_3/InGaAs heterostructure with low D_{it} of (0.8–7)$\times 10^{11}$ $eV^{-1}cm^{-2}$ and high-temperature thermal stability,** Y.-H. G. Lin[1], K. H. Lai[1], H.-W. Wan[1], L. B. Young[1], Y. T. Cheng[1], J. Kwo[2], and M. Hong[1], [1]*National Taiwan U., Taiwan,* [2]*National Tsing Hua U., Taiwan*

2:25 PM — 3.3 – **Ferroelectric high-k on III–Vs,** A. E. O. Persson, R. Athle, M. Borg, and L.-E. Wernersson, *Lund U., Sweden*

2:45 PM — 3.4 – **Attainment of low subthreshold slope in planar inversion-channel InGaAs MOSFETs with in-situ deposited high-κ gate dielectrics,** L. B. Young[1], J. Liu[1], Y.-H. G. Lin[1], H.-W. Wan[1], T. D. Lin[1], J. Kwo[2], and M. Hong[1], [1]*National Taiwan U., Taiwan,* [2]*National Tsing Hua U., Taiwan*

Session 4: Poster Preview I

Session Chair: W. G. Vandenberghe

3:15 PM — 4.1 – **Origins of Fermi Level Pinning for Ni and Ag Contacts on $MoSe_2$ and $MoTe_2$: An Interface Chemistry Study,** X. Wang, S. Y. Kim, Y. Shen, and R. M. Wallace, *UT Dallas*

3:16 PM — 4.2 – **2D $ReSe_2$ RRM and Analog Model for Neuromorphic Computing,** Y. Huang[1], X. Wu[1], Y. Gu[1], R. Ge[1], J. Zhang[1], Y.-F. Chang[2], D. Akinwande[1], and J. C. Lee[1], [1]*UT Austin,* [2]*Intel*

3:17 PM — 4.3 – **Bias-Temperature Instability (BTI) in Multilayered ReS_2 FET with a high-k α-MoO_3 passivation,** J. Lee[1], J. Chun[1,2], and G.-T. Kim[1], [1]*Korea U., Korea,* [2]*Samsung, Korea*

3:18 PM — 4.4 – **Band Alignment of WS_2 with SiO_2: Evolution with Layer Thickness,** G. Delie[1], P. M. Litwin[2], G. C. Abad[2], S. J. McDonnell[2], D. Chiappe[3], and V. V. Afanas'ev[1], [1]*U. Leuven, Belgium,* [2]*U. Virginia,* [3]*imec, Belgium*

3:19 PM — 4.5 – **Oxidized MoS_2:the path to memristor based memories,** K. Burgholzer, R. Adhikari, and A. Bonanni, *Johannes Kepler U. Linz, Austria*

3:20 PM — 4.6 – **Schottky Barrier Heights and Contact Bond Lengths of layered MoS_2,** J. Robertson[1], Z. Zhang[1], and Y. Guo[2], [1]*U. Cambridge, UK,* [2]*Wuhan U., China*

3:21 PM — 4.7 – **Making Defect-Free Transition-Metal Dichalcogenide Transistors using Transition-Metal Nitride Halide Dielectrics,** M. Rostami Osanloo, A. Saadat, M. L. Van de Put, A. Laturia, and W. G. Vandenberghe, *UT Dallas*

3:22 PM — 4.8 – **Tunable contacts and device performance in Graphene/Group-III monochalcogenides MX (M=In, Ga; X=S, Se) heterostructures,** H. Guo[1], Y. Yin[1], J. Robertson[1], Z. Zhang[2], and Y. Guo[1], [1]*Wuhan U., China,* [2]*U. Cambridge, UK*

3:23 PM — 4.9 – **Contact Resistivity Improvement by Metal-Insulator-Semiconductor (MIS) Contacts with Bilayer Insulators,** A. Okuyama[1], R. Suzuki[1], M. Schaekers[2], J.-L. Everaert[2], and N. Horiguchi[2], [1]*Sony Semiconductor Solutions, Japan,* [2]*imec, Belgium*

3:24 PM 4.10 – **Probing Ferromagnetism in van der Waals Iron Germanium Telluride,** S. Chyczewski, K. Xu, and W. Zhu, *UIUC*

3:25 PM 4.11 – **In-situ doping of WSe_2 for low resistance contacts and memory applications,** R. Younas, G. Zhou, and C. L. Hinkle, *U. Notre Dame*

3:26 PM 4.12 – **Schottky Barrier Heights and Tunnelling at Metal/Oxide Interfaces,** J. Chen, Z. Zhang, Y. Guo, and J. Robertson, *U. Cambridge, UK*

3:27 PM 4.13 – **Oxidation and passivation mechanisms for SiC/SiO_2 interfaces,** J. Robertson and Z. Zhang, *U. Cambridge, UK*

3:28 PM 4.14 – **A Multi-Objective Approach to Identifying Post-Cu Interconnect Candidates,** A. Ramdas, E. Antoniuk, and E. J. Reed, *Stanford U.*

3:29 PM 4.15 – **Selectivity Relationship of Ru ALD towards Bulk-like Resistivity,** M. Breeden[1], V. Wang[1], F. Yu[1], R. Kanjolia[2], M. Moinpour[2], J. Woodruff[3], H. Simka[4], and A. C. Kummel[1], [1]*UCSD,* [2]*EMD Electronics,* [3]*Samsung Electronics*

3:30 PM 4.16 – **Multifunctional Ruthenium Oxide for BEOL-compatible Reprogrammable One-Time-Programmable (OTP) Memory Application,** Y.-C. Chen[1], C.-C. Lin[2], and C.-H. Lin[2], [1]*Northern Arizona U.,* [2]*National Applied Research Laboratories, Taiwan*

3:31 PM 4.17 – **Epitaxial growth corundum V_2O_3 and Cr_2O_3 on Si(111) substrate,** W.-F. Hsu, M. Recamán Payo, A. Binetti, J. W. Seo, and J.-P. Locquet, *U. Leuven, Belgium*

3:32 PM 4.18 – **Internal reverse-biased p-n junctions: a possible origin of the high resistance in phase change superlattice,** B. Li[1], L. Xu[1], Y. Guo[2], and H. Li[1], [1]*Tsinghua U., China,* [2]*Swansea U., UK*

3:33 PM 4.19 – **A dimensional crossover to a Mott insulator in V_2O_3 ultrathin films,** S. Mellaerts, C. Bellani, W.-F. Hsu, K. Schouteden, M. Recamán Payo, J. W. Seo, and J.-P. Locquet, *U. Leuven, Belgium*

3:34 PM 4.20 – **Highly Reliable Ultra-Steep Slope Threshold Switching Behavior with Controlled Ag Doping of Nano-polycrystalline ZnO Layer,** A. Sahota, H. S. Kim, J. Mohan, Y. C. Jung, H. Hernandez-Arriaga, D. N. Le, and J.-H. Kim, *UT Dallas*

3:35 PM 4.21 – **Insights into Cold Source Devices with Sub-60 mV/decade and Negative Differential Resistance Effect,** Y. Yin[1], Z. Zhang[2], C. Shao[1], J. Robertson[2], and Y. Guo[1,2], [1]*Wuhan U., China,* [2]*U. Cambridge, UK*

3:36 PM 4.22 – **Multi-State Quantum Dot Channel (QDC) FETs for Multi-Bit Computing,** F. Jain[1], R. Gudlavalleti[1], R. Mays[1], B. Saman[1,2], P-Y. Chan[1], J. Chandy[1], M. Lingalugari[3], and E. Heller[4], [1]*U. Connecticut,* [2]*Taif U., Saudi Arabia,* [3]*Intel,* [4]*Synopsys*

3:37 PM 4.23 – **High-quality single-crystal superconducting Al thin film and ultra-low interface roughness in Al_2O_3/Al/sapphire heterostructure for quantum computing,** Y.-H. G. Lin[1], L. B. Young[1], L. S. Chiang[1], H.-W. Wan[1], Y. T. Cheng[1], C.-H. Hsu[2], J. J. Lin[3], C.-T. Liang[1], Y. H. Lin[4], J. Kwo[4], and M. Hong[1], [1]*National Taiwan U., Taiwan,* [2]*National Synchrotron Radiation Research Center, Taiwan,* [3]*National Yang Ming Chiao Tung U., Taiwan,* [4]*National Tsing Hua U., Taiwan*

3:38 PM 4.24 – **Artificial Photonic Synapse with Colloidal Perovskite Quantum Dot $CsPbI_3$,** B. Ku, B. Koo, W. Kim, M. J. Ko, and C. Choi, *Hanyang U., Korea*

3:39 PM 4.25 – **Crystalline Gallium Nitride Deposition by RF-Biased Atomic Layer Annealing,** A. J. McLeod[1], S. T. Ueda[1], J. Spiegelman[2], and A. C. Kummel[1], [1]*UCSD,* [2]*RASIRC*

Session 5: Back-end-of-line Technologies

Session Chair: C. L. Hinkle

3:40 PM — 5.1 *Invited* – **RF-Biased Atomic Layer Annealing of Polycrystalline Materials at Low Temperature on Insulators,** A. J. McLeod[1], S. T. Ueda[1], J. Spiegelman[2], and A. C. Kummel[1], [1]*UCSD,* [2]*RASIRC*

4:15 PM — 5.2 – **Thermal Engineering of Top-gated In_2O_3 Field-effect Transistor Achieving 2 A/mm Drain Current Directly on Highly Resistive Silicon Substrate,** P.-Y. Liao, M. Si, Z. Zhang, Z. Lin, and P. D. Ye, *Purdue U.*

4:35 PM — 5.3 – **Atomically thin In_2O_3 Field-effect Transistors with 10^{17} Current On/Off Ratio,** A. Charnas, Z. Lin, Z. Zhang, and P. D. Ye, *Purdue U.*

4:55 PM — 5.4 – **First Demonstration of Atomically Thin Indium-Tin-Oxide Transistors Enabled by Atomic Layer Deposition,** Z. Zhang[1], Y. Hu[2], Z. Lin[1], M. Si[1], K. Cho[2], and P. D. Ye[1], [1]*Purdue U.,* [2]*UT Dallas*

Session 6: Poster Preview II

Session Chair: W. G. Vandenberghe

5:35 PM — 6.1 – **Surface Band-bending Modulation of Ga-face GaN through ALD Oxides,** J. Gong[1], J. Kim[1], T. K. Ng[2], K. Lu[3], D. Kim[1], J. Zhou[1], D. Liu[1], J. Kim[3], B. S. Ooi[2], and Z. Ma[1], [1]*U. Wisconsin–Madison,* [2]*King Abdullah U. Science and Technology, Saudi Arabia,* [3]*MIT*

5:36 PM — 6.2 – **$Al_{0.85}Ga_{0.15}N$ MOSFET with High Quality Interface and >3 kV Breakdown Voltage,** J. Wang, H. Zhou, J. Zhang, and Y. Hao, *Xidian U., China*

5:37 PM — 6.3 – **Plasma Enhanced Atomic Layer Deposition of Crystallized Gallium Phosphide with Triethylgallium and Tritertbutylphosphine,** S. Yun, S. T. Ueda, V. Wang, C.-H. Kuo, H. Kashyap, A. J. McLeod, and A. C. Kummel, *UCSD*

5:38 PM — 6.4 – **Low Resistivity Titanium Nitride Thin Film Fabricated by Atomic Layer Deposition in Patterned Samples,** C.-H. Kuo[1], A. J. McLeod[1], J. Huang[1], V. Wang[1], Z. Chang[1], D. Alvarez[2], and A. C. Kummel[1], [1]*UCSD,* [2]*RASIRC*

5:39 PM — 6.5 – **Facile method of etching the shell of the core-shell Si Nanowires synthesized by Hot Wire Chemical Vapor Processing Technique,** N. Arya and R. O. Dusane, *IIT Mumbai, India*

5:40 PM — 6.6 – **Growing GaOOH nanocrystals on GaAs surface by hot water oxidation,** Z. J. Rad[1], S. Vuori[1], J.-P. Lehtiö[1], S. Granroth[1], H. Singh[2], I. Angervo[1], M. P. J. Punkkinen[1], M. Kuzmin[1], M. N. Singh[3], M. Lastusaari[1], P. Laukkanen[1], M. Huttula[2], P. Paturi[1], and K. Kokko[1], [1]*U. Turku, Finland,* [2]*U. Oulu, Finland,* [3]*Raja Ramanna Centre for Advanced Technology, India*

5:41 PM — 6.7 – **Semiconductor interfaces investigated by T-ray cameraless 3D layer-by-layer imaging,** A. Rahman, *Applied Research & Photonics*

5:42 PM — 6.8 – **Time-dependent photoluminescence from nanostructured photon upconverters,** E. Y. Chen[1], T. A. Welsch[1], J. M. Cleveland[1], C. C. Milleville[1], K. R. Lennon[1], J. M. O. Zide[1], D. B. Chase[1], M. F. Doty[1], and H. Y. Ramírez[2], [1]*U. Delaware,* [2]*Pedagogical and Technological U. Colombia, Colombia*

5:43 PM 6.9 – **Model for the Bipolar Amplification Effect for MOS Interface Defect Studies,** J. P. Ashton[1], S. J. Moxim[2], A. D. Purcell[2], P. M. Lenahan[2], and J. T. Ryan[1], [1]*NIST,* [2]*Pennsylvania State U.*

5:44 PM 6.10 – **Controlling the negative charge formation in Si/Al_2O_3 interfaces,** J.-P. Lehtiö, Z. J. Rad, M. P. J. Punkkinen, R. Punkkinen, P. Laukkanen, and K. Kokko, *U. Turku, Finland*

5:45 PM 6.11 – **Early Stage Mechanisms in Time-Dependent Dielectric Breakdown in the Si/SiO_2 System,** F. V. Sharov[1], S. J. Moxim[1], D. R. Hughart[2], G. S. Haase[2], and P. M. Lenahan[1], [1]*Pennsylvania State U.,* [2]*Sandia National Laboratories*

5:46 PM 6.12 – **Selective Chemical Vapor Deposition of TiO_2/Al_2O_3 and HfO_2/Al_2O_3 Nanolaminates on Si and SiO_2 in Preference to SiCOH,** J. Huang[1], Y. Cho[1], Z. Zhang[1], K. T. Wong[2], S. D. Nemani[2], E. Yieh[2], and A. C. Kummel[1], [1]*UCSD,* [2]*Applied Materials*

5:47 PM 6.13 – **Demonstration of 1e11 endurance of low power ferroelectric HfO_2 device with CeO_x buffer layer fabricated by ultra-low thermal budget process,** J. Molina[1,2], H. Funakubo[2], I. Fujiwara[2], H. Wakabayashi[2], K. Tsutsui[2], and K. Kakushima[2], [1]*National Institute of Astrophysics, Optics and Electronics, Mexico,* [2]*Tokyo Institute of Technology, Japan*

5:48 PM 6.14 – **P-type oxides in Back-end-of-line Semiconductor Devices,** Z. Zhang[1], Y. Guo[2], and J. Robertson[1], [1]*U. Cambridge, UK,* [2]*Swansea U., UK*

5:49 PM 6.15 – **High-performance Asymmetric Ferroelectric Semiconductor Junction Based on Millimeter Scale PVD-Grown α-In_2Se_3,** D. Zheng, Z. Chen, M. Si, and P. D. Ye, *Purdue U.*

5:50 PM 6.16 – **The Impact of Dielectric Layer on the Memory Characteristics of Ferroelectric Field-Effect Transistors,** M. Si[1,2] and P. D. Ye[2], [1]*Shanghai Jiao Tong U., China,* [2]*Purdue U.*

5:51 PM 6.17 – **Interlayer thinning by Oxygen scavenging Electrode in HZO/Ge interface,** H. Kashyap and A. C. Kummel, *UCSD*

5:52 PM 6.18 – **BEOL (Back End of Line) Applicable Ferroelectric $HfZrO_2$ by PEALD with Low Temperature Annealing, Wake-up Free, and Synaptic Application,** C.-Y. Liao[1], K.-Y. Hsiang[1,2], Z.-F. Luo[1], C.-Y. Lin[1], Y.-D. Lin[3], P.-C. Yeh[3], C.-Y. Wang[3], H.-Y. Yang[3], P.-J. Tzeng[3], Y.-T. Tang[4], T.-H. Hou[2,3], and M. H. Lee[1], [1]*Nation Taiwan Normal U., Taiwan,* [2]*Nation Yang Ming Chiao Tung U., Taiwan,* [3]*Industrial Technology Research Institute, Taiwan,* [4]*National Central U., Taiwan*

5:53 PM 6.19 – **Ferroelectricity in CeO_2-Doped $Hf_{0.5}Zr_{0.5}O_2$ Thin Films,** Z. Yu[1], B. Saini[1], P. J. Liao[2], Y. K. Chang[2], V. Hou[2], C. H. Nien[2], Y. C. Shih[2], S. H. Yeong[2], V. V. Afanas'ev[3], F. Huang[1], J. D. Baniecki[4], A. Mehta[4], C. S. Chang[2], H.-S. P. Wong[1], W. Tsai[1], and P. C. McIntyre[1,4], [1]*Stanford U.,* [2]*TSMC, Taiwan,* [3]*U. Leuven, Belgium,* [4]*SLAC National Accelerator Laboratory*

5:54 PM 6.20 – **TCAD Based Study of the Impact of Traps on RF FinFETs,** J.-L. Huang, Y.-C. Liu, and M.-H. Chiang, *National Cheng Kung U., Taiwan*

5:55 PM 6.21 – **Paradigm Change for the Interfaces of III–V MOS-based Devices,** A. Irish, A. Troian, R. Atle, A. E. O. Persson, M. S. Ram, K.-M. Persson, G. D'Acunto, L.-E. Wernersson, M. Borg, and R. Timm, *Lund U., Sweden*

5:56 PM — 6.22 – **Achieving Low D_{it} of (2–4) $\times$ 10^{10} $eV^{-1}cm^{-2}$ using Y_2O_3/epi-Si/Ge Gate Stacks,** H.-W. Wan[1], Y. T. Cheng[1], C. K. Cheng[1], T. Y. Chu[1], T. W. Pi[2], J. Kwo[3], and M. Hong[1], [1]*National Taiwan U., Taiwan,* [2]*National Synchrotron Radiation Research Center, Taiwan,* [3]*National Tsing Hua U., Taiwan*

5:57 PM — 6.23 – **Thermal Stability of Epitaxial GeSn Layers on Ge-buffered Si by CVD,** W.-H. Hsieh, S.-Y. Lin, and C. W. Liu, *National Taiwan U., Taiwan*

5:58 PM — 6.24 – **Structural characterization of thin epi-Si in high-k/Si/Ge,** C. K. Cheng[1], H.-W. Wan[1], Y. T. Cheng[1], C.-H. Hsu[2], J. Kwo[3], and M. Hong[1], [1]*National Taiwan U., Taiwan,* [2]*National Synchrotron Radiation Research Center, Taiwan,* [3]*National Tsing Hua U., Taiwan*

5:59 PM — 6.25 – **A High I_{ON}/I_{OFF} Ratio of 5.3×10^2 in $Ge_{0.85}Sn_{0.15}$ n+/p Junctions by Phosphorus Ion Implantation and Microwave Annealing,** S.-Y. Lin, W.-H. Hsieh, and C. W. Liu, *National Taiwan U., Taiwan*

6:00 PM — 6.26 – **Ge Intra-Chip Data Communication,** C.-C. Chou, C.-P. Chen, and T.-H. Cheng, *LiveStrong Optoelectronics, Taiwan*

6:05 PM — End

6:30 PM – 7:30 PM — Virtual Poster Session on Zoom

7:00 PM – 11:00 PM — Reception/Poster Session

Friday, December 10, 2021

Session 7: Ferroelectrics II

Session Chair: H. Bu

8:15 AM — 7.1 *Invited* – **Ferroelectric Materials and Devices for Disruptive Semiconductor Technology,** J. Heo[1], D.-H. Choe[1], H. Lee[1], S. Jo[1], H. Bae[1], S. G. Nam[1], J.-H. Kim[1], E. Lee[1], Y. Kim[2], H. Kim[2], Y. Lee[1], T. Moon[1], and H. Lee[1], [1]*Samsung Advanced Institute of Technology, Korea,* [2]*Sungkyunkwan U., Korea*

8:50 AM — 7.2 – **The Effects of Anhydrous Hydrogen Peroxide as the Oxidant Source for Low Temperature Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Films Using Thermal Atomic Layer Deposition,** J.-H. Kim[1], Y. C. Jung[1], S. Hwang[1], H. Hernandez-Arriaga[1], J. Mohan[1], D. N. Le[1], D. Alvarez[2], J. Spiegelman[2], and J.-H. Kim[1], [1]*UT Dallas,* [2]*RASIRC*

9:10 AM — 7.3 – **Dielectric response evolution in ferroelectrics during electric polarization switching based on analytical calculations and first-principles modelling,** S. Clima[1], A. S. Verhulst[1], B. Truijen[1], G. Pourtois[1,2], and J. Van Houdt[1,3], [1]*imec, Belgium,* [2]*U. Antwerp, Belgium,* [3]*U. Leuven, Belgium*

9:30 AM – 10:00 AM — Coffee Break

Session 8: Tribute to T. P. Ma

Session Chair: W. Zhu

10:00 AM — 8.1 *Invited* – **CMOS Logic Technology Scaling Beyond FinFETs — In memory of the legacy of T. P. Ma,** H. Bu, D. Guo, D. Dechene, V. Narayanan, A. Chen, J. Rozen, and M. Frank, *IBM*

10:35 AM — 8.2 *Invited* – **Dielectrics for Devices from CMOS Extension to Beyond-CMOS A personal research journey owing to the inspiration, guidance, and support of Prof. Ma,** A. Chen, *SRC*

11:10 AM — 8.3 *Invited* – **Atomic-layer-deposited atomically thin In_2O_3 channel for BEOL logic and memory applications,** P. D. Ye, *Purdue U.*

Session 9: 2D Materials

Session Chair: A. Seabaugh

1:30 PM — 9.1 – **Understanding CV response and band bending fluctuations in dual gated WS_2 MOSCAPs,** V. Mootheri[1,2], X. Wu[1], D. Cott[1], M. Heyns[1,2], I. Asselberghs[1], I. Radu[1], and D. Lin[1], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

1:50 PM — 9.2 – **Thermal Stability Study of Ni Contacts on MoS_2,** X. Wang, S. Y. Kim, and R. M. Wallace, *UT Dallas*

2:10 PM — 9.3 – **Origins of Fermi Level Pinning for Ni and Ag Contacts on Tungsten Dichalcogenides: Interface Chemistry and Band Alignment,** S. Y. Kim, X. Wang, and R. M. Wallace, *UT Dallas*

2:30 PM — 9.4 – **Spatially Composition-graded Monolayer $WSe_{2x}Te_{2-2x}$ Nanosheets,** K. Xu, Z. Hao, J. Kang, and W. Zhu, *UIUC*

2:50 PM — 9.5 – **Van der Waals Vertical Transistors with Run-time Reconfigurability,** Z. Zhao and W. Zhu, *UIUC*

3:10 PM – 3:35 PM — Coffee Break

Session 10: Memory

Session Chair: J. Kim

3:35 PM — 10.1 – **First 1S1R device based on Ge-rich GeSbTe-based "Wall" Phase Change Memory (PCM) and GeSbSeN-based Ovonic Threshold Switching (OTS) for BEOL Crossbar Arrays,** Y. Moustapha-Rabault[1,2,3], C. Laguna[1], J. Gasquez[2], V. Meli[1], J. Garrione[1], M. Tessaire[1], C. Sabbione[1], C. Socquet-Clerc[1], T. Magis[1], F. Aussenac[1], N. Castellani[1], G. Bourgeois[1], M. C. Cyrille[1], F. Andrieu[1], P. Boivin[2], and G. Navarro[1], [1]*CEA-Leti, France,* [2]*STMicroelectronics, France,* [3]*U. Grenoble Alpes, France*

3:55 PM — 10.2 – **Hexagonal Boron Nitride as the Tunnel Barrier in Magnetic Tunnel Junctions,** H. Lu[1,2] and J. Robertson[2], [1]*Beihang U., China,* [2]*U. Cambridge, UK*

4:15 PM — 10.3 – **Insights into the Origin of MLC Capability and its Reliability in Si-doped GeSbTe Phase Change Memory for SCM applications,** G. Lama, N. Bernier, F. Fillot, G. Bourgeois, N. Castellani, M. C. Cyrille, F. Andrieu, and G. Navarro, *CEA-Leti, France*

4:35 PM 10.4 – **Low Resistance States Variability in Innovative V_2O_3:Cr Mott Insulator-based Resistive Memory,** L. Laborie[12], J. Tranchant[2], B. Corraze[2], G. Lefevre[3], N. Castellani[1], G. Bourgeois[1], C. Castellana[1], T. Magis[1], E. Janod[2], M.-P. Besland[2], C. Vallée[13], S. David[3], E. Nowak[1], G. Molas[1], E. Jalaguier[1], and L. Cario[2], [1]*CEA-Leti, France,* [2]*U. Nantes, France,* [3]*U. Grenoble Alpes, France*

4:55 PM 10.5 – **Surface-to-Surface Tunneling Device using Three Dimensional Topological Insulators,** S. P. Fluckey, S. Tiwari, and W. G. Vandenberghe, *UT Dallas*

5:15 PM 10.6 – **Magnetic Memory Device using a Topological Insulator Ferromagnet Heterostructure,** S. Tiwari[1,2,3], M. L. Van de Put[1], W. G. Vandenberghe[1], and B. Sorée[2,3], [1]*UT Dallas,* [2]*U. Leuven, Belgium,* [3]*imec, Belgium*

7:00 PM – 10:00 PM Conference Banquet & Limerick Contest

Saturday, December 11, 2021

Session 11: Ferroelectrics III

Session Chair: J. Heo

8:00 AM 11.1 – **Charge Trapping Effects on Memory Window in Ferroelectric Field Effect Transistors,** N. Tasneem, Z. Wang, M. M. Islam, S. F. Lombardo, H. Chen, J. Hur, S. Yu, W. Chern, and A. Khan, *Georgia Institute of Technology*

8:20 AM 11.2 – **Impact of Electric Field, Electrode Material and Stress Bias on the Reliability Performance of Ferroelectric HZO Thin Film,** X. Lyu, M. Si, and P. D. Ye, *Purdue U.*

8:40 AM 11.3 – **Performance Enhancement of BEOL-Compatible Atomic-Layer-Deposited In_2O_3 Fe-FETs by Interfacial Layer Engineering,** Z. Lin, M. Si, X. Lyu, and P. D. Ye, *Purdue U.*

9:00 AM 11.4 – **Fabrication of cerium doped hafnium-zirconium oxide thin films by solution process and their application to ferroelectric gate transistors,** Mohit and E. Tokumitsu, *JAIST, Japan*

9:20 AM – 9:35 AM Coffee Break

Session 12: High-Temperature & Power Electronics

Session Chair: P. D. Ye

9:35 AM 12.1 *Invited* – **High-Frequency Ga_2O_3 FETs and Interface Related Challenges in Their Development,** M. Higashiwaki, T. Kamimura, and S. Kumar, *National Institute of Information and Communications Technology, Japan*

10:10 AM 12.2 – **High-temperature AlGaN/GaN Transistors with Nanolaminate Gate Dielectrics,** H. Ryu, H. Lee, and W. Zhu, *UIUC*

10:30 AM 12.3 – **Extreme High Temperature Operation of Depletion-Mode and Enhancement-Mode AlGaN/GaN MIS-HEMT,** H. Lee, H. Ryu, and W. Zhu, *UIUC*

10:50 AM 12.4 – **Nanoscale study on surface potential fluctuations of SiO_2/SiC interfaces by time-resolved scanning nonlinear dielectric microscopy,** K. Yamasue and Y. Cho, *Tohoku U., Japan*

11:10 AM 12.5 – **High I_{ON}/I_{OFF} Ratio 4H-SiC MISFETs with Stable Operation at 500 °C using $SiO_2/Si_3N_4/Al_2O_3$ Gate Stacks,** J. Kang and W. Zhu, *UIUC*

Session 13: Extreme Conditions

Session Chair: A. Saadat

11:45 AM 13.1 – **Time-Dependent Cryogenic Device Characterization,** P. R. Shrestha[1,2], A. Akturk[3], B. Hoskins[2], A. Madhavan[4,2], and J. P. Campbell[2], [1]*Theiss Research,* [2]*NIST,* [3]*CoolCAD,* [4]*U. Maryland*

12:05 PM 13.2 – **MOSFET Parameter Variations Depending on the Distribution of Externally-Induced GPa-level Mechanical Stress,** K. Lee[1,2], B. Kaczer[2], A. Kruv[1,2], M. Gonzalez[2], G. Eneman[2], O. O. Okudur[2], A. Grill[2], and I. De Wolf[1,2], [1]*U. Leuven, Belgium,* [2]*imec, Belgium*

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