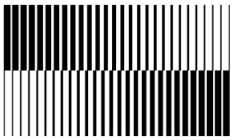

SISC 2022

53rd IEEE
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December 7–10, 2022
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SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology," published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author for either an oral or a poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

2021 SISC Ed Nicollian Award for Best Student Paper

Nujhat Tasneem

Georgia Institute of Technology

"Charge Trapping Effects on Memory Window in Ferroelectric Field Effect Transistors"
with Z. Wang, M. M. Islam, S. F. Lombardo, H. Chen, J. Hur, S. Yu, W. Chern, and A. Khan

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SISC T. P. Ma Award for Best Student Poster

In 2021, the SISC added an award for the best student poster in honor of Professor T. P. Ma, Yale University. Professor Ma was an internationally recognized pioneer for his contributions to semiconductor science and technology — in particular, breakthroughs in advanced gate dielectrics, which paved the path for high-κ dielectrics and extended the scaling of CMOS technology. His research also generated fundamental and lasting impacts on many other applied physics fields, notably ferroelectrics and ionizing radiation sciences.

The *SISC T. P. Ma Award* will be presented to the lead student author for a poster presentation. The winner will be chosen by members of the technical program committee at the end of the SISC. The award will consist of a plaque, an honorarium, and a permanent mention on the conference web site.

2021 SISC T. P. Ma Award for Best Student Poster

Simon Mellaerts

University of Leuven, Belgium

"A dimensional crossover to a Mott insulator in V_2O_3 ultrathin films"
with C. Bellani, W. F. Hsu, K. Schouteden, M. Recaman Payo, J. W. Seo, and J.-P. Locquet

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Wednesday Evening Tutorial

Wednesday, December 7, 2022, 8:00 PM

First introduced at SISC 2008, the Wednesday Evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

Prof. Muhammad A. Alam, *Purdue U.*

Reliability Physics for Post-Moore Era Electronics: An Integrated Material, Devices, and System Perspective

In the 1950s, one had to walk into a computer; today, we carry a number of computers as we walk around. These Interface computers (e.g., Google Watches, Fitbits, Amazon Echo) contain ultra-scaled heterogeneously-integrated logic and power transistors, DRAM and Flash memories, MEMS microphones and gyroscopes, physical and bio-chemical sensors, energy harvesters, batteries, and so on.

The material library needed for 3D heterogeneous ICs is exploding, the device options are proliferating, and the von-Neumann computing architecture itself is expanding to include neural networks, guided by the specialized needs of ecosystem companies, such as Amazon, LinkedIn, and eBay. I believe that this sea-change in computing technology must be supported by a corresponding broadening of our focus on multi-component reliability physics. We must understand on equal footing the reliability physics of logic and power transistors, sensors, solar cells, and batteries (as well as the interaction between the package and the ICs it encapsulates) and create a platform that predicts the integrated, application-specific, system-level reliability.

I will use illustrative examples of self-heating in transistors, fluid-stability of biosensors, shadow/corrosion physics of solar cells, fatigue/stiction in MEMS, and ion-transport due to chip-package interaction to explain how a new generation of predictive reliability models will ensure the reliability of post-Moore era electronics.

Biography

Professor Alam holds the Jai N. Gupta professorship at Purdue University, where his research focuses on the physics and technology of semiconductor devices. From 1995 to 2003, he was with Bell Laboratories, Murray Hill, NJ, as a Member of the Technical Staff in the Silicon ULSI Research Department. Since joining Purdue in 2004, Dr. Alam has published over 350 papers and he has contributed to the reliability physics of transistors, biosensors, and solar cells. He is a fellow of IEEE, APS, and AAAS. His awards include the 2006 IEEE Kiyo Tomiyasu Medal for contributions to device technology, the 2015 SRC Technical Excellence Award for fundamental contributions to reliability physics, and the 2018 IEEE EDS Award for educating, inspiring, and mentoring students and electron device professionals around the world. More than 450,000 students worldwide have learned some aspects of semiconductor devices from his web-enabled courses.

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Conference Agenda Overview

Wednesday, December 7, 2022

Registration	6:00 PM – 8:00 PM
Evening Tutorial	8:00 PM – 9:30 PM

Thursday, December 8, 2022

Registration	8:00 AM – 5:00 PM
Session 1: Ferroelectrics I	8:20 AM – 9:45 AM
Session 2: BEOL Oxides	10:20 AM – 11:55 AM
Session 3: Advanced Device Technologies	1:30 PM – 3:05 PM
Session 4: Poster Preview I	3:05 PM – 3:25 PM
Session 5: Wide Bandgap Semiconductors	3:45 PM – 5:00 PM
Session 6: Poster Preview II	5:20 PM – 5:50 PM
Reception & Poster Session	7:00 PM – 10:00 PM

Friday, December 9, 2022

Registration	8:00 AM – 12:00 PM
Session 7: 2D Materials I	8:00 AM – 9:35 AM
Session 8: Ferroelectrics II	9:50 AM – 11:45 AM
Committee / Invited Speaker Luncheon	12:00 PM – 1:30 PM
Session 9: 2D Materials II	1:30 PM – 3:25 PM
Session 10: Advanced Characterization Technologies	3:40 PM – 5:15 PM
Conference Banquet & Limerick Contest	7:00 PM – 10:00 PM

Saturday, December 10, 2022

Session 11: Ferroelectrics III	8:00 AM – 9:15 AM
Session 12: 2D Materials III	9:30 AM – 11:05 AM
Session 13: Emerging Technologies	11:20 AM – 12:20 PM

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Wednesday, December 7, 2022

Tutorial

Session Chair: P. D. Ye

8:00 PM – 9:30 PM *Tutorial* – **Reliability Physics for Post-Moore Era Electronics: An Integrated Material, Devices, and System Perspective,** M. A. Alam, *Purdue U.*

Thursday, December 8, 2022

Session 1: Ferroelectrics I

Session Chair: J. Van Houdt

8:20 AM Introduction

8:25 AM 1.1 – **Vertically Stacked Ge GAAFET by Using Diamond-shape Nanowires with Ferroelectric HZO application,** Y.-W. Lin, H.-H. Chang, C.-J. Sun, S.-C. Yan, and Y.-C. Wu, *National Tsing Hua U., Taiwan*

8:45 AM 1.2 – **Engineering $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectricity with Amorphous WO_x Bottom Electrodes Achieving High Remnant Polarization,** Z. Zhao, Y.-R. Chen, Y.-W. Chen, Y. Xing, G.-H. Chen, and C. W. Liu, *National Taiwan U., Taiwan*

9:05 AM 1.3 – **Oxygen-scavenging effect on Si and Ge substrates with $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric films for ultra-low write voltage,** C. Park[1,2], D. Das[1], J. Hur[3], N. Tasneem[1], S. F. Lombardo[1], W. Chern[1], S. Yu[1], and A. Khan[1], [1]*Georgia Institute of Technology,* [2]*SK Hynix, Korea,* [3]*Intel*

9:25 AM 1.4 – **New Insights into Operation and Memory Window Degradation of Oxide Channel FEFET,** M. Passlack[1], K. A. Aabrar[2], and S. Datta[2], [1]*TSMC, Taiwan,* [2]*U. of Notre Dame*

9:45 AM – 9:50 AM Limerick Contest Introduction

9:50 AM – 10:20 AM Coffee Break

Session 2: BEOL Oxides

Session Chair: P. D. Ye

10:20 AM — 2.1 *Invited* – **Oxide Semiconductor Back-end-of-line (BEOL)-Compatible Transistors and Memories,** X. Gong, K. Han, S. Samanta, C. Sun, C. Wang, and Z. Zheng, *National U. of Singapore, Singapore*

10:55 AM — 2.2 – **Highly Gate-Bias-Stress Stable Atomic-Layer-Deposited InZnO TFTs with BEOL-Compatibility,** D. Zheng, A. Charnas, H. Dou, Z. Hu, J. Zhang, H. Wang, and P. D. Ye, *Purdue U.*

11:15 AM — 2.3 – **Effect of V-V dimer on metallic and semiconducting grain boundaries of VO_2,** X. Zhang[1], H. Lu[2], Y. Guo[3], D. P. Chu[1], and J. Robertson[1], [1]*U. of Cambridge, UK,* [2]*Beihang U., China,* [3]*Wuhan U., China*

11:35 AM — 2.4 – **BEOL-Compatible Atomic-Layer-Deposited In-rich InGaO TFTs with High Positive-Gate-Bias-Stress Stability,** J. Zhang, Z. Zhang, D. Zheng, A. Charnas, Z. Lin, and P. D. Ye, *Purdue U.*

Session 3: Advanced Device Technologies

Session Chair: J. Rozen

1:30 PM — 3.1 *Invited* – **Hardware Algorithm Co-optimization for Scalable Analog Compute Technology,** T. Ando, *IBM*

2:05 PM — 3.2 – **Highly Stacked $Ge_{0.95}Si_{0.05}$ Nanowire nFETs Featuring High I_{ON}=140μA (6500μA/μm) at V_{OV}=V_{DS}=0.5V by Low Temperature Epitaxy and Wet Etching,** Y.-C. Liu, C.-Y. Cheng, W.-H. Hsieh, B.-W. Huang, C.-T. Tu, and C. W. Liu, *National Taiwan U., Taiwan*

2:25 PM — 3.3 – **L_g = 50 nm gate-all-around $In_{0.53}Ga_{0.47}As$ nanosheet MOSFETs with selectively regrown $In_{0.53}Ga_{0.47}As$ S/D contacts,** I.-G. Lee[1], H.-B. Jo[1], J.-M. Baek[1], W.-S. Park[1], J.-H. Yoo[1], S.-T. Lee[2], S.-K. Kim[3], J.-G. Kim[3], J. Yun[3], T. Kim[3], J.-H. Lee[1], J.-G. Shin[1], C.-S. Shin[2], K.-S. Seo[2], and D.-H. Kim[1], [1]*Kyungpook National U., Korea,* [2]*KANC, Korea,* [3]*QSI, Korea*

2:45 PM — 3.4 – **Degradation mechanism of vertical nanosheet Tunnel-FETs under constant-voltage-stress and hot-carrier injection stress,** J.-M. Baek[1], Kim[1], H.-B. Jo[1], W.-S. Park[1], S.-M. Choi[1], J.-H. Yoo[1], H.-S. Jeong[1], J.-H. Kim[1], I.-G. Lee[1], S. George[1], M. Kong[2], J. Oh[3], S.-T. Lee[2], H. Jang[2], C. Song[2], S.-K. Kim[4], J. Yun[4], T. Kim[4], H.-M. Kwon[5], J.-W. Shin[6], K.-Y. Shin[6], W. Amir[6], T.-W. Kim[6], and H. Kim[3], [1]*Kyungpook National U., Korea,* [2]*KANC, Korea,* [3]*Sungkyunkwan U., Korea,* [4]*QSI, Korea,* [5]*Korea Polytechnics, Korea,* [6]*U. of Ulsan, Korea*

Session 4: Poster Preview I

Session Chair: W. G. Vandenberghe

3:05 PM — 4.1 – **Studying Polarization "Wake-Up" in $Hf_{0.5}Zr_{0.5}O_2$ Thin Films Using Synchrotron X-ray Diffraction,** B. Saini[1], F. Huang[1], Z. Yu[1], J. D. Baniecki[2], V. Thampy[2], W. Tsai[1], and P. C. McIntyre[1,2], [1]*Stanford U.,* [2]*SLAC National Accelerator Laboratory*

3:06 PM — 4.2 – **AlGaN/GaN HEMT's Ohmic Contact with Graphene interlayer,** H. Xie, H. Hsu, W. Lu, C. Su, and Y. Hsin, *National Central U., Taiwan*

3:07 PM — 4.3 – **Al_2O_3, HfO_2, La_2O_3, ZrO_2/InP interfaces without atomic substitutions or passivation,** X. Zhang[1], Z. Zhang[2], Y. Guo[2], D. P. Chu[1], and J. Robertson[1], [1]*U. of Cambridge, UK,* [2]*Wuhan U., China*

3:08 PM — 4.4 – **Analog Synaptic Behaviors of CeO_2 Memristor Deposited by Atomic Layer Deposition Process,** K. Park, J. Han, and T.-S. Yoon, *UNIST, Korea*

3:09 PM — 4.6 – **Bi Contact Interface and Band Alignment Study on W-based Transition Metal Dichalcogenides,** J. Roy, S. Y. Kim, X. Wang, and R. M. Wallace, *UT Dallas*

3:10 PM — 4.7 – **Two-dimensional SiO_x-cladded Si and GeO_x-cladded Ge Quantum Dot Arrays vertically stacked for CMOS-X Logic, SRAMs, NVRAMs and IR imaging and multi-bit Computing,** F. Jain[1], R. Gudlavalleti[1], R. Mays[1], B. Saman[1,2], P.-Y. Chan[1], J. Chandy[1], M. Lingalugari[3], and E. Heller[4], [1]*U. of Connecticut,* [2]*Taif U., Saudi Arabia,* [3]*Intel,* [4]*Synopsys*

3:11 PM — 4.8 – **Growth of Topological Semimetal CoSi for Scaled Interconnects,** Y. Li, G. Zhou, and C. L. Hinkle, *U. of Notre Dame*

3:12 PM — 4.9 – **Effects of UV treatments on the device performance of MoS_2 FETs,** H. Cho, S. Y. You, D. Kim, and G.-T. Kim, *Korea U., Korea*

3:13 PM — 4.10 – **Design and Evaluation of Nanoscale NbO_2 based Insulator Metal Transition Devices,** K. Beckmann[1], R. R. Mathkari[2], R. Pareis[2], M. Rodgers[1], and N. Cady[2], [1]*NY CREATES,* [2]*SUNY Polytechnic Institute*

3:14 PM — 4.11 – **Physics in Very Shallow Trap Formation at SiC/SiO_2 Interfaces,** K. Shiraishi and K. Chokawa, *Nagoya U., Japan*

3:15 PM — 4.12 – **Quantum Transport Simulation of Metal–Semiconductor Contacts in a Continuum Description,** P. Reyntjens[1,2,3], P. K. R. Baikadi[1], M. L. Van de Put[2], and W. G. Vandenberghe[1], [1]*UT Dallas,* [2]*imec, Belgium,* [3] *U. Leuven, Belgium*

3:16 PM — 4.13 – **Normally-Off $Al_{0.65}Ga_{0.35}N/Al_{0.3}Ga_{0.7}N$/AlN/SiC MOS-HEMTs with USPD-Grown Al_2O_3 Gate Dielectric,** C. S. Lee[1], C. H. Ke[2], W. C. Hsu[2], and C. L. Li[1], [1]*Taiwan Feng Chia U., Taiwan,* [2]*Taiwan Cheng Kung U., Taiwan*

3:17 PM — 4.14 – **Low Frequency Defect Analysis Methods in High-K Metal Gate Stacks for Spin-Qubit Application,** Y. Raffel, R. Olivo, M. Simon, R. Hoffmann, S. De, T. Kämpfe, K. Seidel, and M. Lederer, *Fraunhofer CNT, Germany*

3:18 PM — 4.15 – **In-situ Visualization of Structural Transformations with Sub-ms Time Resolution via Time-Resolved Synchrotron X-ray Scattering of Flash Annealed HZO Thin Films,** M. H. Karigerasi[1], D. Van Campen[1], B. Saini[2], F. Huang[2], A. Mehta[1], P. C. McIntyre[1,2], and J. D. Baniecki[1], [1]*SLAC National Accelerator Laboratory,* [2]*Stanford U.*

3:19 PM — 4.16 – **Enhanced Artificial Synaptic Behaviors in Oxide/suboxide HfO_x Bilayer RRAM Devices,** D. P. Sahu, P. H. Chung, K. Park, J. Han, and T.-S. Yoon, *UNIST, Korea*

3:20 PM — 4.17 – **Selective HfO_2 Chemical Vapor Deposition on SiO_2 in preference to Aniline Passivated W,** J. Huang[1], Y. Cho[1], Z. Zhang[1], K. T. Wong[2], S. D. Nemani[2], E. Yieh[2], and A. C. Kummel[1], [1]*UCSD,* [2]*Applied Materials*

3:21 PM — 4.18 – **Achieving Excellent Neuromorphic Performance of Si:HfO_2-based FeFETs by Interface Fluorination,** Y. Raffel, S. De, R. Olivo, S. Thunder, R. Hoffmann, K. Seidel, T. Kämpfe, and M. Lederer, *Fraunhofer CNT, Germany*

3:22 PM — 4.19 – **A novel approach for analysis of conductance spectra from MoS_2 field effect devices,** E. Reato[1,2], A. Esteki[2], A. Piacentini[1,2], D. S. Schneider[1], M. Otto[1] ,A. Grundmann[2], H. Kalisch[2], Z. Wang[1], M. Heuken[2,3], A. Vescan[2], M. C. Lemme[1,2], and O. Engström[1,2], [1]*AMO GmbH, Germany,* [2]*RWTH Aachen U., Germany,* [3]*AIXTRON SE, Germany*

3:23 PM — 4.20 – **Image Force Potential for Top Contacted Two-Dimensional Materials,** S. R. Evans[1], E. Deylgat[1,2,3], E. Chen[4], and W. G. Vandenberghe[1], [1]*UT Dallas,* [2]*U. Leuven, Belgium,* [3]*imec, Belgium,* [4]*TSMC, Taiwan*

3:25 PM – 3:30 PM — Limerick Contest Introduction

3:30 PM – 3:45 PM — Coffee Break

Session 5: Wide Bandgap Semiconductors

Session Chair: J. Robertson

3:45 PM — 5.1 *Invited* – **Interfaces between GaN and AlN: epitaxy, properties and devices,** H. G. Xing, *Cornell U.*

4:20 PM — 5.2 – **Improved Growth of Low-Temperature GaN for BEOL Transistors,** T. Sun, G. Zhou, J. Shin, R. Younas, Y. Li, and C. L. Hinkle, *U. of Notre Dame*

4:40 PM — 5.3 – **A revisit of the oxidation and passivation mechanisms of SiC/SiO_2 interfaces,** Z. Zhang[1,2], Y. Guo[1], and J. Robertson[2], [1]*Wuhan U., China,* [2]*U. of Cambridge, UK*

5:00 PM — 5.4 – **Crystalline Gallium Nitride Deposition by RF-Biased Atomic Layer Annealing,** P. C. Lee[1], A. J. McLeod[1], S. T. Ueda[1], J. Spiegelman[2], and A. C. Kummel[1], [1]*UCSD,* [2]*RASIRC*

Session 6: Poster Preview II

Session Chair: A. C. Kummel

5:20 PM — 6.1 – **Non-Volatile Charge-Trap Memory Characteristics in the IGZO TFT with UV/Ozone-Treated HfO_{2-x} Charge-Trap Layer for the Formation of Interface Tunneling Oxide,** J. Han, B. Jeong, and T.-S. Yoon, *UNIST, Korea*

5:21 PM — 6.2 – **Low Resistivity Titanium Nitride Thin Film Fabricated by Atomic Layer Deposition with $TiCl_4$ and Metal-Organic Precursors in Horizontal Vias,** C.-H. Kuo[1], A. J. McLeod[1], J. Huang[1], V. Wang[1], S. Yun[1], Z. Zhang[1], J. Spiegelman[2], R. Kanjolia[3], M. Moinpour[3], and A. C. Kummel[1], [1]*UCSD,* [2]*RASIRC,* [3]*EMD Electronics*

5:22 PM 6.3 – **DFT modeling on inversion domain boundaries of piezoelectric AlScN thin films,** T. Hwang[1], W. Aigner[2], T. Metzger[2], A. C. Kummel[3], and K. Cho[1], [1]*UT Dallas,* [2]*Qualcomm, Germany,* [3]*UCSD*

5:23 PM 6.4 – **Understand the Resistive Switching Mechanism of 2D RRAM by Monte Carlo Modeling,** Y. Huang[1], Y. Gu[1], Y.-F. Chang[2], D. Akinwande[1], and J. C. Lee[1], [1]*UT Austin,* [2]*Intel*

5:24 PM 6.5 – **A new opportunity for the emerging tellurium semiconductor: making neuromorphic devices,** H. Li[1,2], Y. Yang[1], and M. Xu[1], [1]*Tsinghua U., China,* [2]*Chinese Institute for Brain Research, China*

5:25 PM 6.6 – **Charge Traps in H Incorporated SiN in 3D NAND Memories,** F. Nanataki, A. Oshiyama, and K. Shiraishi, *Nagoya U., Japan*

5:26 PM 6.7 – **Cold effects in the gate-drivability of 22 nm FD-SOI transistors,** Y. M. Chang, Y. W. Chiu, T. Tsai, C.-H. Lin, and P. W. Li, *National Yang Ming Chiao Tung U., Taiwan*

5:27 PM 6.9 – **Conformal, ultrathin nucleating layers and gate oxides on sp^2 carbon surfaces for HOPG (highly oriented pyrolytic graphite) capacitors and CNT field effect transistors,** Z. Zhang[1], G. Pitner[2], M. Passlack[2], S. Natani[1], A. C. Kummel[1], and P. Bandaru[1], [1]*UCSD,* [2]*TSMC, Taiwan*

5:28 PM 6.10 – **Dual-Functional Nano Helical-Shaped Devices for Self-rectified Memory and Selector Applications,** Y.-C. Chen[1], S. Sarkar[1], J. Gibbs[1], C.-C. Lin[2], and C.-H. Lin[2], [1]*Northern Arizona U.,* [2]*National Applied Research Laboratories, Taiwan*

5:29 PM 6.11 – **Self-selective Bipolar Artificial Synapse with n-ZnO/p-NiO/n-ZnO Structure for Selector-less Crossbar Array Architecture Application,** P. H. Chung and T.-S. Yoon, *UNIST, Korea*

5:30 PM 6.12 – **Optimal Nucleation Method for Plasma Enhanced Atomic Layer Deposition of Crystallized Gallium Phosphide,** S. Yun, C.-H. Kuo, S. T. Ueda, V. Wang, H. Kashyap, A. J. McLeod, Z. Zhang, P. C. Lee, and A. C. Kummel, *UCSD*

5:31 PM 6.13 – **Room temperature synthesis of Silicon nanowires (SiNWs) on a flexible substrate for electronic applications,** N. Arya and R. O. Dusane, *IIT Bombay, India*

5:32 PM 6.14 – **Reduced leakage current obtained in SiC on insulator junctionless MOSFET using high-k dielectric as the buried oxide,** P. Vudumula and S. Kotamraju, *IIIT Sri City, India*

5:33 PM 6.15 – **Ferroelectric N:HfO_2 characterization by synchrotron XPS and electrical analysis and the application on non-volatile ferroelectric field-effect transistor memory,** Y.-J. Yao, C.-J. Sun, S.-H. Chen, G.-L. Luo, and Y.-C. Wu, *National Tsing Hua U., Taiwan*

5:34 PM 6.16 – **Whole Wafer Mapping and Interface Characterization via Cameraless T-ray Imaging,** A. Rahman, *Applied Research & Photonics*

5:35 PM 6.17 – **Using nonlinear electric fields in non-planar geometries for low-voltage operation of Ferroelectric Field Effect Transistor based memory devices,** S. Natani and P. Bandaru, *UCSD*

5:36 PM 6.18 – **Effects of different surface treatments on silicon contact resistivity,** M. Miettinen, E. Vuorinen, J.-P. Lehtiö, Z. Jahanshah Rad, M. Kuzmin, R. Punkkinen, P. Laukkanen, and K. Kokko, *U. of Turku, Finland*

5:37 PM 6.19 – **Simulated dielectric function of a low-K dielectric MOF material in gigahertz regime,** S. Jamnuch, A. C. Kummel, and T. A. Pascal, *UCSD*

5:38 PM 6.20 – **Vapor Deposited MOFs as Low-k Dielectrics for Logic and RF,** W.-J. Lee, C. Swank, G. Samuel, J. Watson, H. Kim, and A. C. Kummel, *UCSD*

5:39 PM 6.21 – **Intermediate phase of V_2O_3 at low-temperature phase transition,** W.-F. Hsu[1], S. Mellaerts[1], M. Menghini[2], J. R. Zuazo[3,4], J. L. Sánchez[3,4], J. W. Seo[1], and J.-P. Locquet[1], [1]*U. Leuven, Belgium,* [2]*IMDEA Nanociencia, Spain,* [3]*European Synchrotron Radiation Facility, France,* [4]*ICMM-CSIC, Spain*

5:40 PM 6.22 – **SiO_2/high-κ induced negative charge in GaAs/SiO_2/Al_2O_3 and Ge/SiO_2/Al_2O_3 interfaces,** J.-P. Lehtiö, Z. J. Rad, M. Miettinen, M. P. J. Punkkinen, R. Punkkinen, P. Laukkanen, and K. Kokko, *U. of Turku, Finland*

5:41 PM 6.23 – **Passive network model of resistance switching materials,** S. J. Lee and S. J. Baik, *Hankyong National U., Korea*

5:42 PM 6.24 – **Producing Black GaAs as Anti-reflection coating on GaAs by a Two-step Wet Chemical Method,** Z. Jahanshah Rad[1], S. Vuori[1], J.-P. Lehtiö[1], K. Iltanen[1], M. P. J. Punkkinen[1], M. Miettinen[1], M. Kuzmin[1], A. Tukiainen[2], J. Viheriälä[2], J. Kozlova[3], M. Rähn[3], A. Tamm[3], P. Laukkanen[1], M. Lastusaari[1], M. Guina[2], and K. Kokko[1], [1]*U. of Turku, Finland,* [2]*Tampere U., Finland,* [3]*U. of Tartu, Estonia*

5:43 PM 6.25 – **Near-Zero-Field Magnetoresistance Investigation of Defects in Packaged Integrated Circuits,** M. J. Elko, S. J. Moxim, F. V. Sharov, and P. M. Lenahan, *Pennsylvania State U.*

5:44 PM 6.26 – **Fabrication of Extreme Density Microdiamond Composites for RF and Logic Heat Spreaders,** C. Swank[1], W.-J. Lee[1], J. Spiegelman[1], S.-M. Chang[2], M. Chen[3], J. Buckwalter[2], E. Pop[3], and A. C. Kummel[1], [1]*UCSD,* [2]*UCSB,* [3]*Stanford U.*

5:45 PM 6.28 – **The Facile integration of giant exchange bias in 2D magnet/oxide heterostructures,** S. Liang, J. Liang, T. Xie, and C. Gong, *U. of Maryland*

5:50 PM End

7:00 PM – 10:00 PM Reception/Poster Session

Friday, December 9, 2022

Session 7: 2D Materials I

Session Chair: P. C. McIntyre

8:00 AM — 7.1 *Invited* – **Reduced Contact Resistances for Moire Lattice Interfaces of MoS_2 and other Layered Compounds,** J. Robertson[1], Z. Zhang[1], and Y. Guo[2], [1]*U. Cambridge, UK,* [2]*Wuhan U., China*

8:35 AM — 7.2 – **Origins of Fermi Level Pinning for Ni and Ag Contacts on Transition Metal Dichalcogenides,** X. Wang, Y. Hu, S. Y. Kim, R. Addou, K. Cho, and R. M. Wallace, *UT Dallas*

8:55 AM — 7.3 – **Ambipolar Contacts at WSe_2/Metal via Moire Interfaces,** J. Chen[1], Z. Zhang[1], Y. Guo[2], and J. Robertson[1,2], [1]*U. of Cambridge, UK,* [2]*Wuhan U., China*

9:15 AM — 7.4 – **Gate oxide charge trapping in 300 mm integrated dual-gate WS_2 FETs,** L. Panarella[1,2], Q. Smets[2], D. Verreck[2], T. Schram[2], D. Cott[2], I. Asselberghs[2], V. V. Afanas'ev[1,2], G. S. Kar[2], and B. Kaczer[2], [1]*U. Leuven, Belgium,* [2]*imec, Belgium*

9:35 AM – 9:50 AM — Coffee Break

Session 8: Ferroelectrics II

Session Chair: M. Passlack

9:50 AM — 8.1 *Invited* – **EWF control of advanced high-thermal-budget RMG gate stack,** H. Arimura, J. Franco, S. Brus, E. Dentoni Litta, and N. Horiguchi, *imec, Belgium*

10:25 AM — 8.2 – **Direct Quantitative Extraction of Internal Variables from Measured PUND Characteristics of Silicon Channel Ferroelectric FETs,** M. Passlack[1], N. Tasneem[2], Z. Wang[2], J. Hur[2], H. Chen[2], V. D.-H. Hou[1], C.-S. Chang[1], M. F. Chang[1], S. Yu[2], W. Chern[2], and A. Khan[2], [1]*TSMC, Taiwan,* [2]*Georgia Institute of Technology*

10:45 AM — 8.3 – **Quasi-static non-volatile capacitive memory window in ferroelectric capacitors for Compute-in-Memory applications,** S. Mukherjee[1,2], J. Bizindavyi[1], S. Clima[1], M. I. Popovici[1], X. Piao[1], K. Katcko[1], S. Yu[3], V. V. Afanas'ev[2], and J. Van Houdt[1,2], [1]*imec, Belgium,* [2]*U. Leuven, Belgium,* [3]*Georgia Institute of Technology*

11:05 AM — 8.4 – **Ferroelectric Reverse Switching based Subthreshold Swing (SS) Improvement of FeFETs,** C.-Y. Liao[1], K.-Y. Hsiang[1,2], Z.-F. Lou[1], C.-Y. Lin[1], F.-S. Chang[1], J.-Y. Lee[1,3], Z.-X. Li[1], H.-C. Tseng[1], W.-C. Ray[1], C.-C. Wang[1], C. W. Liu[3], and M. H. Lee[1], [1]*National Taiwan Normal U., Taiwan,* [2]*National Yang Ming Chiao Tung U., Taiwan,* [3]*National Taiwan U., Taiwan*

11:25 AM — 8.5 – **Memory-in-Logic FETs for Neuromorphic Computing,** X. Ju, D. C. S. Tan, and D. S. Ang, *Nanyang Technological U., Singapore*

Session 9: 2D Materials II

Session Chair: C. L. Hinkle

1:30 PM	9.1 – **Magnetic or non-magnetic? Magnetic impurity doped transition metal dichalcogenides,** R. Younas[1], G. Zhou[1], J. Heron[2], and C. L. Hinkle[1], [1]*U. of Notre Dame,* [2]*U. of Michigan*
1:50 PM	9.2 – **Elemental diffusion at Ni/MoS_2/SiO_2 interfaces,** X. Wang, X. Zhu, S. Y. Kim, M. J. Kim, and R. M. Wallace, *UT Dallas*
2:10 PM	9.3 – **Improved P-Type Performance in Bilayer WSe_2 Transistors,** C. S. Bailey, K. M. Neilson, and E. Pop, *Stanford U.*
2:30 PM	9.4 – **Anomalous Hall Effect in 2D Fe_3GeTe_2/Platinum Heterostructures,** S. Chyczewski and W. Zhu, *UIUC*
2:50 PM	9.5 – **Bi Contact Interface and Band Alignment Study on Molybdenum Disulfides,** S. Y. Kim, J. Roy, X. Wang, and R. M. Wallace, *UT Dallas*
3:10 PM – 3:15 PM	Limerick Contest Introduction
3:15 PM – 3:40 PM	Coffee Break

Session 10: Advanced Characterization Technologies

Session Chair: Y.-C. Chen

3:40 PM	10.1 *Invited* – **Device Engineering and Benefit Maximization for Advanced Cryo-CMOS,** H.-L. Chiang, J.-J. Wu, P.-J. Liao, T.-C. Chen, C.-S. Chang, X. Bao, J. Cai, M. F. Chang, H. Chuang, C. H. Diaz, H.-S. P. Wong, M. Passlack, and I. Radu, *TSMC, Taiwan*
4:15 PM	10.2 – **Optimizing Oxygen Vacancy and Interface Energy Achieving High Remnant Polarization and Dielectric Constants of Respective $Hf_{0.5}Zr_{0.5}O_2$ Superlattice and Alloy Structure,** Y.-R. Chen, Z. Zhao, Y.-W. Chen, Y. Xing , Y. Lin, G.-H. Chen, and C. W. Liu, *National Taiwan U., Taiwan*
4:35 PM	10.3 – **Half-Cycle Study with in-situ Infrared Spectroscopy of Anhydrous Hydrogen Peroxide, Ozone, and Water based HfO_2 Atomic Layer Deposition for Ferroelectric Hafnia based Device Applications,** J.-H. Kim[1], Y. C. Jung[1], S. M. Hwang[1], D. N. Le[1], H. Hernandez-Arriaga[1], K. Tan[1], D. Alvarez[2], J. Spiegelman[2], S. J. Kim[3], and J. Kim[1], [1]*UT Dallas,* [2]*RASIRC,* [3]*Kangwon National U., Korea*
4:55 PM	10.4 – **Interface Engineering to Alleviate Self-Heating Effect in Top-Gated ALD In_2O_3 Transistors,** P.-Y. Liao, K. Khot, S. Alajouni, J. Noh, Z. Zhang, M. Si, A. Shakouri, X. Ruan, and P. D. Ye, *Purdue U.*
7:00 PM – 10:00 PM	Conference Banquet & Limerick Contest

Saturday, December 10, 2022

Session 11: Ferroelectrics III

Session Chair: X. Gong

8:00 AM — 11.1 *Invited* – **Ferroelectric field-effect transistors: Reliability and logic compability,** D. Das, N. Tasneem, and A. Khan, *Georgia Institute of Technology*

8:35 AM — 11.2 – **Enhanced Ferroelectricity in $Hf_{0.5}Zr_{0.5}O_2$ Thin Film with Amorphous Underlayer,** Y.-W. Chen, Y.-R. Chen, Z. Zhao, Y. Xing, G.-H. Chen, and C. W. Liu, *National Taiwan U., Taiwan*

8:55 AM — 11.3 – **Multilevel Functionality of $Al_{0.4}Sb_{0.6}$ Phase Change Memory,** R. Ume, H. Gong, M. Yakimov, V. Tokranov, K. Brew, G. Cohen, K. Beckmann, N. Cady, and S. Oktyabrsky, *SUNY Polytechnic Institute*

9:15 AM – 9:30 AM — Coffee Break

Session 12: 2D Materials III

Session Chair: A. Khan

9:30 AM — 12.1 *Invited* – **Efficient Control of 2D Magnets,** C. Gong, *U. Maryland*

10:05 AM — 12.2 – **Enhancing Atomic Diffusion Using 2D Materials for Low-Temperature High-Quality Growth of 3D Semiconductors,** G. Zhou, R. Younas, T. Sun, Y. Li, and C. L. Hinkle, *U. of Notre Dame*

10:25 AM — 12.3 – **Reconfigurable Transistors Based on van der Waals Heterostructures,** J. Kang, S. Rakheja, and W. Zhu, *UIUC*

10:45 AM — 12.4 – **Comparing Semi-Classical Models for Contact Resistivities in Top- and Side-contacted Two-Dimensional Materials,** E. Deylgat[1,2,3], E. Chen[4], M. L. Van de Put[3], M. V. Fischetti[1], B. Sorée[2,3,5], and W. G. Vandenberghe[1], [1]*UT Dallas,* [2]*U. Leuven, Belgium,* [3]*imec, Belgium,* [4]*TSMC, Taiwan,* [5]*U. of Antwerp, Belgium*

11:05 AM–11:20 AM — Coffee Break

Session 13: Emerging Technologies

Session Chair: C. Gong

11:20 AM — 13.1 – **Mott physics in corundum-based superlattices,** S. Mellaerts[1], W.-F. Hsu[1], M. Houssa[1,2], J. W. Seo[1], and J.-P. Locquet[1], [1]*U. Leuven, Belgium,* [2]*imec, Belgium*

11:40 AM — 13.2 – **Ultra Low Resistivity Ru via ALD,** V. Wang[1], M. Breeden[1], C.-H. Kuo[1], M. Bergschneider[2], N. Ashburn[2], X. Lang[2], A. Jog[3], H. Simka[4], R. Kanjolia[5], M. Moinpour[5], J. Woodruff[5], K. Cho[2], D. Gall[3], and A. C. Kummel[1], [1]*UCSD,* [2]*UT Dallas,* [3]*Rensselaer Polytechnic Institute,* [4]*Samsung,* [5]*EMD Electronics*

12:00 PM — 13.3 – **Low-Temperature CF_4/N_2O Plasma Treated In_2O_3 Thin Film Transistors with Excellent Bias Stability,** J. Zhang, A. Charnas, Z. Lin, D. Zheng, Z. Zhang, P.-Y. Liao, and P. D. Ye, *Purdue U.*

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