3D sequential integration: an alternative path towards CMOS scalability
Outline

What is 3D sequential integration?

Why 3D sequential integration?

Key technological modules
Outline

What is 3D sequential integration?

Why 3D monolithic integration?

Key technological modules
3D sequential integration flow

1/ Bottom Layer process

2/ Top active creation

Thermal budget limitation is needed

3/ Top FET process

4/ 3D contact formation
Difference with 3D packaging

Packaging integration (e.g.: TSV)

1/ Wafers processed separately

2/ Stacking and contacting

Sequential integration

1/ Bottom Layer process

2/ Top layer process

3/ 3D contact formation

Packaging integration: stacked MOSFETs processed in separately
Sequential integration: stacked MOSFETs processed sequentially
3D sequential integration: advantage & challenge

Major asset: Highest 3D contact density

Packaging integration (e.g. TSV)

Sequential integration

3D TSV contact pitch 3-8µm
3D contact density $10^4 - 10^5 / \text{mm}^2$

Two reasons for the high 3D contact pitch:
- Alignment performance
- 3D contact process

3D contact pitch <100nm
3D contact density $> 10^8 / \text{mm}^2$

Major challenge: Process top MOSFET at low thermal budget
Alignment performance with sequential 3D

**SEQUENTIAL 3D**
- Blanket top active
- Standard lithography

**PACKAGING 3D**
- Bonding of patterned films
- Alignment & bonding at the same time

**Sequential 3D:** alignment obtained by lithography. Litho stepper capability $\sim 3\sigma=5$nm

**Packaging 3D:** alignment made during bonding. Bonding stepper capability $3\sigma \sim 1\mu$m

[1] www.besang.com
3D contact integration scheme

3D contact process similar to a standard planar W plug process

Contact in an oxide with a slightly higher depth

No keep out of zone
3D contact density

D = Density = Number of 3D contacts per mm²

[3,4]: P. Garrou et al., Handbook of 3D integration, Vol 1,2 (Wiley ed) / [5]: B. Banijamali, ECTC2011
Partitioning levels

1-Entire core

2-Logic bloc

3-Logic gates

4-Transistors

Granularity scale

3D packaging

3D sequential
Outline

What is 3D sequential integration

Why 3D sequential integration
  1-Road map driven by FET performance
  2-Road map driven by interconnection delay reduction
  3-Opportunities of heterogeneous cointegration

Key technological modules
1- Roadmap driven by FET performance
1- Roadmap driven by FET performance

- 28nm (2012)
- 14nm (2014)
- 10nm (2016)
- 7nm (2018)

- 28FDSOI
- 14FDSOI
- 10FDSOI

Electrostatic: Non planar/trigate

Mobility boost

**Finit**

Performance boosters are different for N & PFETs

Independant N&P optimization is easier with P/N stacking
N/P configuration: boosting FET performance

→ Enable to choose the best
- Material
- Gate stack
- Strain
- Orientation
- Architecture

[1]: P. Batude et al., VLSI 2009
[2]: P. Batude et al., IEDM 2009
The ultimate cointegration III-V and (Si)Ge

nFET III-V and pFET Ge process are highly different:
Dual active etching/ Dual Gate stack/ Dual RSD/ different optimum architecture/ Dual salicidation/Substrate fabrication: dual material (epi with ART or III-V bonding on GeOI)...

Processing independantly n&pFET on distinct levels enable to save a lot of lithography levels and process co-integration challenges.

Additionnaly, III-V and Ge transistors requires lower thermal budget process. These devices are well adapted to 3D sequential integration.

T. Irisawa et al., VLSI 2013 (AIST)
**Choice of architectures**

<table>
<thead>
<tr>
<th>Bottom transistor</th>
<th>top transistor</th>
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<td>Trigate</td>
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<tr>
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For bottom level, every existing technology can be used.
On top level, all the thin film technology can be used.
Parallel 3D
Sequential 3D

Granularity scales
1-Entire core
2-Logic bloc
3-Logic gates
4-Transistors

Partitioning levels

Packaging 3D
N/P or P/ N stacking
→ IC Gain obtained by boosting FET performance
2- Roadmap driven by interconnection delay
2- Roadmap driven by interconnection delay

IC’s performance are strongly limited by interconnection delay

Wirelength must be reduced to benefit from gate delay reduction
Partitioning levels

Sequential 3D

Granularity scale

Packaging 3D

CMOS/CMOS stacking

→ IC Gain obtained by decreasing wirelength
CMOS/ CMOS option: Reducing wirelength

The 3D contact links blocks of MOSFETs

To avoid routing congestion, introduction of intermediate lines is mandatory.
PPA gain thanks to wirelength reduction

Case of FPGA circuit
14nm planar FDSOI versus 2 stacked 14 nm FDSOI levels

Study taking into account parasitics / 3 metal line between the 2 stacked layers
Partitioning SRAM memory on bottom level, logic on top

Top metal layers
local interco W
Metal lines Cu et low-k

3D contact

Interlevel metal lines in W
No low k dielectrics
Analysis on a specific application: FPGA

- Power Performance Area (PPA) benchmark for 3D versus planar
  - Area gain = 55%
  - Perf gain = 23%
  - Power gain = 12%

- Decreased delay and power due to shorter wirelengths
  - reduced wire capacitance
  - less signal buffering requirement

1,5 node gain without scaling
Stacking 14nm/14nm leads to PPA below 10nm
Specific caution for IC performance evaluation

N°1: Evaluation gain will depend on the considered node and on technology hypothesis (Design Rule Manual)

PPA on FPGA for 65nm² vs 65nm
[1]: P. Gaillardon et al., CASFET 2012

No intermetal lines
Area gain: 21% in average
Delay gain: 22% in average

PPA on FPGA for 14nm² vs 14nm
[2]: O. Turkyilmaz et al., DAC 2014

3 level of intermetal lines
W lines, no low-k dielectrics
Area gain: 55% in average
Delay gain: 23% in average

Evaluation gain will depend on the considered node
Specific caution for IC performance evaluation

N°2: No place & route (P&R) tool adapted for 3D

- Results provided only for FPGA thanks to its regular architecture that can be achieved with full custom layout.

- P&R tool enable to optimize the position of the cells to obtain the best gain (in term of area, timing or power).

- Preliminary evaluation via « DIY » P&R tools.

Reliable conclusion can’t be provided without dedicated 3D P&R tool.
N° 3: PPA Gain will highly depend on the application

Evaluation for ASiCs
45nm node/ 1 intermediate level only / with 2D modified P&R tool

Gain depends on the application
Evaluation on FPGA is feasible thanks to its regular design (Full custom layout possible).

FPGA with two 14 nm stacked levels should enable to outperform the 10nm

Stacking more efficient than scaling?

No modification of transistor technology (tool reuse)

Gain obtained only due to wirelength reduction
Specific cautions to make a proper PPA benchmark:

# 1: Evaluation for other ICs cannot be properly performed due to the lack of 3D P & R tool → work with EDA providers is necessary

#2: The results will greatly depend on the IC (predominance of delay in interconnection delay in the full IC performance)

#3: The result will greatly depend on the considered node (predominance of delay in advanced nodes)

#4: Technology assumptions must be analyzed carefully, particularly the number of intermediate lines authorized as well as the metal and dielectrics chosen.
3- A key technology for heterogeneous co-integration

Advantages of 3D

→ Independant optimisation of each level

→ Proximity between stacked functions

Only 3D sequential technology available if 3D contact pitch is smaller than 1µm
3D integrated CMOS Image Sensors (3D-CIS)

Concept: Vertical dissociation of basic pixel operations

Advantages of 3D configuration:
- Photodetection $\rightarrow$ dedicated material and processes, 100% fill factor
- Readout transistors $\rightarrow$ optimized process, relaxed geometries
- Signal Processing $\rightarrow$ Massively parallel treatment, dense IC integration
Miniaturized 3D CMOS Image Sensors

Innovative miniaturized 4T pixels with backside illumination (BSI)\textsuperscript{[24]}

- Bottom layer: pinned photodiode + Transfer Gate
- Top layer with 3 transistors

Multiple benefits
- BSI integration $\rightarrow$ high quantum efficiency
- Photodiode area +44\% for 1.4μm pitch pixel

Only sequential integration can address these dimensions
The challenge of detecting NEMS resonance: NEMS-CMOS integration schemes

**Stand-alone NEMS + off-chip CMOS**
No density (pads number limitation)
Very strong signal attenuation (LP filter)

**3D sequential NEMS-CMOS**
No density limitation
No signal attenuation

NEMs = ultra sensitive mass sensors used for gas sensing & mass spectroscopy

MEMS → NEMS enable to increase the sensitivity
but resonance detection is more complex

3D sequential NEMS-CMOS co-integration can solve the NEMS density and detection limitation

Contribution of J. Arcamone from leti
3D sequential integration of sensors with CMOS

**Moving to NEMS array**: i.e each NEMS is individually addressed.

→ Multiple benefits: increased robustness (redundancy), better SNR (averaging NEMS individual response, provide a spatial response (like an imager), ultra-high density to improve capture efficiency (smaller concentration detection)

→ **NEMS array enables novel NEMS-based applications such as mass spectrometry**

At this scale, only 3D sequential integration enable to reach the 3D contact pitch required (NEMS dimensions converge towards CMOS transistors)

Easy integration of NEMS thanks to it low thermal budget.

→ **3D sequential is well adapted for NEMS array**

Rmk: same benefits applicable to other domains such as NEMS-based logic
Outline

What is 3D sequential integration

Why 3D sequential

1-Road map driven by FET performance
2-Road map driven by interconnection delay reduction
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Key technological modules

1-Maximum top layer thermal budget determination
2-Top active creation
3-Top FET at low temperature process
General Integration Flow

Bottom FET process

Low temperature
Top active layer

Low temperature
Top FET process

Which thermal budget?
Part III - Key technological modules

1- Maximum top FET thermal budget determination
Making 3D sequential integration possible

Standard FET process TB: up to 1000-1100°C

Standard FET stability: 400°C i.e. temperature of BEOL process
Making 3D sequential integration possible

Standard FET process TB: up to 1000-1100°C

Standard FET stability: 400°C i.e. temperature of BEOL process

Interlayer dielectric (ILD)

Buried Oxide (BOX)

Si substrate
Bottom FET stability

• Simple method: Annealing of a transistor and observe what is the critical thermal budget for preserving its performance.

• This critical thermal budget will depend on the technology (BULK, FINFET, FDSOI) and the node analyzed.
FDSOI with implanted Si RSD stability

FDSOI with implanted RSD: max thermal budget = 500°C
FDSOI with implanted Si RSD stability

- No impact of the different anneals shown on multiple key electrical parameters such as:
  - DIBL, short channel mobility evidencing no additional dopant diffusion
  - EOT regrowth and reliability (NBTI & PBTI) evidencing good stability of the gate stack
FDSOI with implanted Si RSD stability

- 550°C 1h30: anneal degrades the silicide on NMOS and PMOS

Need to improve NiPt 10% silicide thermal stability
NiPt silicidation associated with W offers higher thermal stability
Bottom FET stability

Techno 1: FDSOI [1]
-Si channel
-Si RSD and implanted source & drain
-NiPt 10% salicidation
→ Performance degradation above 500°C, 5h

Techno 2: FDSOI with additional boosters [2]
-Si channel for NFET, SiGe for pFET
-SiGe:B & SiC:P in situ doped source & drain
-NiPt 15% salicidation
→ No Performance degradation up to 550°C 2h & 500°C 5h

Weak point of MOSFET technologies is salicide stability

Improving salicide stability could relax top FET maximum thermal budget

Most secure criteria: max thermal budget= 500°C (5h)
Bottom FET stability

Top FET maximum thermal budget for bottom strata stability

Thermal Budget: Temperature and time

MOSFET stability?

Cu interconnects stability?

Work is needed to determine max temperature for shorter anneals duration

10^{-6} ns laser

10^{-3} DSA

1 RTA

10^3 Furnace

Duration (s)


Part III - Key technological modules

2- Low temperature top active layer creation

Objective:
high crystalline quality/ controlled thickness/ Max TB =500°C
Cristallization of amorphous Silicon

Finding solutions to increase the size of the grains at temperature compatible with bottom MOSFET integrity
Cristallisation of amorphous Silicon

Example of laser annealing

Rmk: Not a lot of application can tolerate the performance dispersion brought by the poly-Si
“Seed window” techniques

To obtain the control of the grain boundaries position and grain orientation.
“Seed window” techniques

<table>
<thead>
<tr>
<th>Lateral epitaxy</th>
<th>Solid Phase recrystallization</th>
<th>Liquid Phase recrystallization</th>
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</table>
| [Diagram of Lateral epitaxy with \( \text{SiO}_2 \) and \( \text{c-Si} \) layers]  
  Lateral epi\( \sim 650^\circ \text{C} \), min  
  S-M. Jung et al., VLSI 2007 |  
  [Diagram of Solid Phase recrystallization with \( \text{SiO}_2 \) and \( \text{c-Si} \) layers]  
  amorphous deposition  
  thermal anneal (\( 600^\circ \text{C}, h \))  
  Liu et al., IEDM 2010 |  
  [Diagram of Liquid Phase recrystallization with \( \text{SiO}_2 \) and \( \text{c-Si} \) layers]  
  amorphous deposition  
  laser local fusion (ns)  
  Y-H. Son et al., VLSI 2007 |

Remark: Too high thermal budgets applied to the bottom MOSFET
“Seed window” techniques

Important challenges needed to be addressed:

- Thickness control is mandatory
- Suppression of crystalline defects
- Reduction of seed window surface penalty

Liquid phase recrystallization on Si with laser

Liquid phase recrystallization on Ge with RTP

Y-H. Son et al., VLSI 2007 & ECS 2013, Samsung

J. Feng et al., EDL 06, Stanford
μ-Czochralski

Enable to grow a monocrystalline semiconductor seed on an oxide
Control of grain position

Could solve the thermal budget issue, but some points need to be improved:
- The window is large: important loss in density
- The window is deep: very high aspect ratio for 3D contact
- The thickness of the film is highly variable
Carbon nanotubes

Decoupling high temperature CNT growth and 3D sequential integration

H. Wei et al., IEDM 2009
BULK direct bonding and ion slicing

- CMP planarization
- Hydrophilic bonding
  Thermal anneal (200°C)
- SiO₂
- H+ implant
- BULK
- Splitting 200-500°C
- Bulk
Examples of ion slicing reports on bottom MOSFET level

D-S. Yu et al., IEDM 2004, Nat'l Chiao-Tung Univ, Taiwan

L. Xue et al., TED 2003, Cornell university

Patterned reports might be due to:

- Non perfect CMP

- Bonding done with deposited oxide (which contains $H_2O$), patterning avoid the defect due to degassing

$\Rightarrow$ Solutions described in the following slides

F. Crnogorac et al., JVSTB 2010, Stanford
SOI direct bonding

CMP planarization

Hydrophilic bonding
Thermal anneal (200°C)

Selective etching

Grinding
High quality top film

Blanket Si film on top of a bottom transistor layer:

Stack cross section

Top view:

Acoustic characterization:

Full transfer on processed 300 mm wafers
## Top active creation techniques benchmark

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**Notes:**
- PMD oxide
- SW

**Additional notes:**
- Thermal budget:
  - Seem incompatible with bottom max TB
  - Ok with ns laser
  - <400°C
- Description of Seed window (SW) Poly-Si Wafer bonding
# Top active creation techniques benchmark

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- Not compatible with high performance devices

**References**

- [5]
- [6]
- [7]
- [8]
- [9]
- [10]
- [3]
- [11]
- [12]
- [13]
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**Density limitation**
Too high thermal budget
## Seed window (SW) vs Poly-Si vs Wafer bonding

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**Density limitation**

**Too high thermal budget**
More details on direct bonding flow

1- CMP

2- Bonding SOI

3- Start top FET process

Constraints brought by 3D sequential integration vs std direct bonding:

- Deposited oxides
- Planarization of topography
- Unusual MEOL→FEOL flow
Importance of perfect CMP and particle-free bonding surface

Requirements:
Particle free surface and/or adapted oxide thickness
Perfect CMP
Solution for bonding with deposited oxides at Low Temp

Degassing phenomenon:

H₂O contained in deposited oxide (not ideal thermal SiO₂)

Diffusion of water T>150°C And oxydation of top silicon

Hydrogen production
Defect apparition

L. Brunet et al, ECS fall meeting 2014
Solution for bonding with deposited oxides at Low Temp

Solution proposed → $\text{Si}_3\text{N}_4 \text{H}_2\text{O}$ barrier to avoid Si oxidation

TOP MOS stack
- Si 7nm
- H$_2$O barrier layer
- SiN

BOTTOM MOS stack
- Si 750µm

RT 200°C 2h
400°C 2h
600°C 1h

3nm SiN barrier
5nm SiN barrier
Part III - Key technological modules

3-Top FET process at low temperature

(1) Bottom FDSOI FET

(2) Top active layer

(3) Top FET
Low temperature MOSFET main challenges

**TOP FET PROCESS**

- Dopant activation: >1000 °C
- Silicon epitaxy: 750 °C
- Spacer deposition: 600 °C

**BOTTOM FET PROCESS**

- Dopant activation
- Silicon epitaxy
- T_{MAX}<500 °C
Low temperature top transistor

Thermal activation 1000°C → Solid Phase Epitaxy (SPE)

Amorphization

Recrystallization <600°C

Buried Oxide (BOX)

Si substrate
Low temperature dopant activation

- 6nm Si channel
- SiO$_2$/HfSiON/TiN patterning
- First Si$_3$N$_4$ spacer
- Raised S/D epitaxy (Si: nFET / SiGe: pFET)
- Low Doped Drain implantation
- Second spacer
- High Doped Drain implantation
- LT=600 °C / HT=1050 °C anneal
- Salicidation

**pFET** Ge preamo B implant

**nFET** As implant
SPER activated FDSOI devices

SPER process leads to similar performance than High T activation

→ High dopant activation level with 600 °C process
SPER activated FDSOI devices

→ Standard drawbacks observed on bulk devices:
  - Junction leakage increase
  - Deactivation

→ SPER FDSOI device do not present same drawbacks, why?
Solid Phase Epitaxial Regrowth

- Amorphizing implant (e.g. As or Ge + B)

- Regrowth during LT anneal (≤ 600° C)

EOR defects formation below former amorphous-cristalline interface
End of Range (EOR) formation

Two phenomena during anneal:

1- Defects growth through an Oswald ripening process

interstitials → SMICs → {311} → Dislocation loop

2- EOR defects dissolution via recombination at the interfaces

BOX= New recombination interface
End of Range defects in FDSOI vs BULK

1. During implantation

- **BULK**
  - Less interstitials in the c-Si film → Less EOR defects

2. During recrystallisation

- **FDSOI**
  - BOX = New recombination interface → More EOR dissolution

- B. Sklenard et al., ULIS 2012
Junction leakage

KMC simulations
Low T activation

For thin channel, no EOR defects at the channel entrance
→ No junction leakage increase

B. Sklenard et al., ULIS 2012
Boron deactivation for thin SOI and BULK

Rs sheet evolution with post activation anneal (spacer, BEOL..)

Boron deactivation can be suppressed for Tseed = 5nm
Dopant deactivation in SOI

EOR evolution with post anneals

Original situation after recrystallisation anneal (original EOR reservoir is smaller in thin SOI)

During post anneal: emission of interstitial Si atoms from the EOR joining the closest sink

Scaling $T_{seed}$ enable to:
- reduce original EOR concentration
- reduce the Si$_i$ flux crossing the highly activated region
  avoiding formation of inative Boron interstitials clusters
Optimizing the sheet resistance

- HT : 1050°C spike annealing
- LT : 2min 600°C SPER

- Applying HT POR implant conditions leads to severe resistance degradation
- Reducing implanted dose, $R_{\text{sheet}}$ reduced for both As and P

22nm SOI doped by ion implantation

L. Pasini et al., IWJT 2013
**Optimizing the sheet resistance**

**Dopant Clustering**: above a certain dopant concentration, for a given $T$, part of the dopant forms inactive clusters.
Optimizing the sheet resistance

\[ R_{\text{sheet}} = \int_{x}^{1} \frac{1}{eC(x)\mu(x)} \, dx \]

C: active concentration, \( \mu \): mobility of carriers

eXtraction by Hall measurements

Implantation with concentration higher than clustering limit degrades either the active level and/or carrier mobility

Dopant concentration must not exceed the clusterisation limit

L. Pasini et al., IWJT 2013
Main learnings from SPER junctions optimization

• FDSOI is a key asset for low temperature junction

Indeed EOR concentration reduction enable to supress:

  – Junction leakage issues

  – Boron deactivation phenomenon

• Optimization of dopant concentration is needed in order to avoid important clusterization phenomena

• SPER activated devices have similar performance than HT spike activated devices
Solutions for activation in 3D sequential integration

Top FET maximum thermal budget for bottom strata stability

Temperature (°C)

1100
1000
900
800
700
600
500
400

Duration (s)

10^{-6}
10^{-3}
1
10^{3}

Nanosecond laser
DSA
RTA
Furnace

MOSFET stability (under evaluation)

Interconnection stability (under evaluation)

SPER

MOSFET stability
Already known
Solutions for activation in 3D sequential integration

Local anneal region

Top FET maximum thermal budget for bottom strata stability

MOSFET stability
To evaluate

Interconnection stability to evaluate
Laser activation

Efficiency of laser ns anneal to activate dopants proven

Protection of bottom MOSFET during laser anneal validated

→ Promising techniques for dopant activation

→ Additional work is needed to evaluate its’ interest for 3D sequential integration:
  Find the laser anneal conditions to have the best gate/source-drain selectivity
  Evaluation of 3D pattern effect on scaled design rules and versus density
  Evaluation on thin SOI devices
  Compatibility with scaled ILD thicknesses

→ Some answers to be found in C. Fenouillet IEDM 2014 paper
Microwave annealing

- Equivalent activation level at 150°C lower than SPER

- Promising techniques for dopant activation

- Additional work is needed to evaluate its’ interest for 3D sequential integration:
  Evaluation of metal interconnections (temperature depending on conductivity)
Low temperature MOSFET main challenges

BOTTOM FET PROCESS

Dopant activation

TOP FET PROCESS

Silicon epitaxy

$T_{\text{MAX}} < 500 \, ^\circ\text{C}$

Spacer deposition

$>1000 \, ^\circ\text{C}$

$750 \, ^\circ\text{C}$

$600 \, ^\circ\text{C}$
Low temperature MOSFET main challenges

BOTTOM FET PROCESS

TOP FET PROCESS

Dopant activation

Silicon epitaxy

Spacer deposition

500 °C

$T_{MAX} < 500 ^\circ C$

750 °C

600 °C
Low temperature MOSFET main challenges

**BOTTOM FET PROCESS**

- Dopant activation: 500 °C

**TOP FET PROCESS**

- Silicon epitaxy: 750 °C
- Spacer deposition: 600 °C
- $T_{\text{MAX}} < 500 °C$
Low temperature epitaxy

Goal: Obtain a selective epitaxy on the source & drain

Standard process: dichlorosilane and HCl flow together

dichlorosilane: deposition of Si and etch on oxide isolation
HCL: etching on nitride spacer

Reasonable deposition rate cannot be obtained at temperature below 750°C
Low temperature epitaxy

Cyclic Deposition Etch (CDE) process

Step 1 - non selective growth

Step 2 - selective etch steps

→ Use disilane instead of dichlorosilane enable to increase Si deposition rate

→ Addition of GeH4 to HCl enable to increase the etching speed
Low temperature epitaxy

Dramatic decrease of Epitaxy thermal budget is achievable via CDE process

Si epitaxy @600°C

SiGe 35% epitaxy @500°C
J-M. Hartmann et al., ECS journal 2014

Use of new precursor for deposition such as Si$_3$H$_8$ and Cl$_2$ for etching are promising for further thermal budget reduction [M. Bauer et al., Thin Solid Fim 2012]

Work is still needed to lower the epitaxy down to 500°C
Low temperature MOSFET main challenges

**BOTTOM FET PROCESS**

- Dopant activation
- SiGe epitaxy @500°C

**TOP FET PROCESS**

- Dopant activation
- Si epitaxy @600°C
- 500 °C
- 600 °C
- Spacer deposition

$T_{MAX} < 500$ °C
Low temperature spacer

Requirements:
- Resistance against HF chemistry (epitaxy pre-clean)
- Stability against subsequent epitaxy thermal budget
- Conformal

Some Low-k spacers seem well adapted: Low temperature (<500°C) and low-k (<6) for parasitic capacitance reduction and delay improvements

+20% on RO speed with SiCBN 550°C (k~5.2)

SiOCH (k~3)

Rmk: std deposition temp ~ 400°C
Low temperature MOSFET main challenges

BOTTOM FET PROCESS

TOP FET PROCESS

Dopant activation
600 °C
Si epitaxy @600 °C
Spacer deposition

500 °C
SiGe epitaxy @500 °C

$T_{\text{MAX}} < 500 \, ^\circ\text{C}$
Low temperature MOSFET main challenges

**BOTTOM FET PROCESS**

**TOP FET PROCESS**

\[ T_{MAX} < 500 \, ^\circ\text{C} \]
Some examples of 3D sequential demonstrations

3 level stacking!
Seed window configuration
SRAM butterfly curves

S³ SRAM technology from Samsung
Dopant activation by high temperature spike anneal *
Top active creation by Selective Epitaxy Growth or laser liquid phase recrystallisation**

*Impossible with intermetal lines
** Incompatible with bottom MOSFET stability at advanced nodes and high loss in density due to seed window area penalty
Some examples of 3D structures

Ultimate CMOS technology from AIST (InGaAsOI nFET on SGOI pFET)
SBH adaptation with appropriate metallization
Top activate creation by In GaAs Direct Bonding

Full 350°C process for top FET!

Inverter

Ring oscillator
Transistor and Memories with vertical channel

Surrounding gate transistor from Besang
Top activate creation by direct bonding
Dopant activation made before wafer report

Technology licensed by Hynix
Thin Film Transistor (Poly-Si)

High variability due to grain variable orientation and grain boundaries

Low performance compared to crystalline channel

« Epi-like Si FET » from NDL
Dopant activation by thermal activation at unknown temperature
Top activate creation by crystallization of amorphous deposition by laser annealing
Carbon nanotubes

Full CNT-FET process below 250°C

Carbon nanotubes transistors from Stanford
Top activate creation obtained by report of carbone nanotube
Some examples of 3D sequential demonstrations

Cool Cube™ technology from Leti
Dopant activation by SPER
Top active creation by SOI direct bonding

P. Batude et al., VLSI 2011, Leti
Conclusion

3D sequential integration leads to ultra high 3D contact density
1x10^6/mm² is demonstrated/ > 1x10^8/mm² is achievable with 14 nm technology

Roadmap driven by transistor performance: 3D monolithic N/P
Main advantage: easier and cheaper way to optimize the transistors’ performance
a path for III-V cointegration with Ge

Roadmap driven by IC performance: 3D mono CMOS/CMOS
a path for reducing interconnection delay penalty
Stacking instead of scaling: Reaching n+1 node with n node technology

Cointegration of heterogeneous functions requiring small grain partitionning
Highly miniaturized CMOS image sensors/ NEM with CMOS
Conclusion

**Bottom transistor preservation:**

Preserved at 500°C for hours (FDSOI with NiPt salicide)

Solution might be available to increase salicide stability above to 500°C

**Top transistor process:**

- Direct bonding enable to achieve top active layer equivalent to bottom substrate

- Dopant activation with SPE activation leads to similar performance than the high temperature standard process

- FDSOI is a crucial asset to achieve high performance LT CMOS (EOR reduction)

- Laser (nanosecond) is a promising option for dopant activation thanks to local annealing of top layer
Thank you to all co-authors and colleagues that have been working on Cool Cube™


Thank YOU for your attention

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