A Tutorial on Reliability Physics for Post-Moore Era Electronics: An Integrated Material, Devices, and Packaged Systems

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The Endless Frontier of Moore's Law!

Intel LabDay Presentation, 2020

- Moore's law is dead, long-live Moore's law
- Self-heated FEOL transistors: An enduring challenge
- BEOL-integrated transistors: The next-frontier?
- Rethinking the reliability of power-transistors
- Reliability of 3D Heterogeneously Integrated Package
- Looking ahead: A zero-trust world, active packaging

Computing

Transport

Agriculture

Energy

Healthcare

Zero-trust reliability

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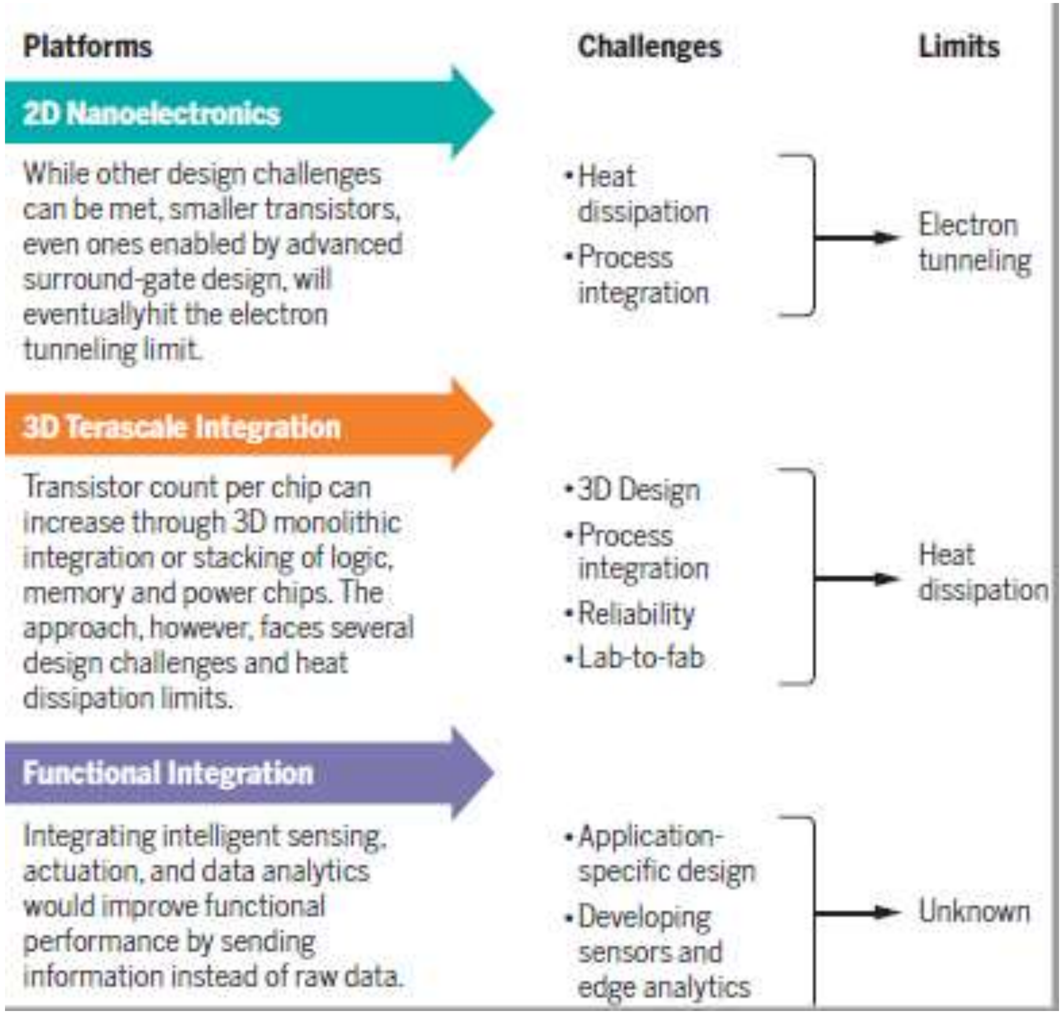
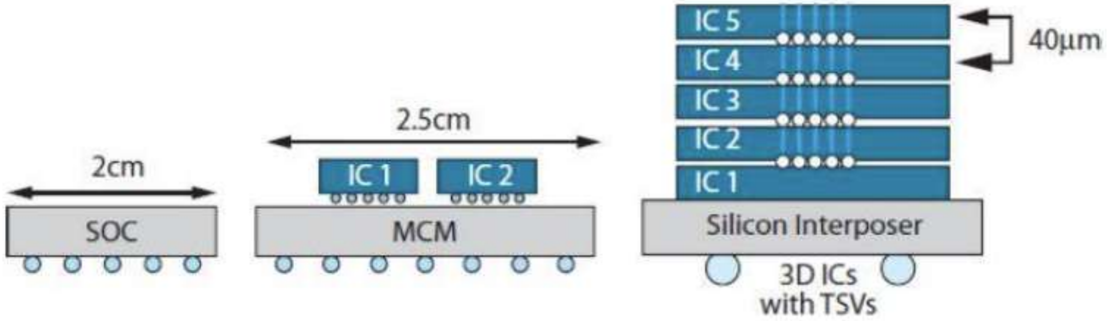
Why SISC will always remain relevant!



Platforms	Challenges	Limits
2D Nanoelectronics While other design challenges can be met, smaller transistors, even ones enabled by advanced surround-gate design, will eventuallyhit the electron tunneling limit.	• Heat dissipation • Process integration	Electron tunneling
3D Terascale Integration Transistor count per chip can increase through 3D monolithic integration or stacking of logic, memory and power chips. The approach, however, faces several design challenges and heat dissipation limits.	• 3D Design • Process integration • Reliability • Lab-to-fab	Heat dissipation
Functional Integration Integrating intelligent sensing, actuation, and data analytics would improve functional performance by sending information instead of raw data.	• Application-specific design • Developing sensors and edge analytics	Unknown

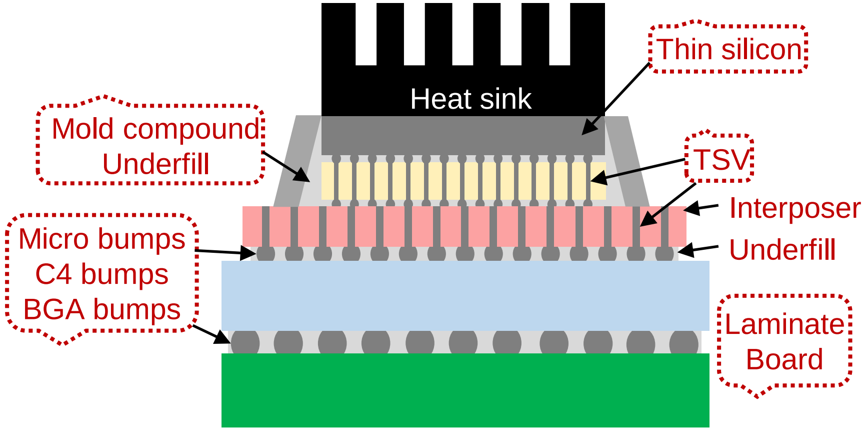
Lundstrom / Alam, Science, 2022



Better Performance!

Smaller Form-factor!

Lower Cost!



*2019 IRPS Tutorial, K. Lee, SK Hynix

Outline

- Moore's law is dead, long-live Moore's law
- Self-heated FEOL: An enduring challenge
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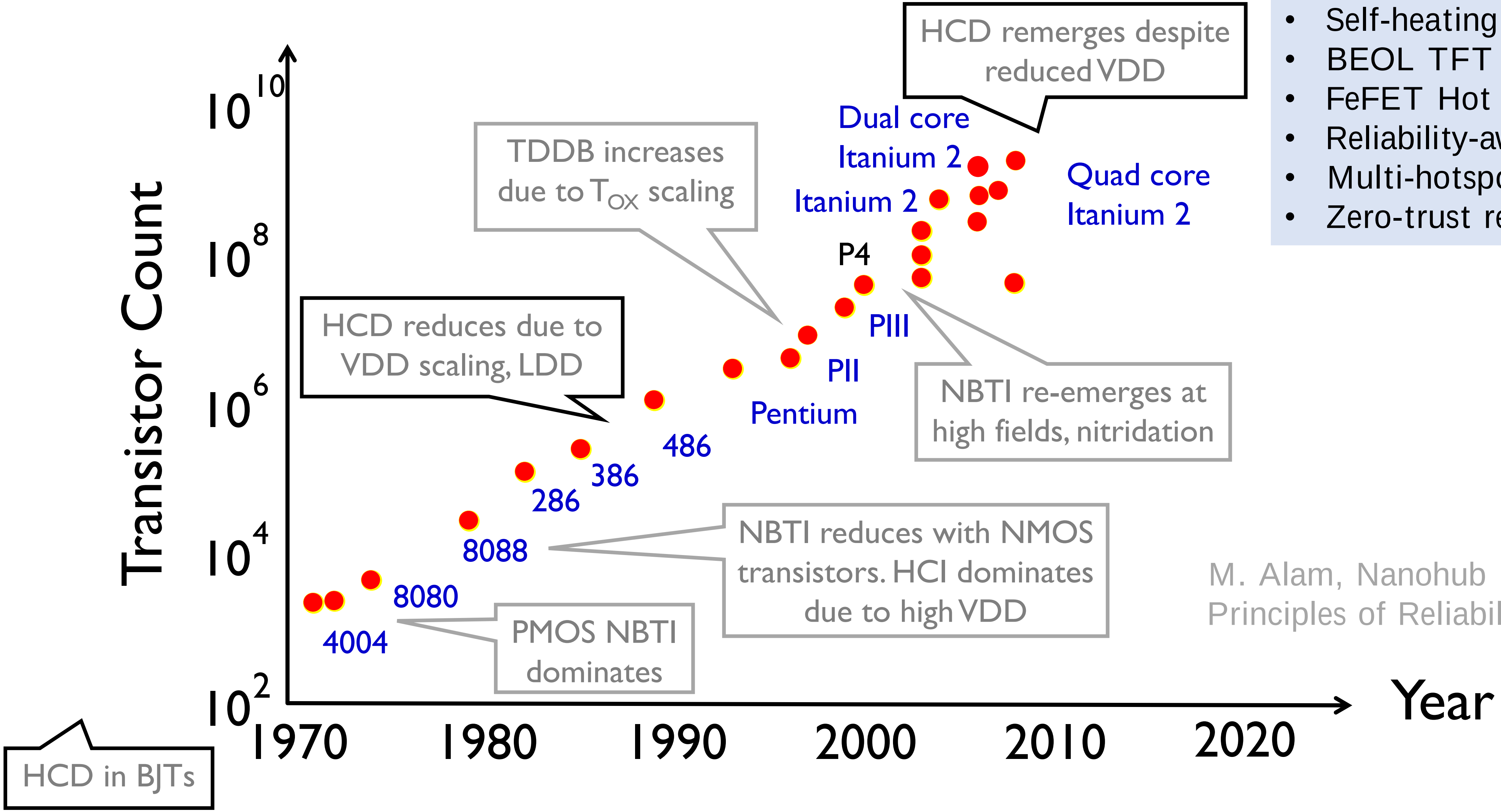
A short history of reliability physics ...



HCD in BJTs

PMOS NBTI dominates

NBTI reduces with NMOS transistors. HCI dominates due to high VDD

HCD reduces due to VDD scaling, LDD

TDDB increases due to T_{OX} scaling

NBTI re-emerges at high fields, nitridation

HCD remerges despite reduced VDD

- Self-heating
- BEOL TFT degradation
- FeFET Hot atom damage
- Reliability-aware SOA
- Multi-hotspot HCD
- Zero-trust reliability

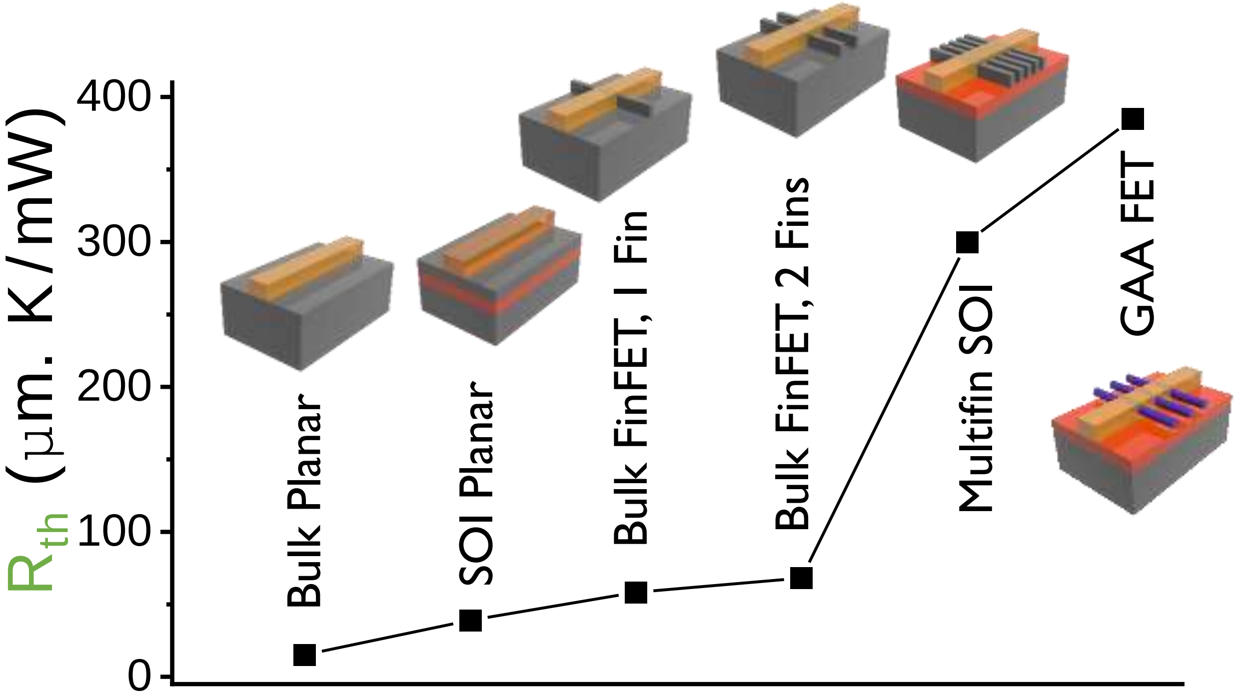
M. Alam, Nanohub Lecture Series
Principles of Reliability Physics

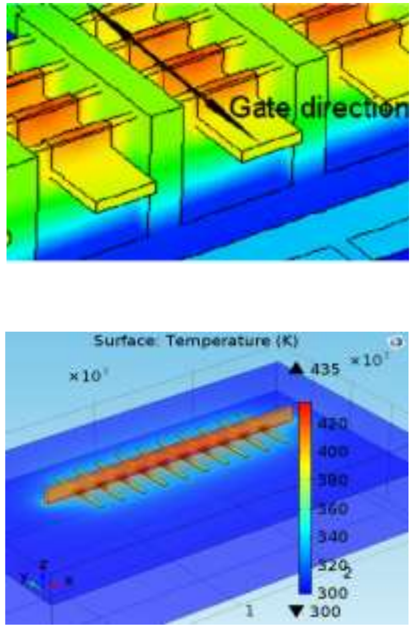
Self-heated transistors: an enduring challenge

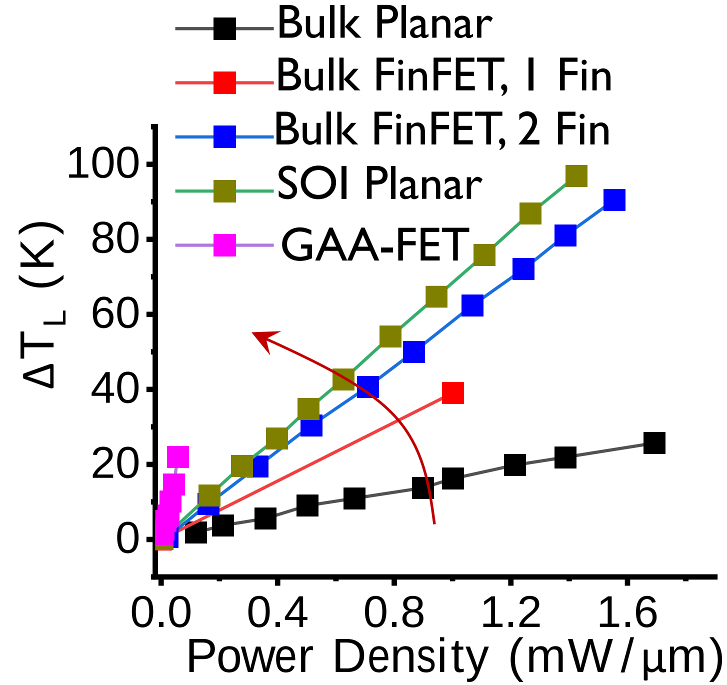
$$T_L = T_A + P\,R_{th}$$

Johnson-Keyes limit (1972)

$$T_L = T_A + P_0 \times \sqrt{A} \times (\beta/\kappa)$$

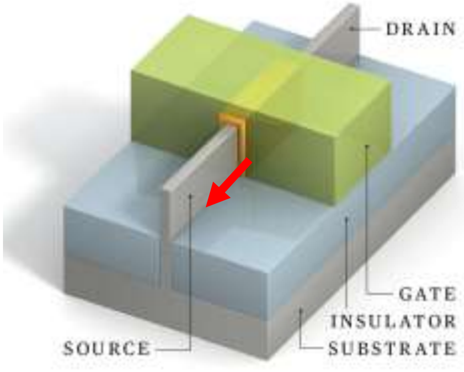






S. H. Shin, et. al., IEDM Tech. Dig., Dec. 2016, pp. 15.7.1–15.7.4.
M. A. Alam, et. al., IEEE TED, 66, 11, 2019.
M. Cho, et. al., in HCD in Semiconductor Devices, 2015, pp. 287–307

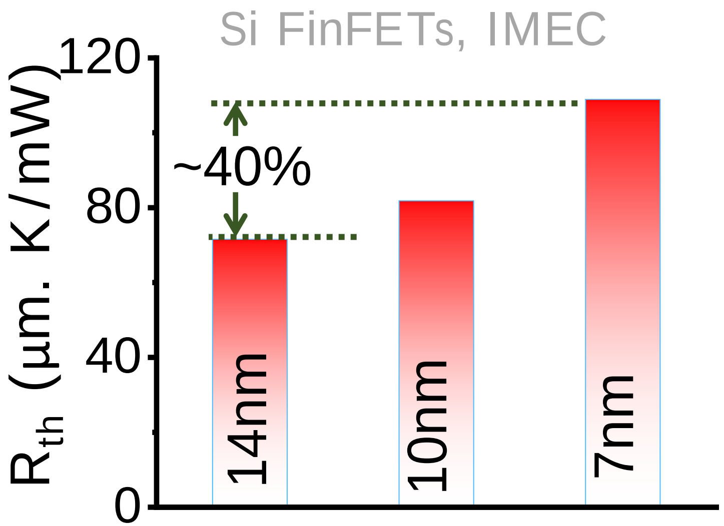
Self-Heating redefines FinFET HCD

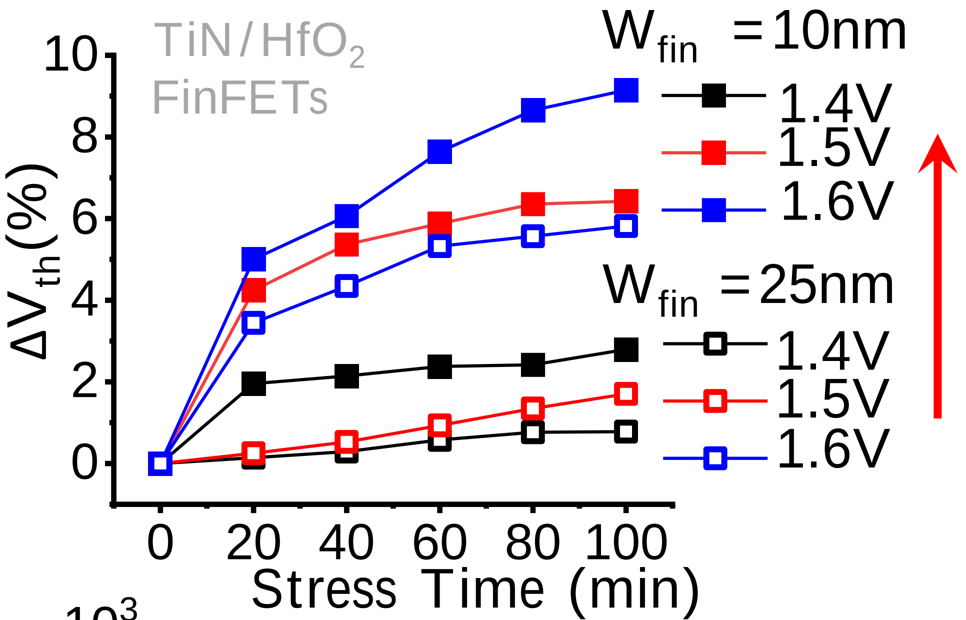


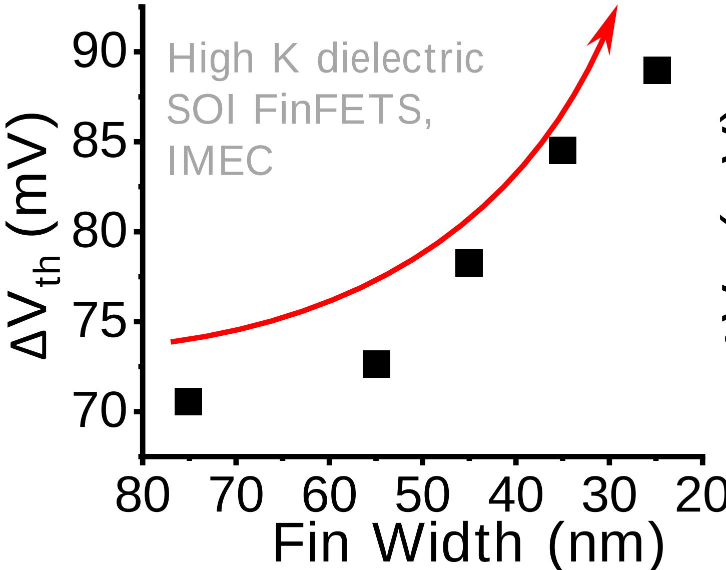
$$R_{th} \sim 1/W_{fin}$$

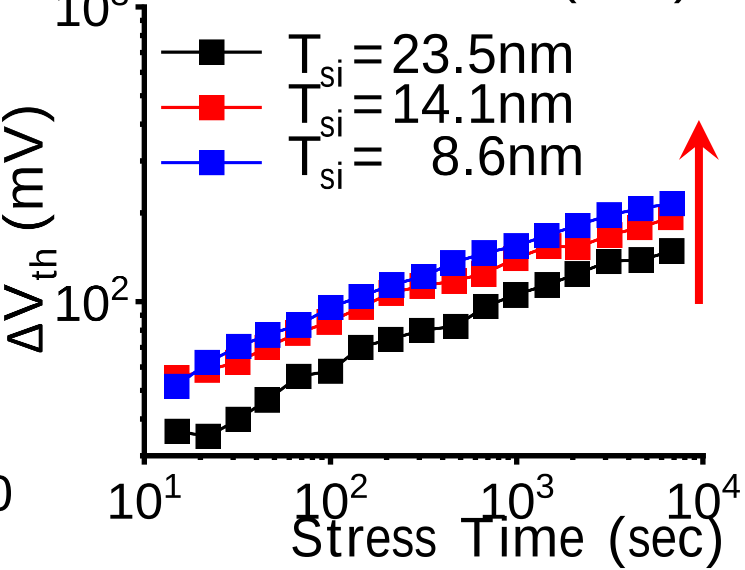
$$T_L = T_A + P\,R_{th}$$

$$R_B \sim e^{-\frac{E_B}{k_B T_L}}$$



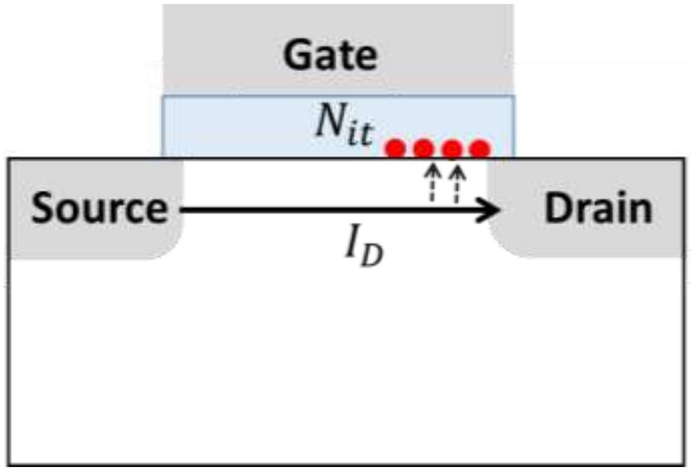


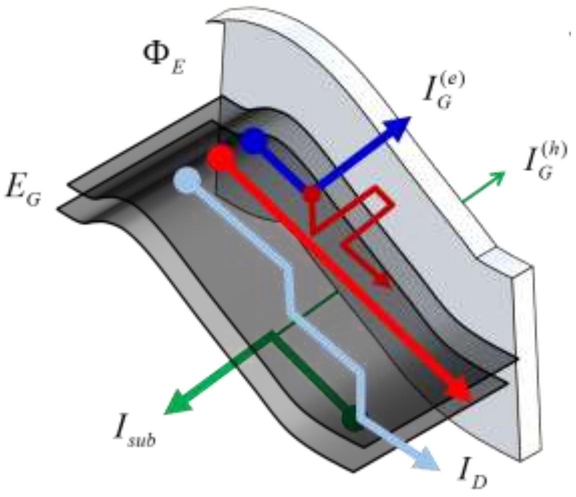




- D. Jang et al., IEDM Tech. Dig., 2015.
- W. T. Chang et al., IEEE TDMR, 15, 1, 2015.
- Chabukswar et. al., Microele. Eng.,87,10,2010
- S. H. Shin et al., IEDM Tech. Dig., 2015

HCD is a complex phenomenon …



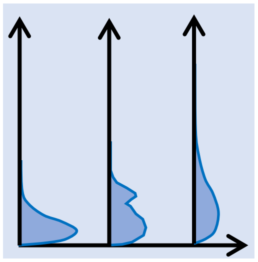


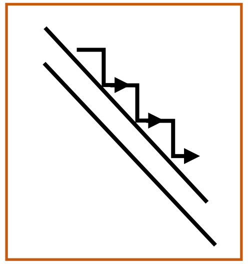
$$\frac{dN_{it}}{dt} = k_f(E_B, T_e, T_L)(N_0 - N_{it})$$

$$R_e \sim e^{-\frac{E}{kT_e}}$$

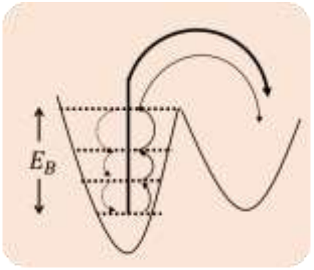
$$R_{II} \sim e^{+\frac{E_g}{k_B T_L}}$$

$$R_B \sim e^{-\frac{E_B}{k_B T_L}}$$



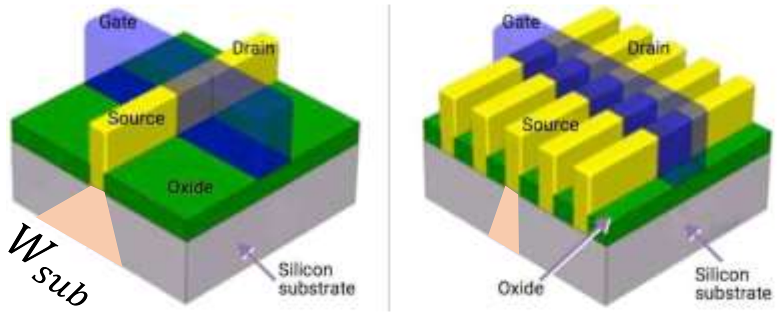


Historically …



Now…

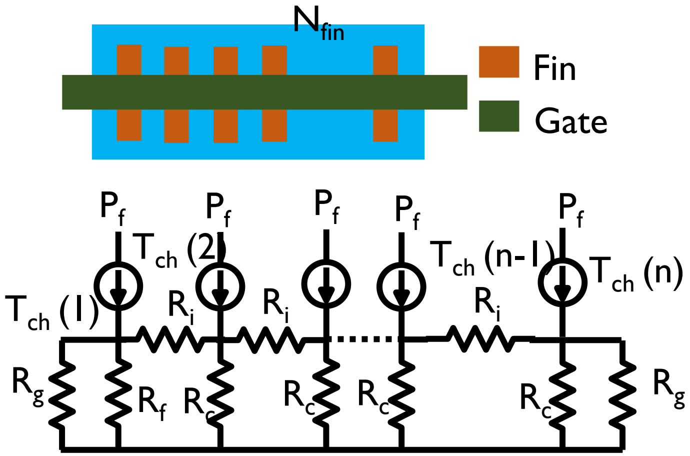
HCD increases with Fin-Number

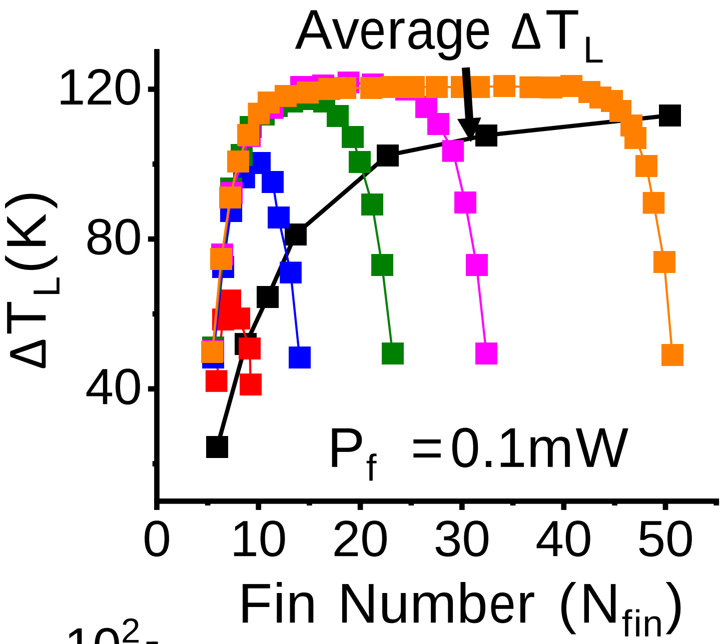


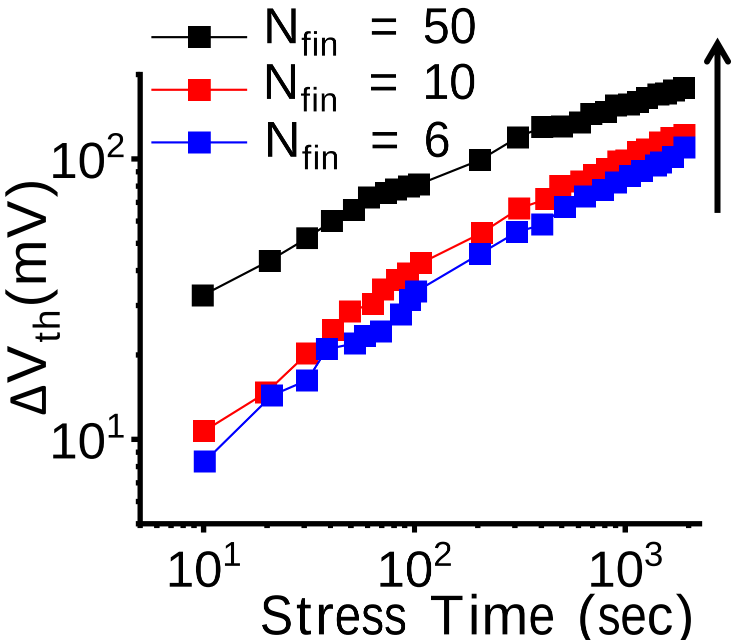
$$R_{th} \sim N_{fin} \sim W_{sub}^{-1}$$

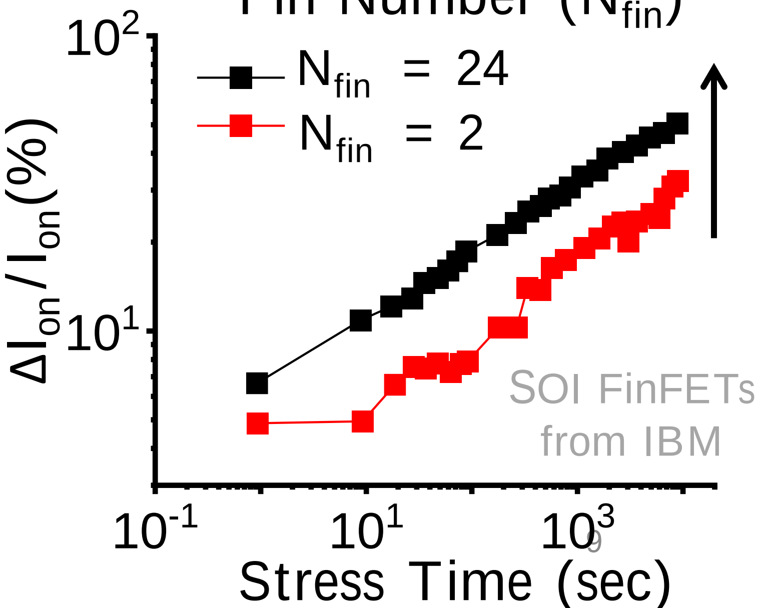
$$T_L = T_A + P\,R_{th}$$

$$R_B \sim e^{-\frac{E_B}{k_B T_L}}$$





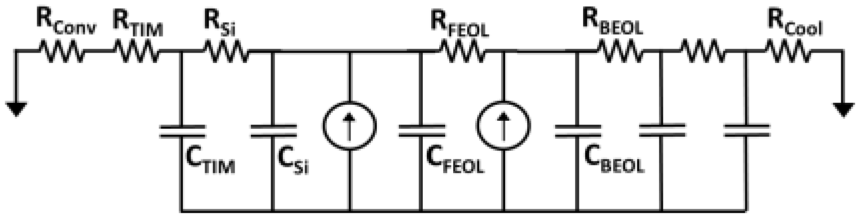




SOI FinFETs from IBM

- H. Jiang, et. al., Proc. IEEE IRPS, 2016.
- H. Jiang, et. al., IEEE EDL, 36, 12, 2016.
- A. Gupta, et. al., IEEE TED, 66, 5, 2019.

Packaging increases HCD further …

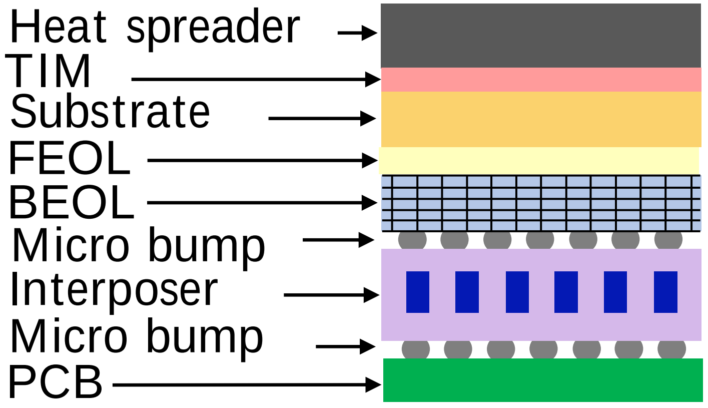


$$R_{th} \sim R_{FEOL} || R_{BEOL}$$

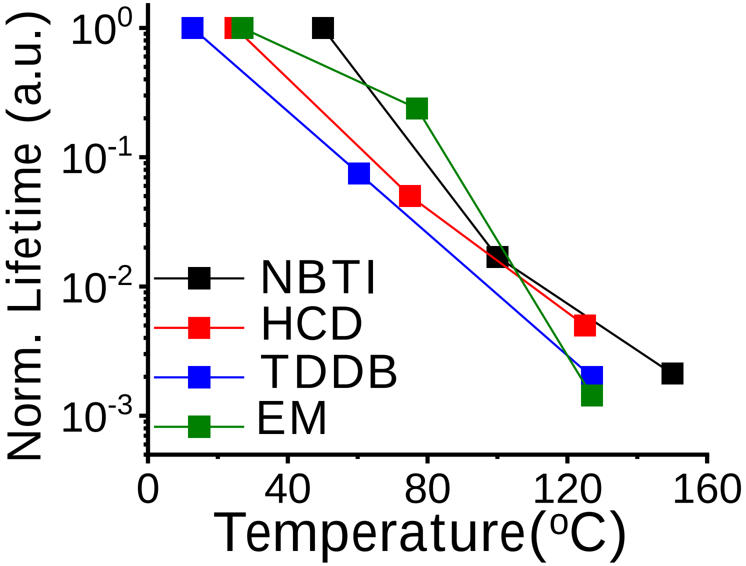
$$T_L = T_A + P\,R_{th}$$

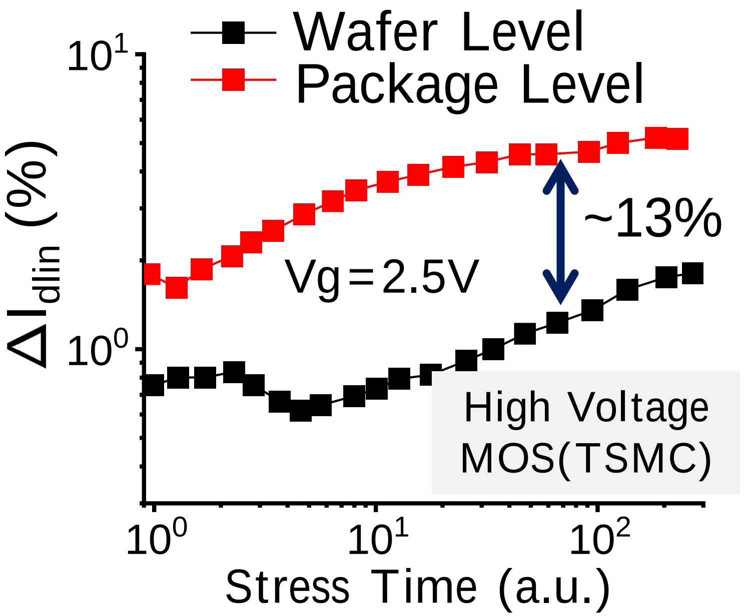
$$R_B \sim e^{-\frac{E_B}{k_B T_L}}$$

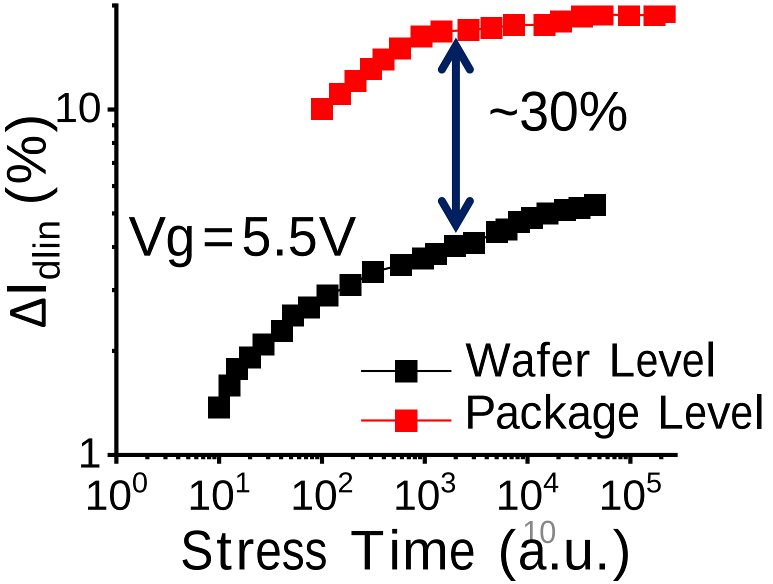
- W. Ahn, et. al., Microelectron. Rel., 81, 2018.
- H. J. Huang et. al., Symp. VLSI Digest, 2011.
- M. A. Alam, et. al., IEEE TED, 66, 11, 2019



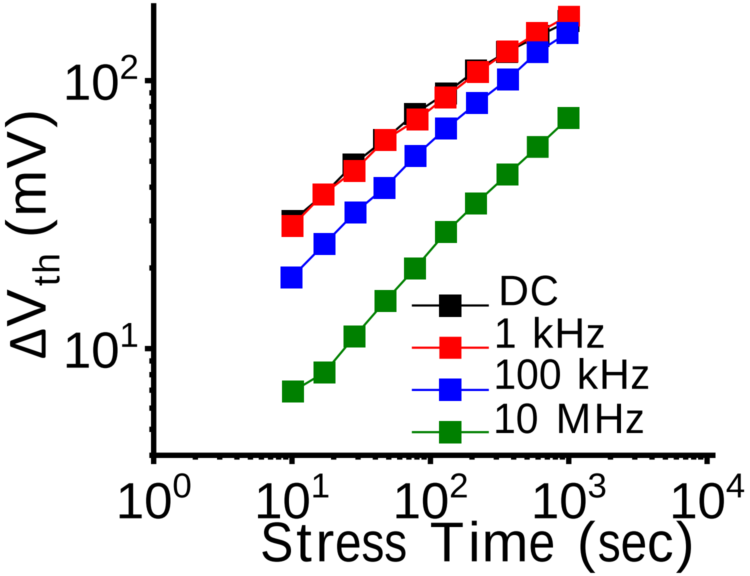
Heat spreader
TIM
Substrate
FEOL
BEOL
Micro bump
Interposer
Micro bump
PCB

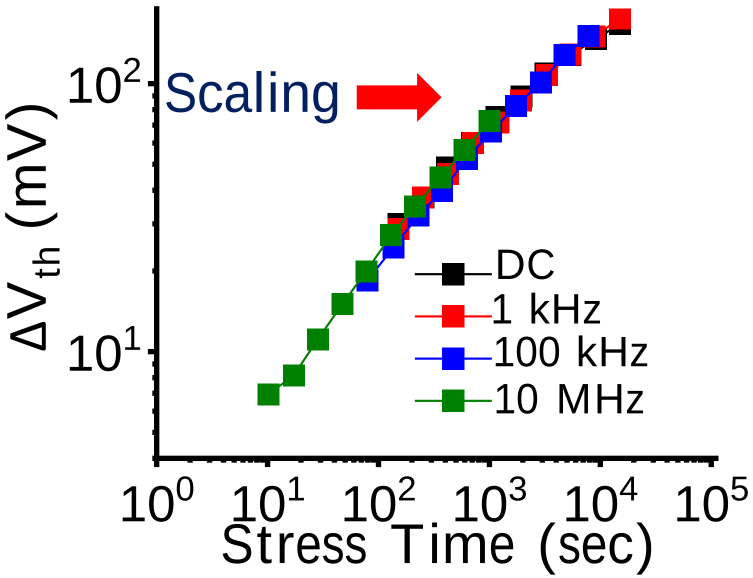




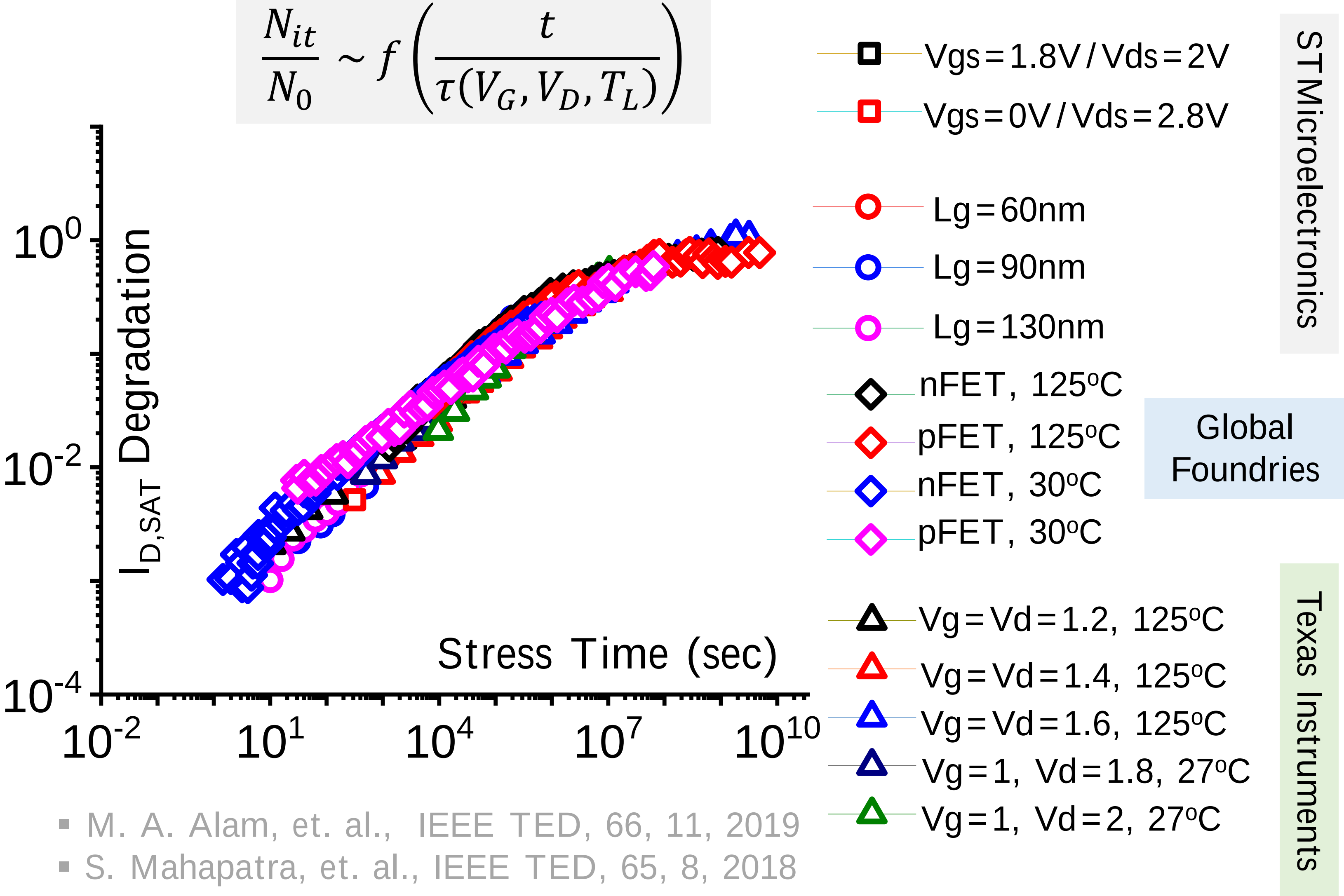


Regardless, HCD of logic FET is universal …





$$\frac{N_{it}}{N_0} \sim f\left(\frac{t}{\tau(V_G, V_D, T_L)}\right)$$



- M. A. Alam, et. al., IEEE TED, 66, 11, 2019
- S. Mahapatra, et. al., IEEE TED, 65, 8, 2018

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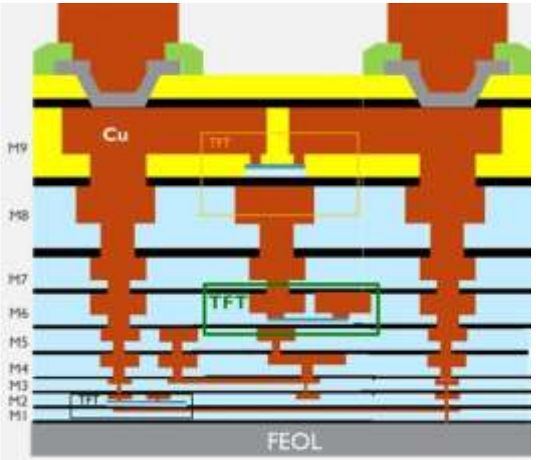
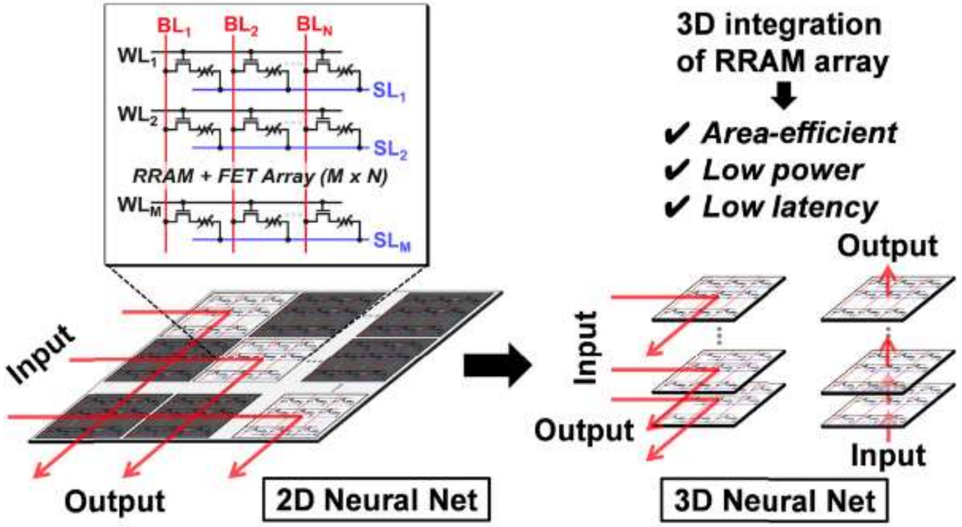
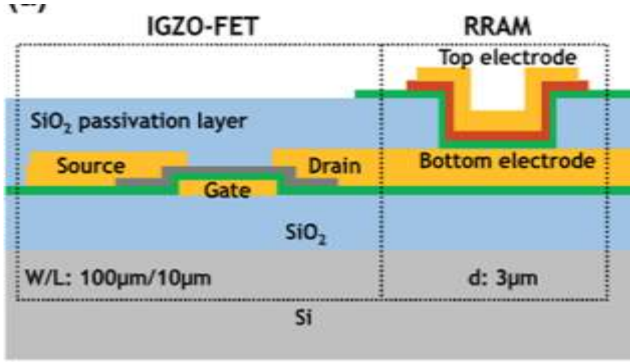
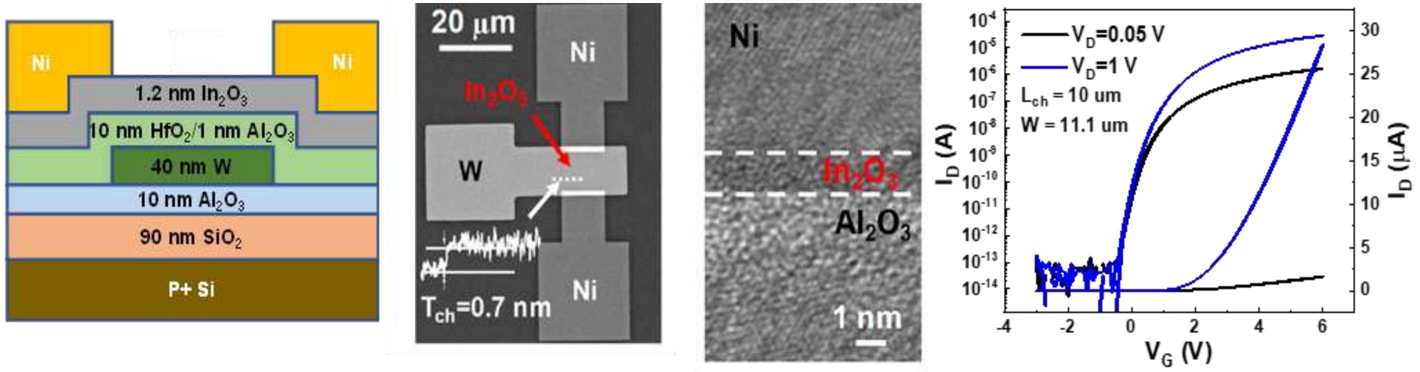
BEOL-integrated 3D transistor: The next frontier?



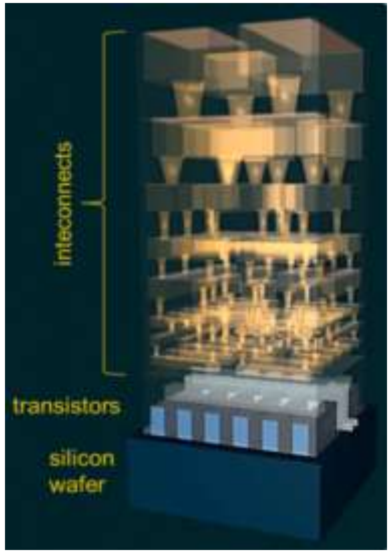


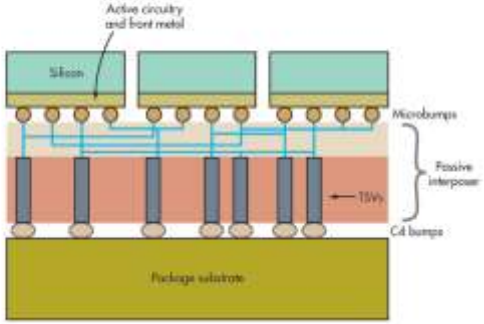


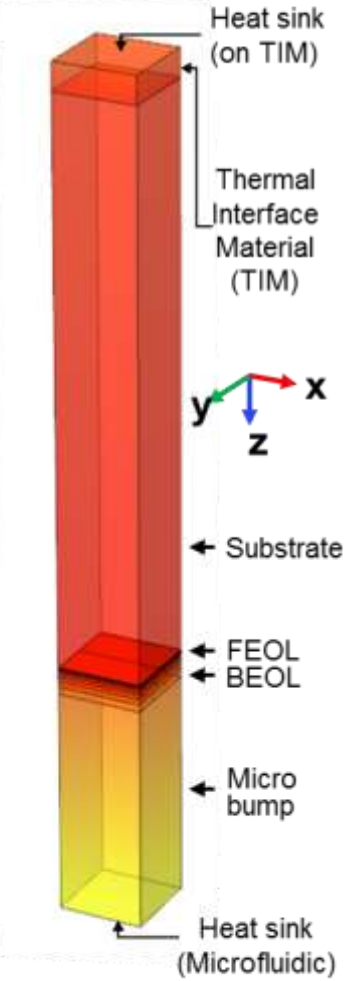
- Datta, S et al. (2019). BEOL compatible transistors for monolithic 3-D integration. IEEE Micro, 39(6), 8-15.
- Jiang, Junkai et al. (2019). Ultimate 3D Integration With 2D Materials: IEEE JED 10.1109/JEDS.2019.2925150.
- Wu, J. et al. (2020). A Monolithic 3-D Integration of RRAM Array and Oxide Semiconductor FET for In-Memory Computing in 3-D Neural Network. TED 67(12), 5322-5328.
- Lin, Zehao, et al. "High-Performance In_2O_3-Based 1T1R FET for BEOL Memory Application." IEEE TED (2021).



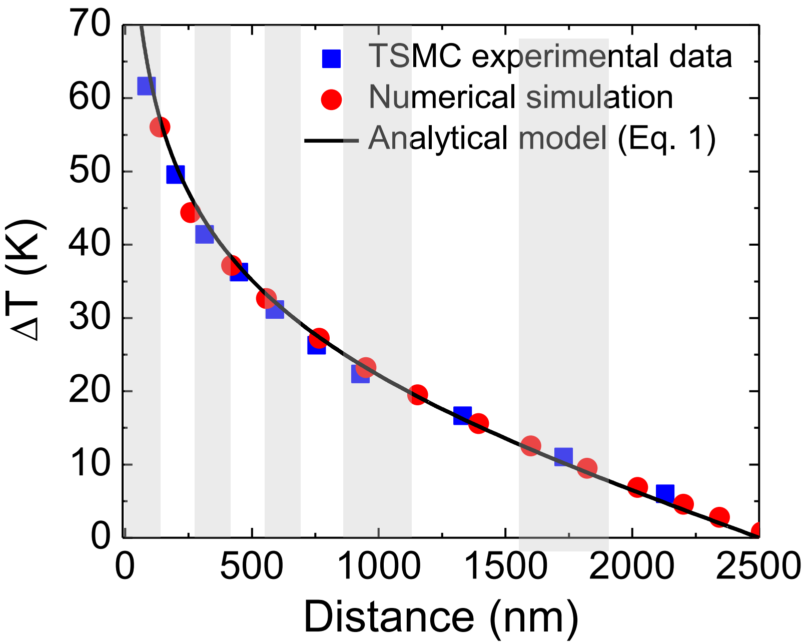
BEOL increases temperature further…





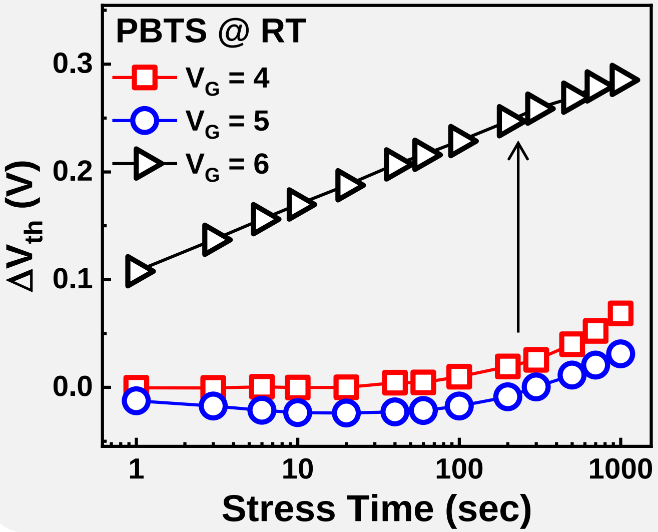


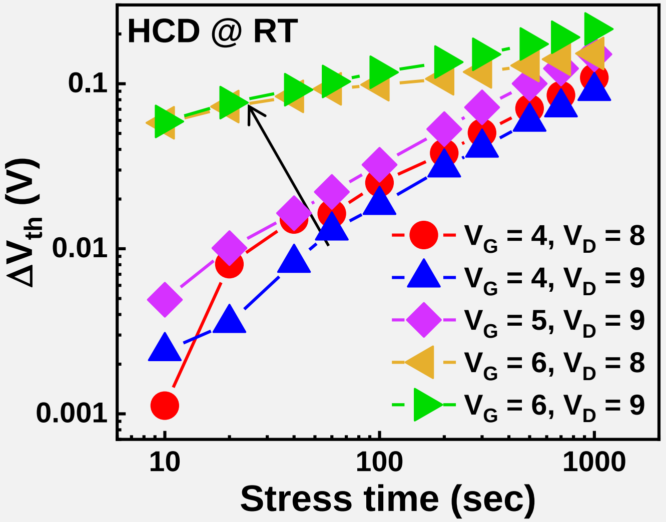
W. Ahn, Ph.D. Thesis, 2019.

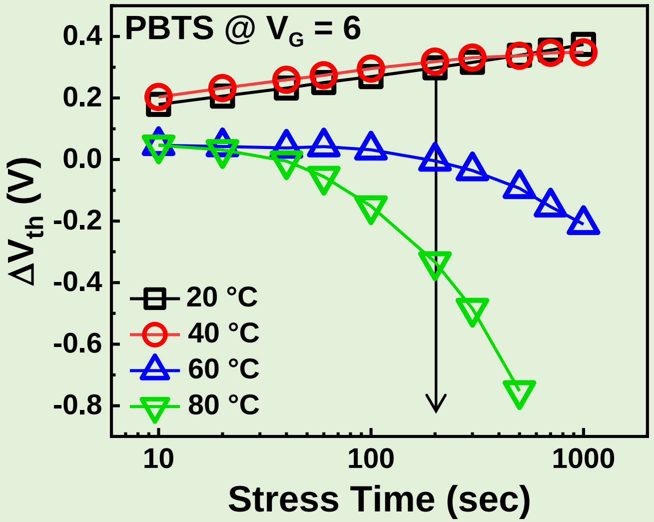


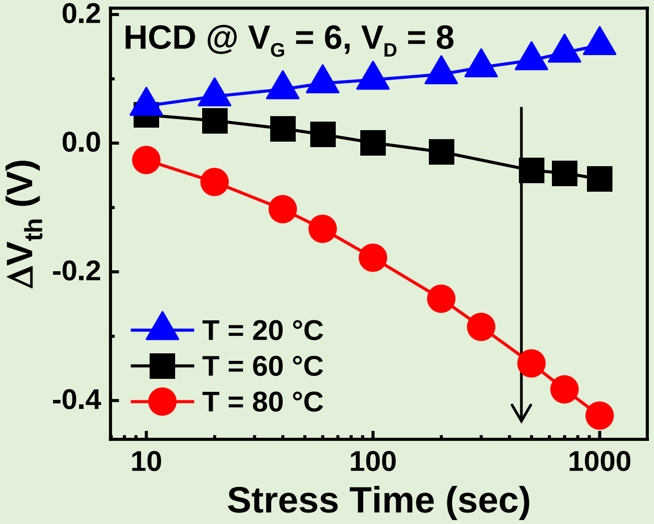
$$T(z) = \frac{P_l}{2\pi\,\boldsymbol{\kappa_{eff}}}\ln\left(\frac{z}{2h_0 - z}\right)$$

PBTI vs. HCD: Extreme Temperature Sensitivity

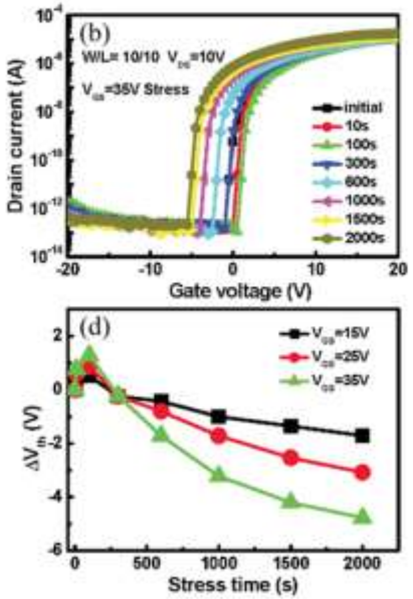




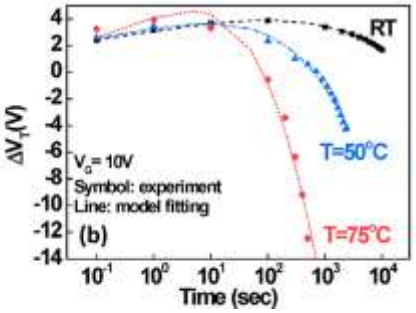




… well known in TFT literature

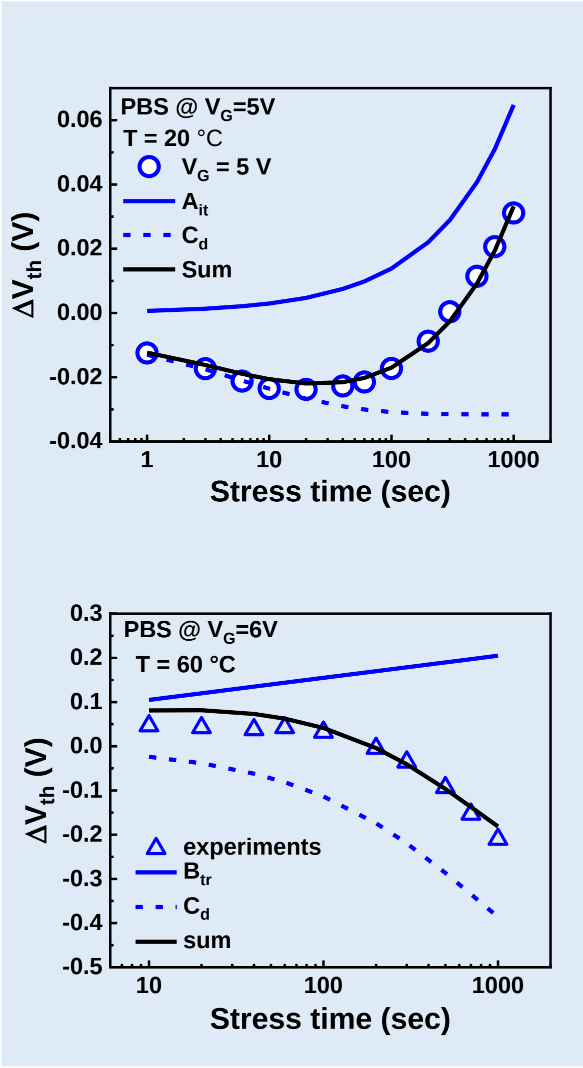


Chen et al. TED, 2019



Chan et al. APL, 2016

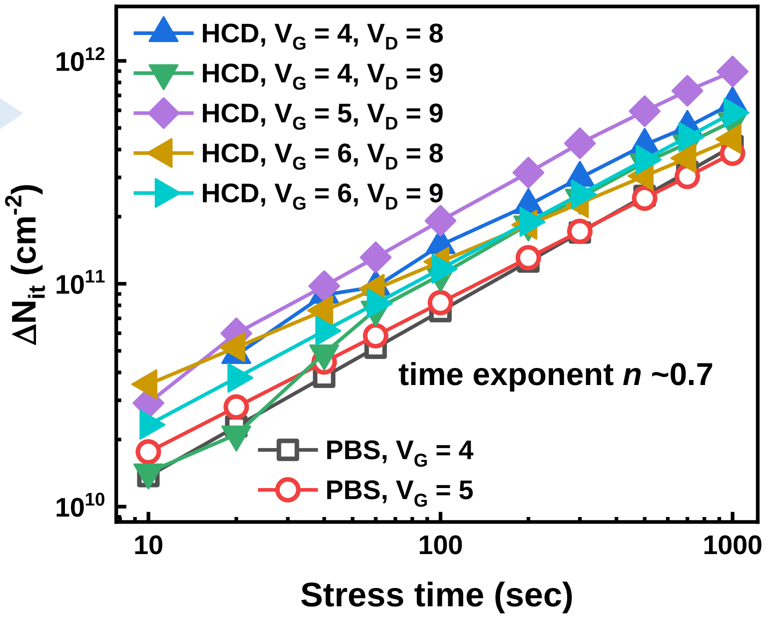
Underlying degradation is actually universal!

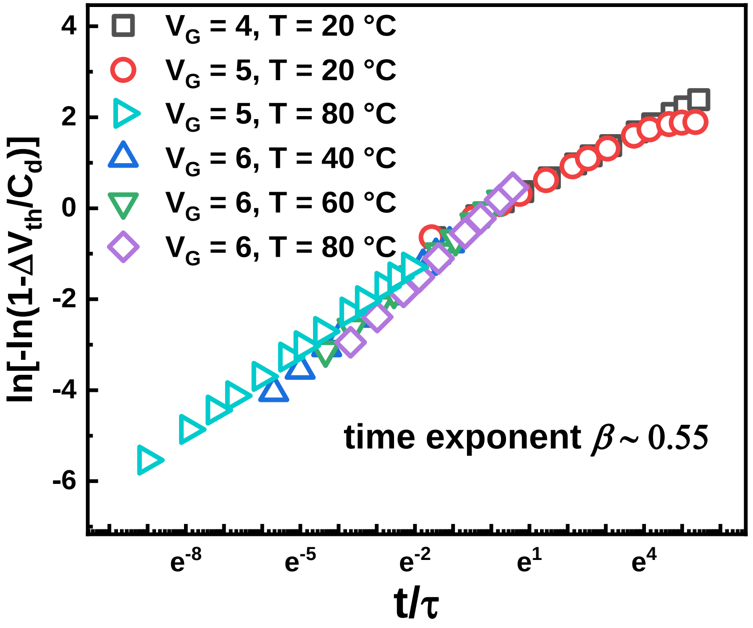


$$\Delta V_{th}(t) = A_{it}\, t^{n} + B_{tr}\, log\left(\frac{t}{\tau_{\mathrm{tr}}}\right) - C_d\left(1 - e^{-\left(\frac{t}{\tau_d}\right)^{\beta}}\right)$$

Interface
Trap-generation

Hydrogen-assisted
Donor trap formation





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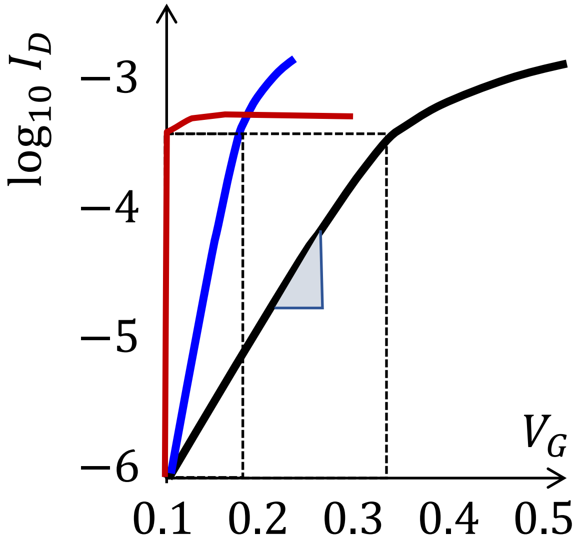
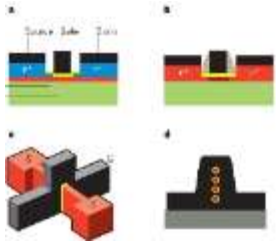
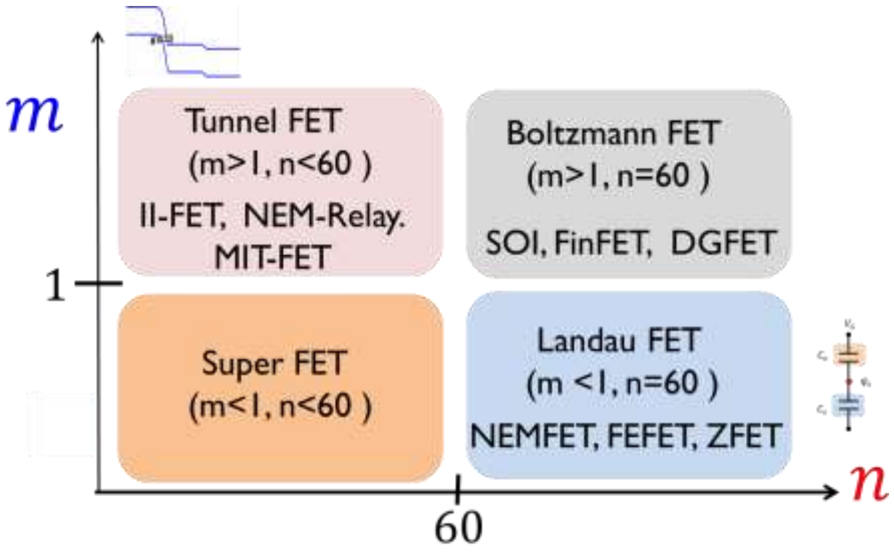
Power Solution: Landau switches



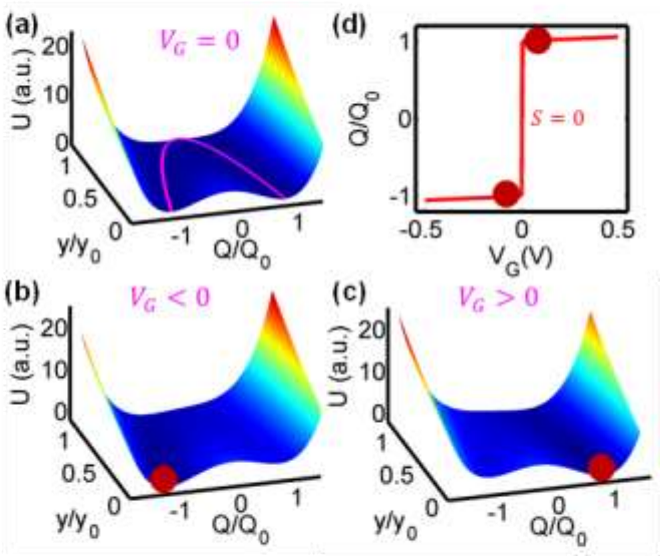
$$\Delta T \equiv T - T_a = P \times R_{th}$$



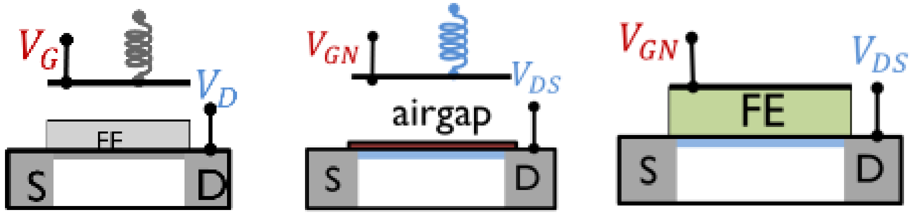
$$S \equiv \left[\left(\frac{d\psi_s}{dV_G} \right) \left(\frac{d \log_{10}(I_{DS})}{d\psi_s} \right) \right]^{-1} = m \times n$$



m	**Tunnel FET** (m>1, n<60) II-FET, NEM-Relay. MIT-FET	**Boltzmann FET** (m>1, n=60) SOI, FinFET, DGFET
1	**Super FET** (m<1, n<60)	**Landau FET** (m<1, n=60) NEMFET, FEFET, ZFET
		60 n



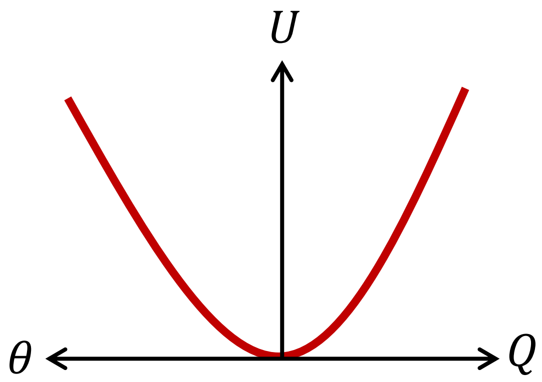
A. Jain, APL, 2014

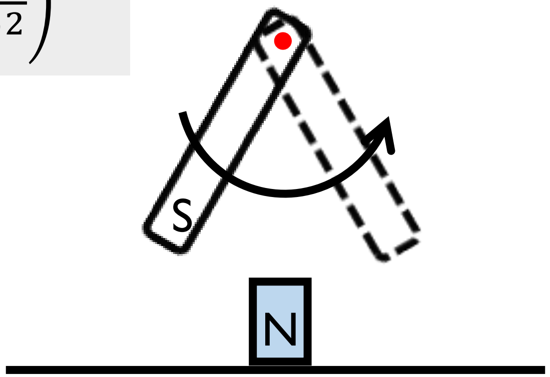


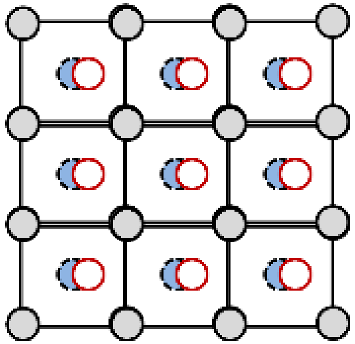
Positive and Negative Capacitors

$U = Q^2/(2C_o)$

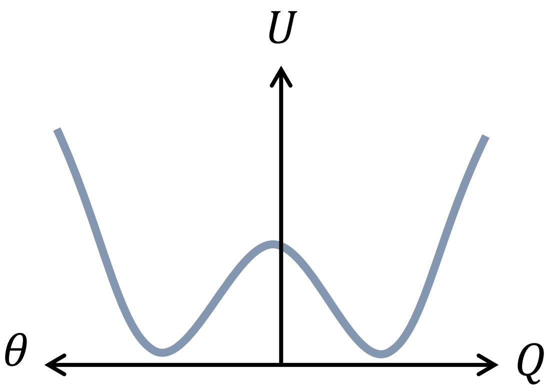
$$C \equiv \left(\frac{d^2U}{dQ^2}\right)^{-1}$$

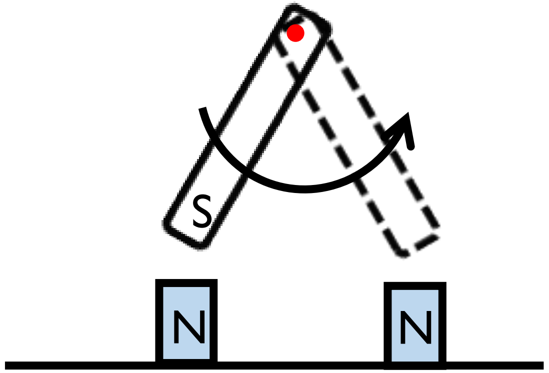


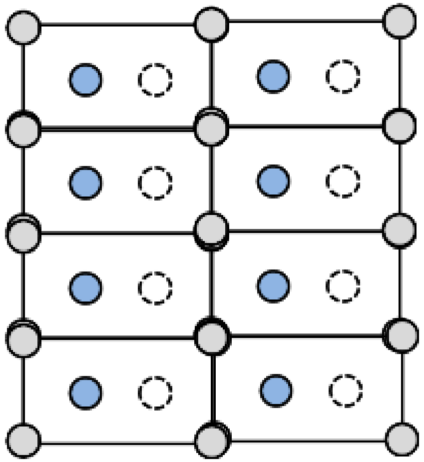




$U = -(\alpha Q^2/2) + (\beta' Q^4/4)$

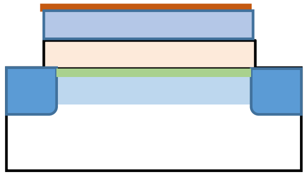


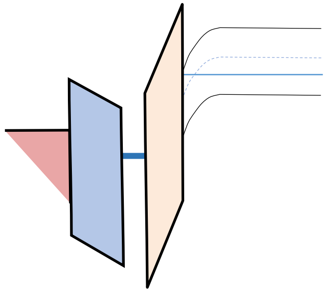


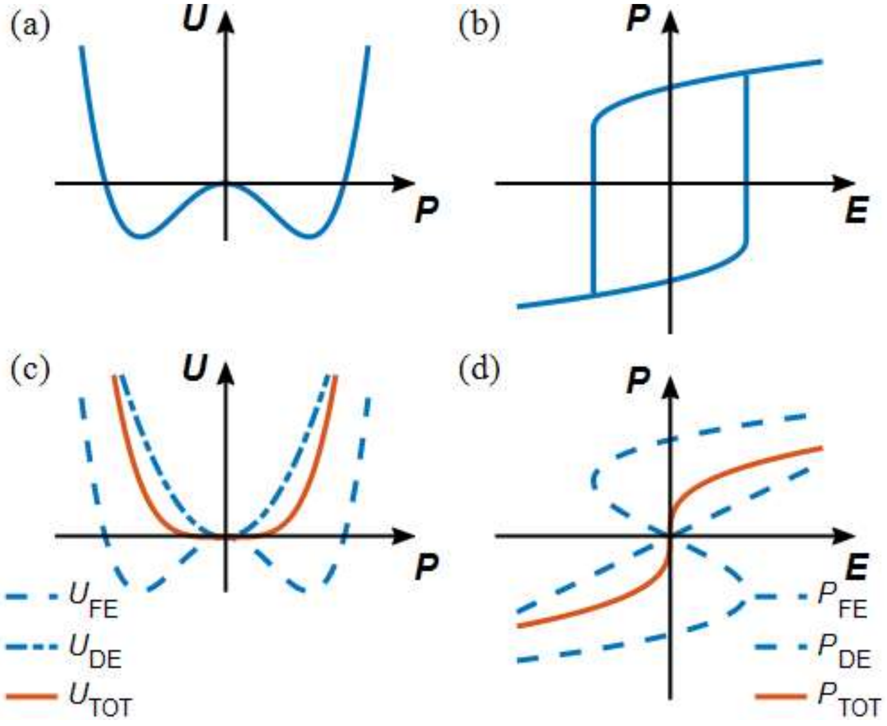


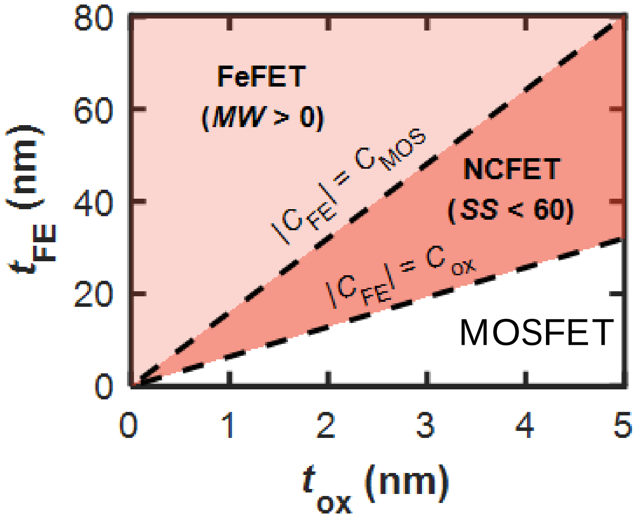
Alam, A Tutorial on Landau Transistors, 2015

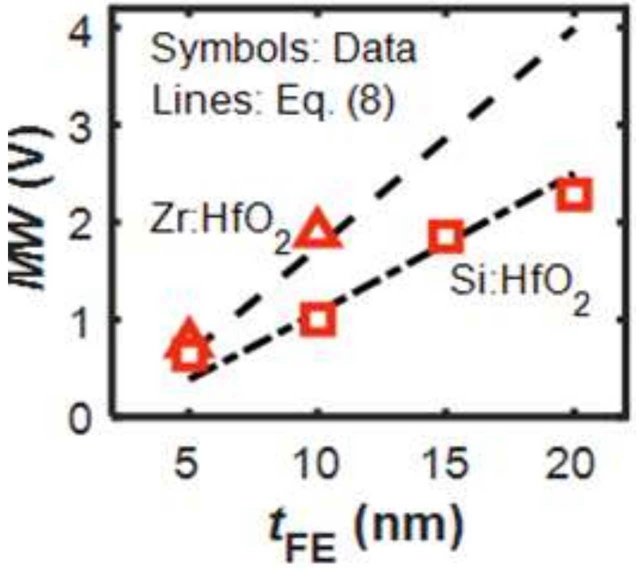
Reliability of FeFET and NCFET: Landau model





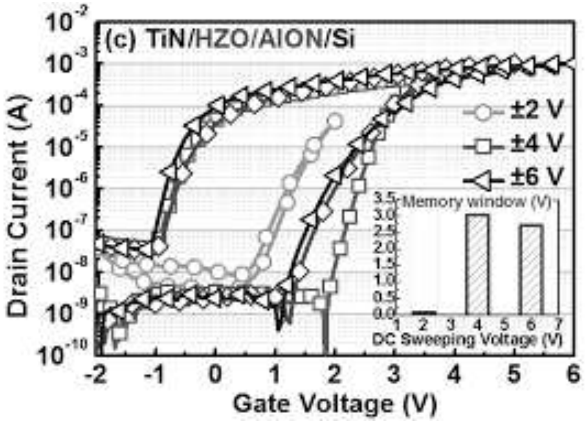


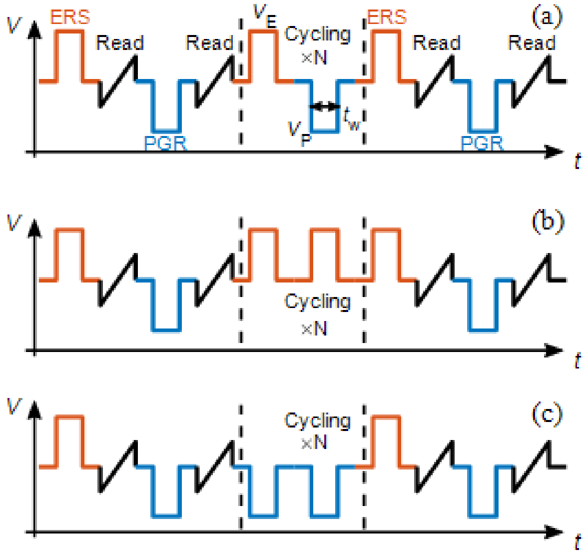


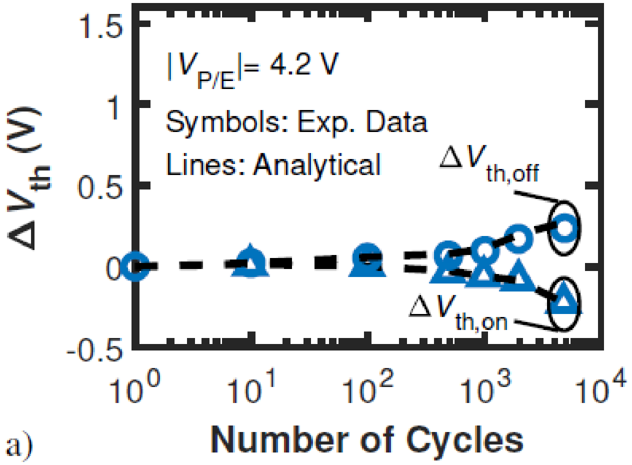


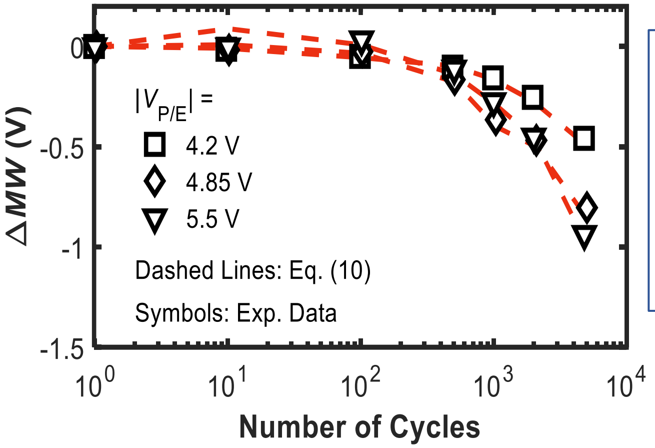
K. Karda et al., TED, 2019. N. Zagni, APL, 2020.
Reliability Physics of Ferroelectric/Negative Capacitance Transistors for Memory/Logic Applications: An Integrated Perspective, JMR, 2021.
A tutorial Introduction to NCFET: https://nanohub.org/resources/23157

Endurance of FETFET .. Si/SiO2 defects







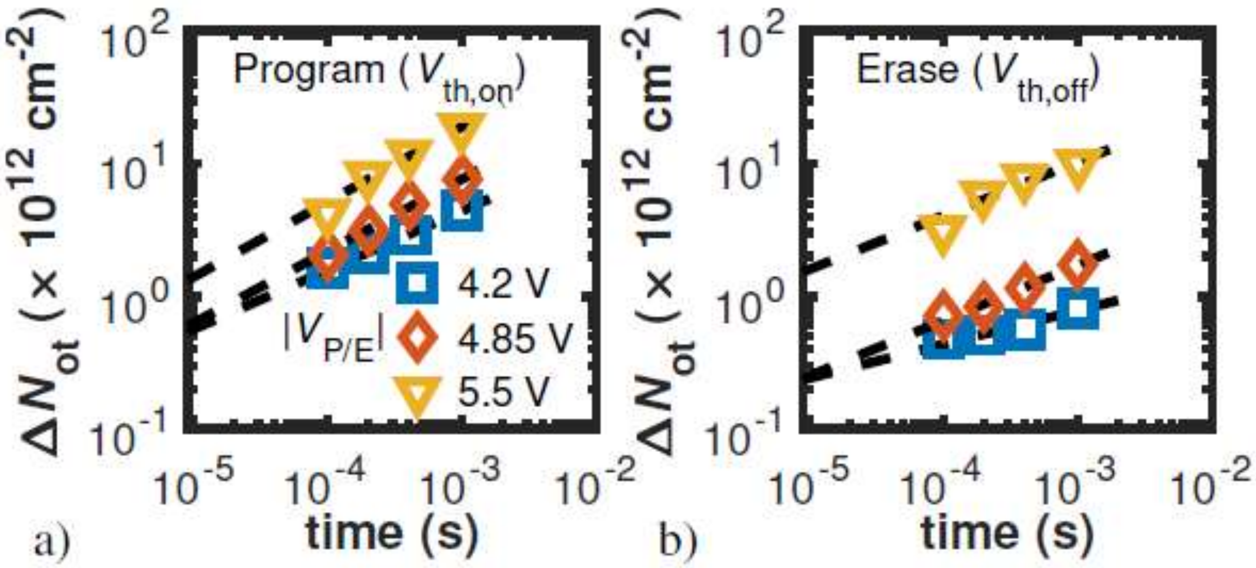


$$V_{th,on} = V_{FB} + 2V_t \ln\left(\frac{2V_t}{|a|Q_0}\right) - 2V_t$$

$$V_{th,off} = V_{FB} + 2V_t \ln\left(\frac{Q_{sw}}{Q_0}\right) - V_{sw}$$

$$MW = 2V_t \ln\left(\frac{2V_t}{|a|Q_{sw}}\right) + (V_{sw} - 2V_t)$$

Zagni, Nicolò et al. APL 117.15 (2020): 152901.

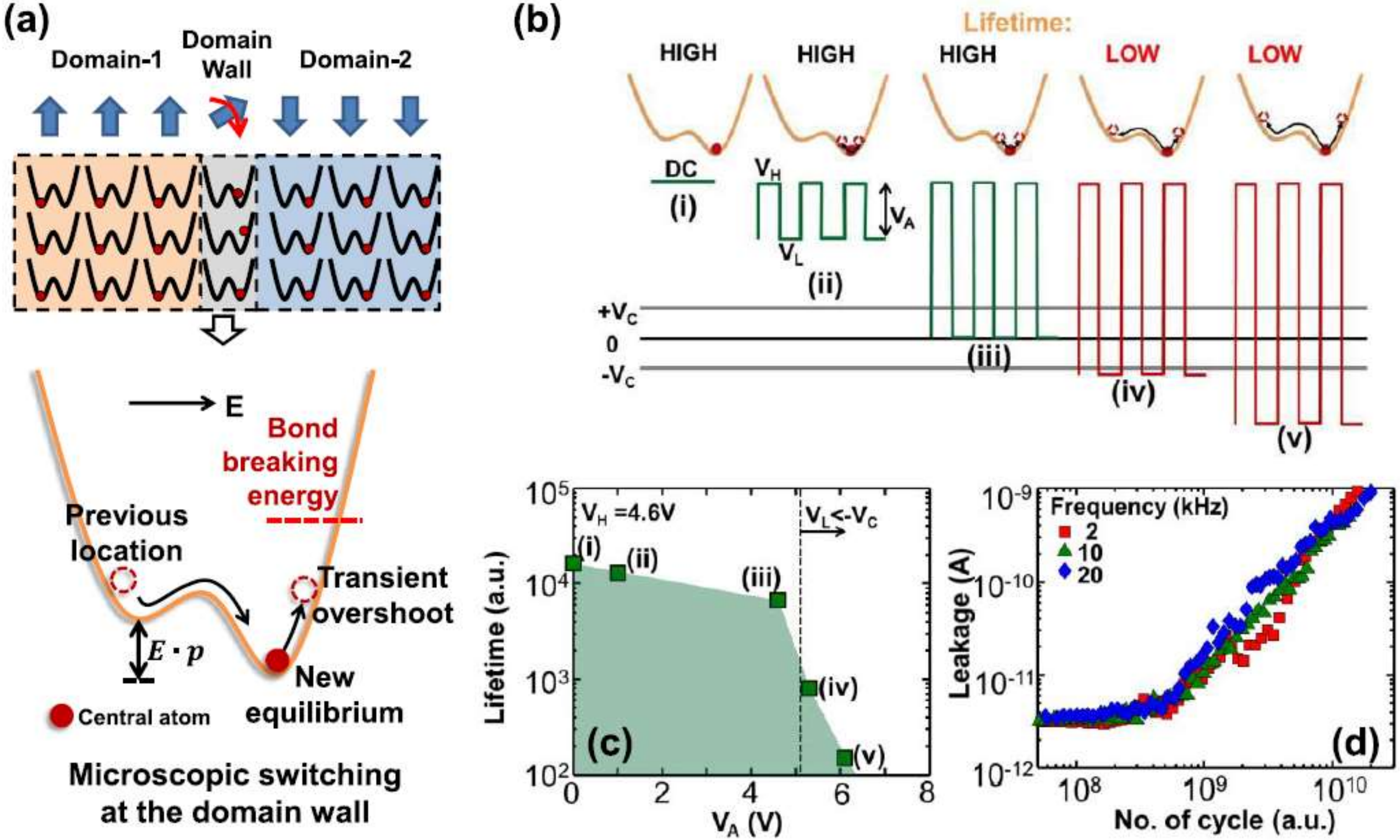


$$\Delta V_{th,on} = 2V_t \ln\left(1 + \frac{q\Delta D_{it,P}}{C_{ox}}\right) \times \left(1 + \frac{q\Delta D_{it,P}}{C_{ox}}\right) - \frac{q}{C_{ox}} \times \left\{\Delta N_{ot,P} - \Delta D_{it,P}\left[2V_t \ln\left(\frac{2V_t}{|a|Q_0}\right) - 2V_t - \phi_b\right]\right\} \tag{8a}$$

$$\Delta V_{th,off} = -\frac{q}{C_{ox}}\left\{\Delta N_{ot,E} - \Delta D_{it,E}\left[2V_t \ln\left(\frac{Q_{sw}}{Q_0}\right) - \phi_b\right]\right\} \tag{8b}$$

$$\Delta MW = 2V_t \ln\left(1 + \frac{q\Delta D_{it,P}}{C_{ox}}\right) \times \left(1 + \frac{q\Delta D_{it,P}}{C_{ox}}\right) - \frac{q}{C_{ox}}\left\{(\Delta N_{ot,P} - \Delta N_{ot,E}) - 2V_t \Delta D_{it,P}\left[\ln\left(\frac{2V_t}{|a|Q_0}\right) - 1\right] + 2V_t \Delta D_{it,E} \ln\left(\frac{Q_{sw}}{Q_0}\right) + (\Delta D_{it,P} - \Delta D_{it,E})\phi_b\right\}.$$

Hot atom damage in FeFET



M. Masduzzaman, TED, 2021.

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- Looking ahead

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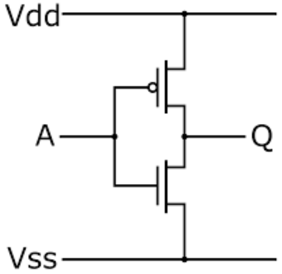
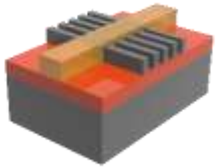
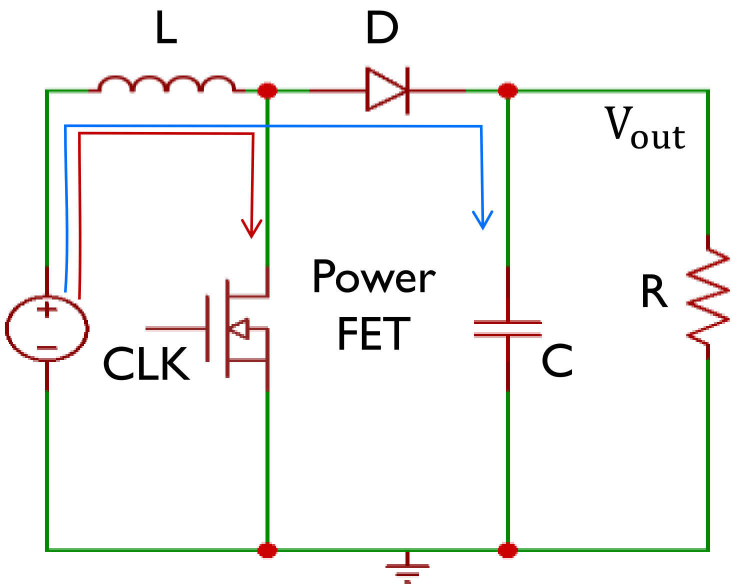
Inverting logic vs. Power Transistors

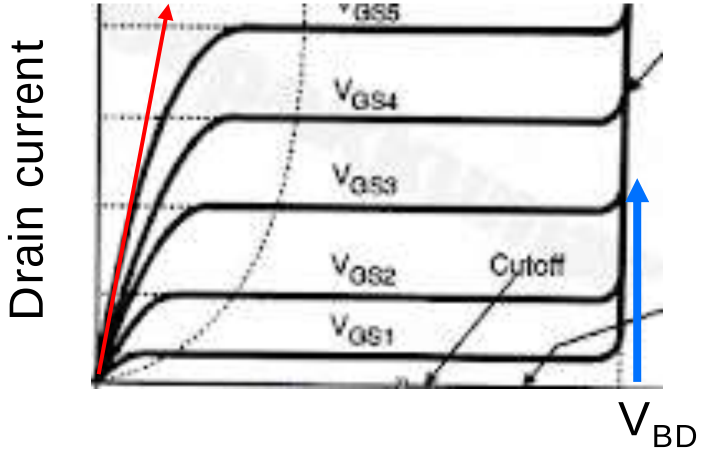
Logic



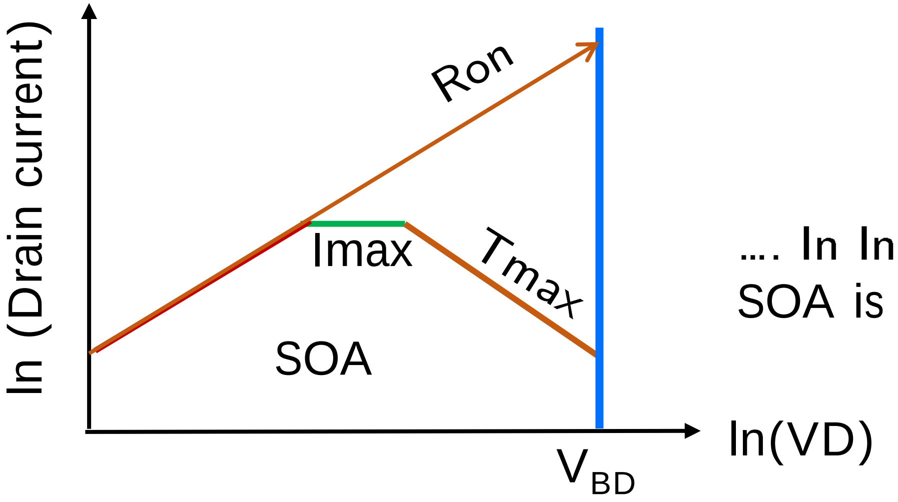


Power transistors



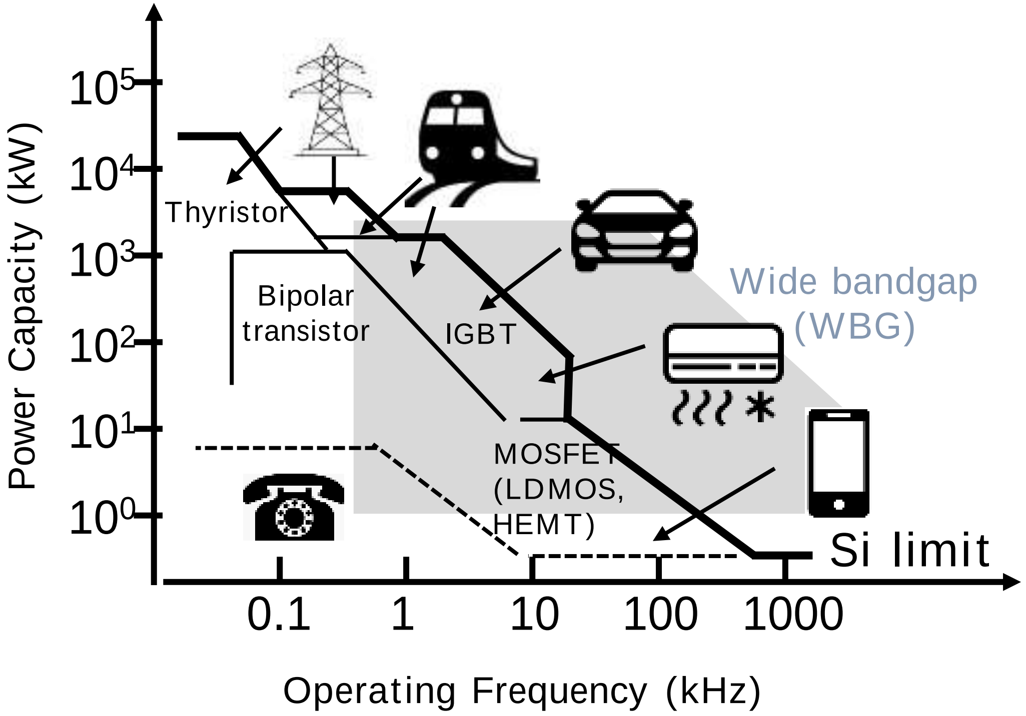


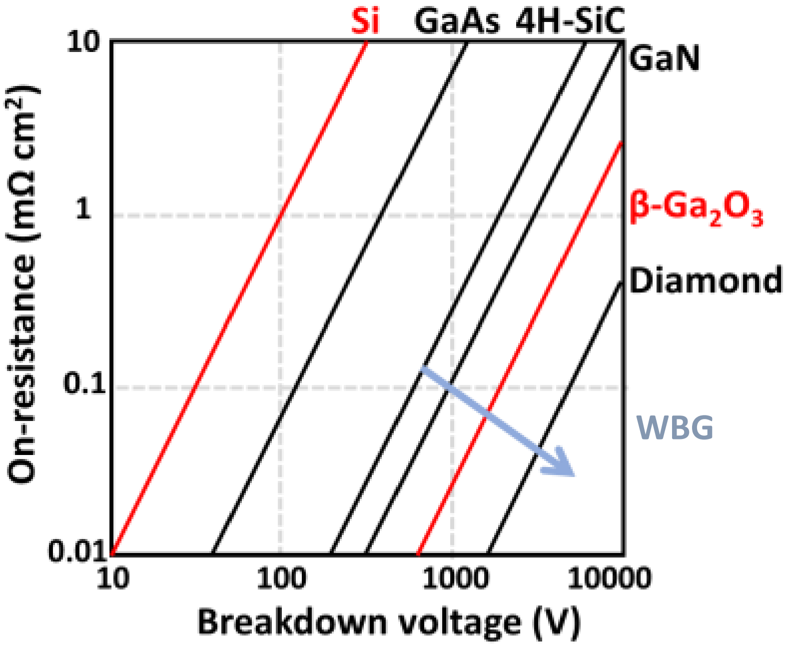
$$\frac{4V_{BD}^2}{R_{on}} = E_c^3\,\kappa\epsilon_0\mu$$



…. In Industry,
SOA is important

WBG electronics: Discovery of Ga2O3 …



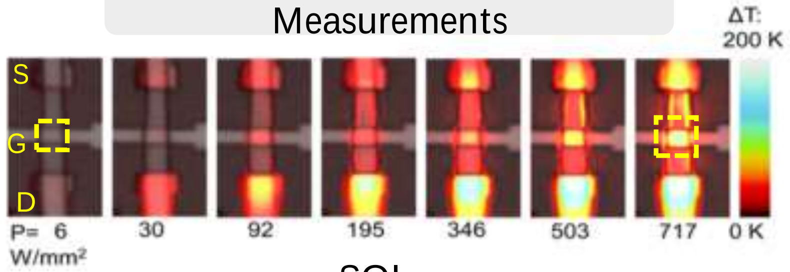


$$\frac{4V_{BD}^2}{R_{on}} = E_c^3\, \kappa \epsilon_0 \mu$$

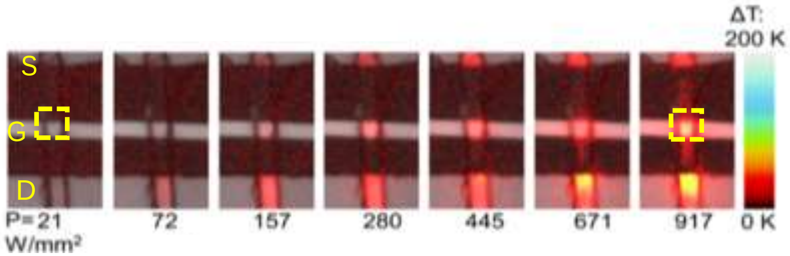
Material Parameters	Si	4H-SiC	GaN	β-Ga_2O_3	Diamond
Bandgap, Eg (eV)	1.1	3.25	3.4	4.85	5.5
Breakdown, Ec (MV/cm)	0.3	2.5	3.3	8	10

TCAD Model … thermal response

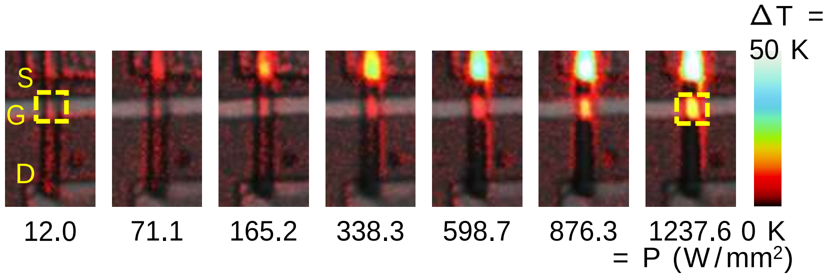
Thermoreflectance Measurements



SOI



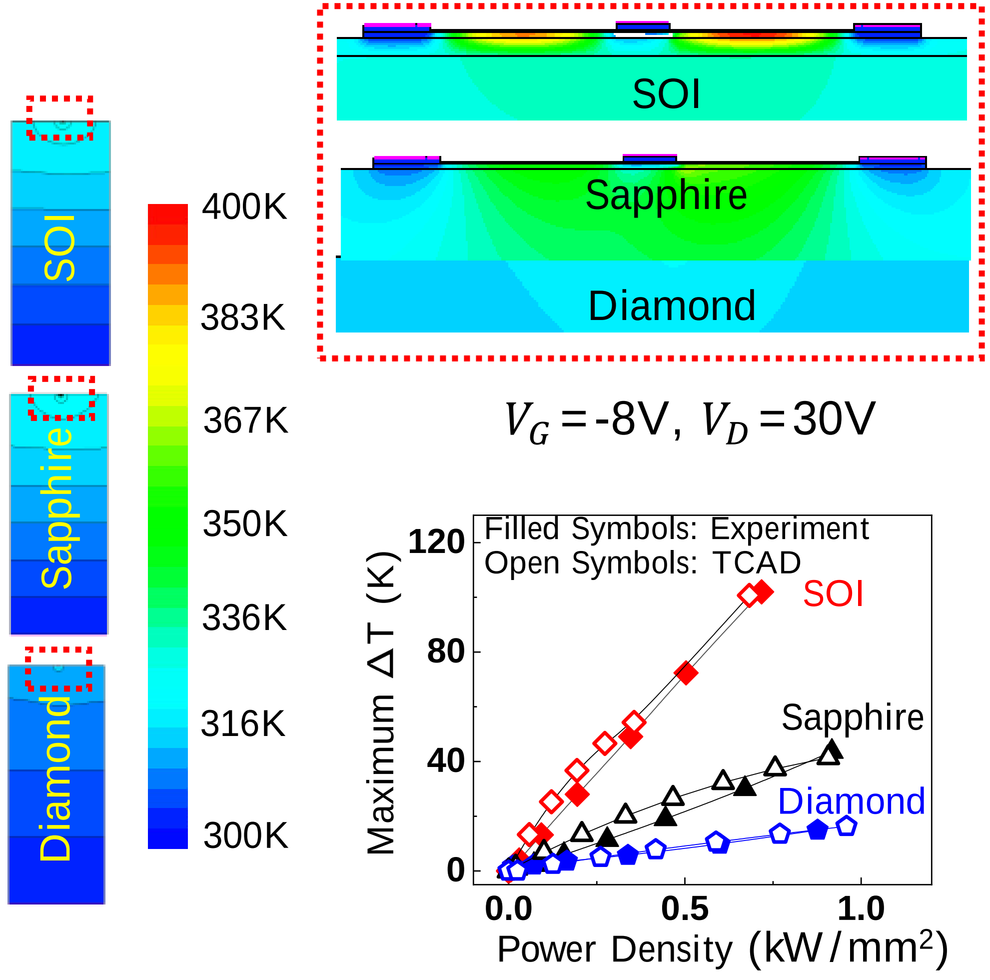
Sapphire



Diamond

Noh, JEDS 2019 Zhou, ACS Omega 2017

Mahajan et al. "Electrothermal performance limit of β-Ga2O3 field-effect transistors." APL, 115.17 (2019): 173508.

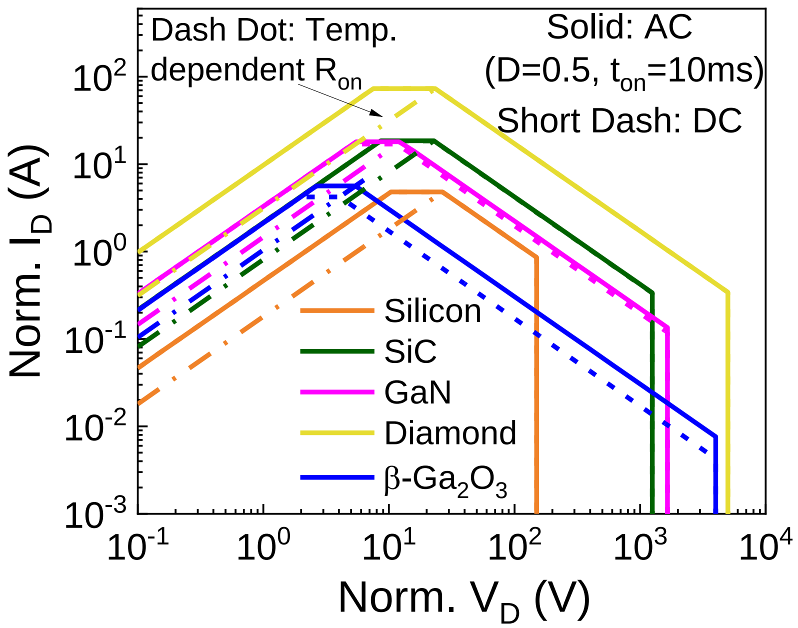


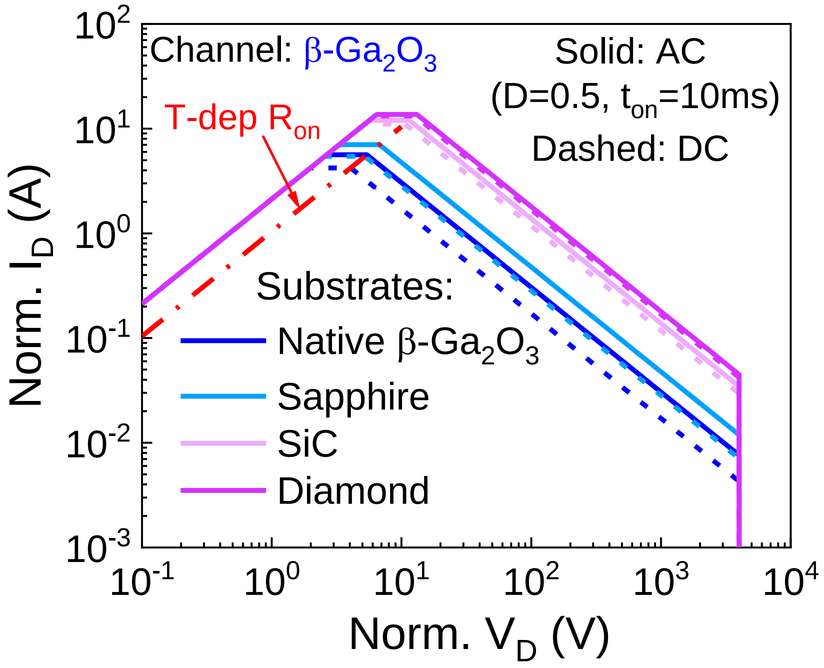
A new SHE/reliability aware Power FOM ..

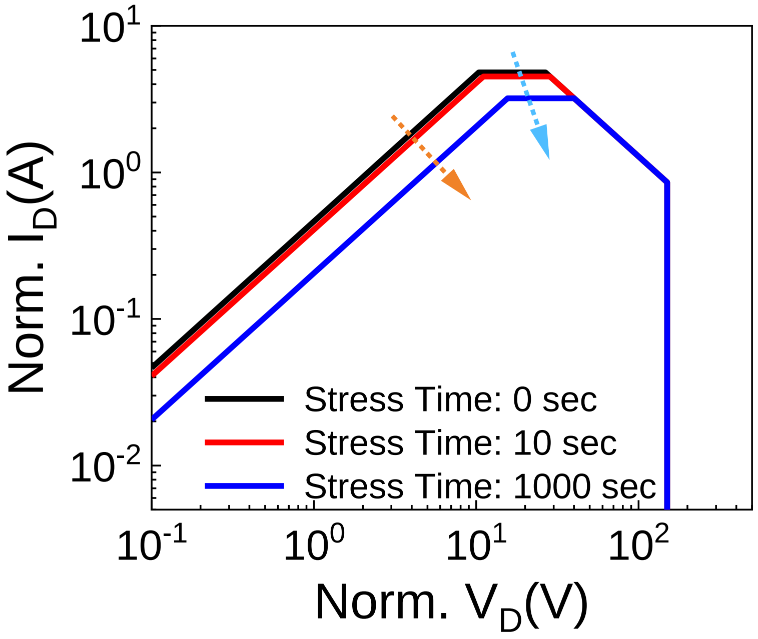
$$\frac{4V_{BD}^2}{R_{on}} = E_c^3\,\kappa\epsilon_0\mu$$

$$R_{on}(T_{on}) = \frac{4V_{bd}^2}{\varepsilon\mu_0 E_C^3}\left[1+\left(\frac{N_D\xi(T_{on})}{N_{ref}}\right)^{\beta}\right]\left(\frac{T_{on}}{300}\right)^{\gamma}\frac{\xi(T_{off})}{\xi(T_{on})}$$

$$Z_{th} = D\cdot R_{th} + (1-D)\cdot Z_0\,(1/f)$$







Mahajan, Chen et al., Self-Heating and Reliability-Aware “Intrinsic” SOA, TED, 2022.

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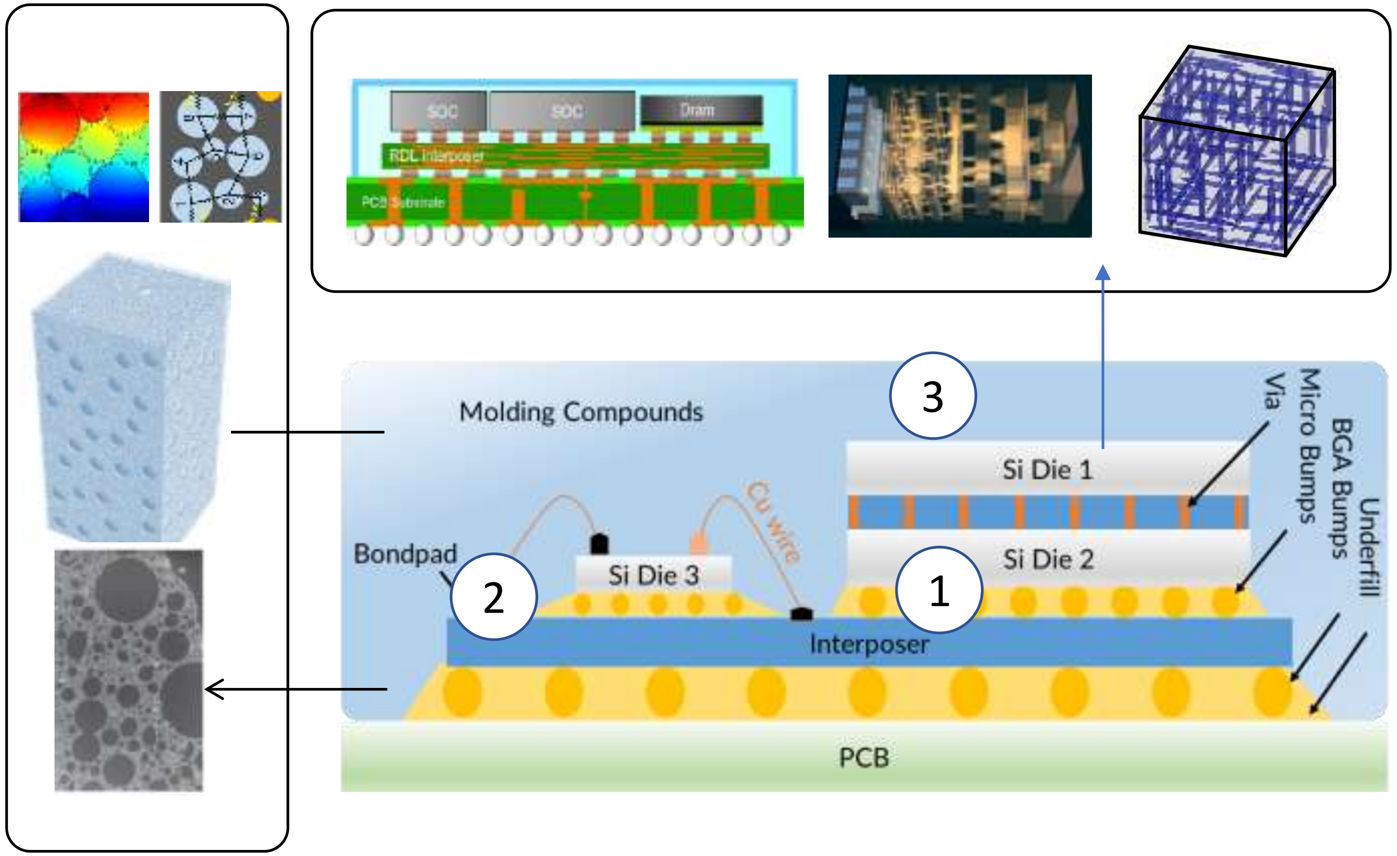
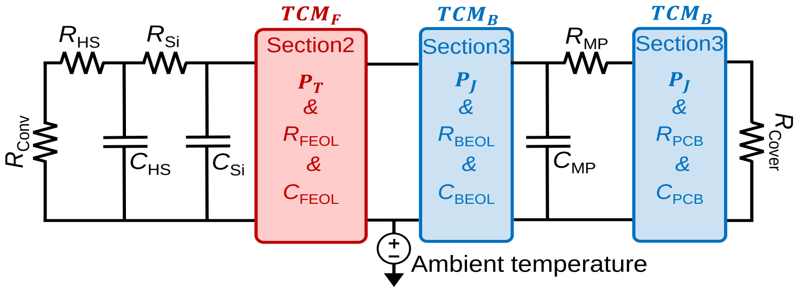
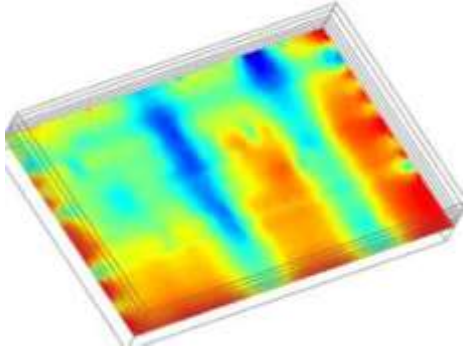
Multi-scale, multi-physics electro-thermal-mechanical environment



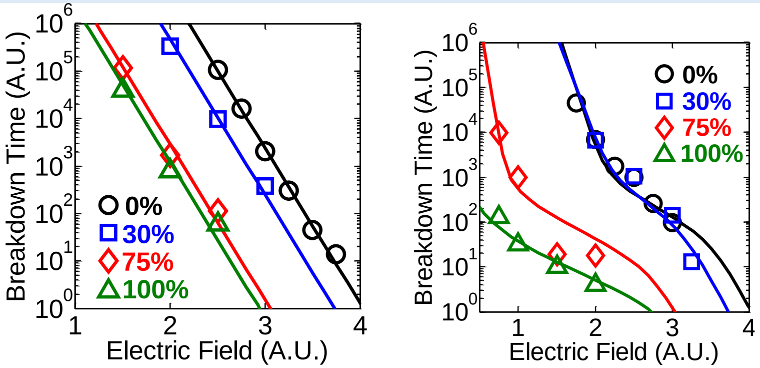




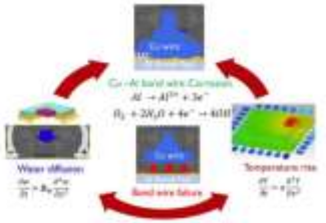
W. Ahn and Alam, TED, 2017; MR 2018.

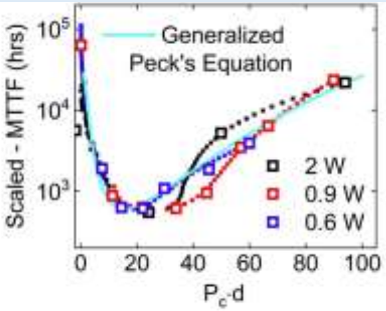
Electrothermal reliability of 3D-HI

1. RDL PI dielectric failure (Palit, JAP, 2018)

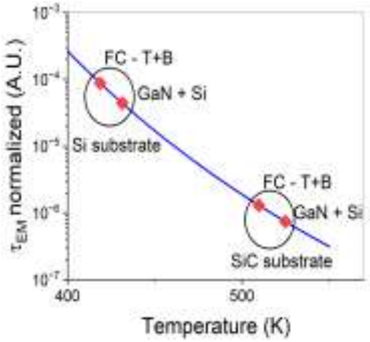


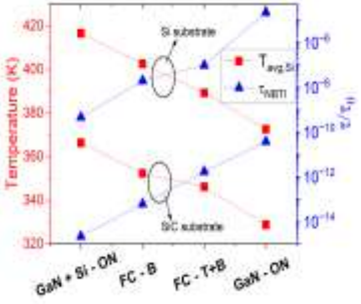
2. Bond corrosion failure (Asad, IRPS, 2021)





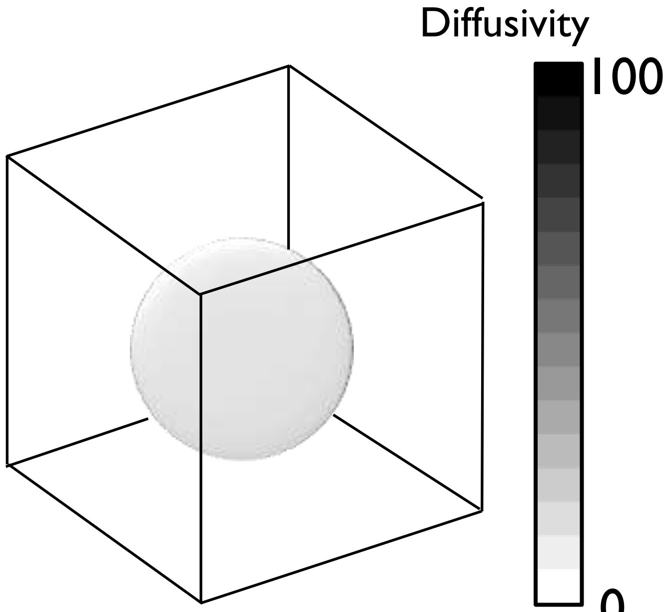
3. Transistor failure due to EM, HCI, NBTI



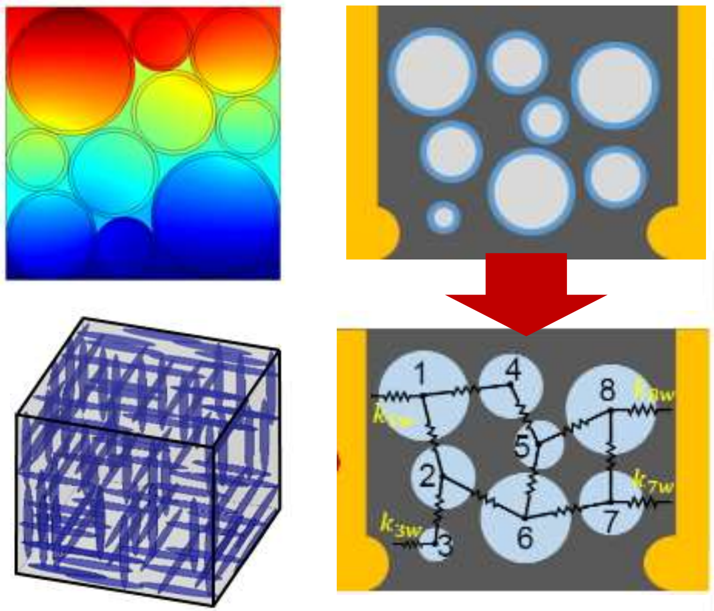


Packaging reliability requires new techniques

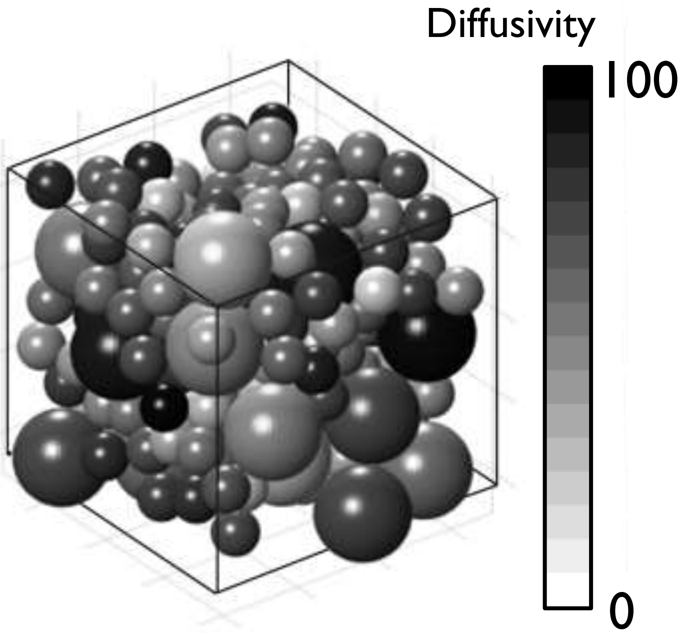
Effective medium theory (MG model)



Our approach (Generalized EMT)

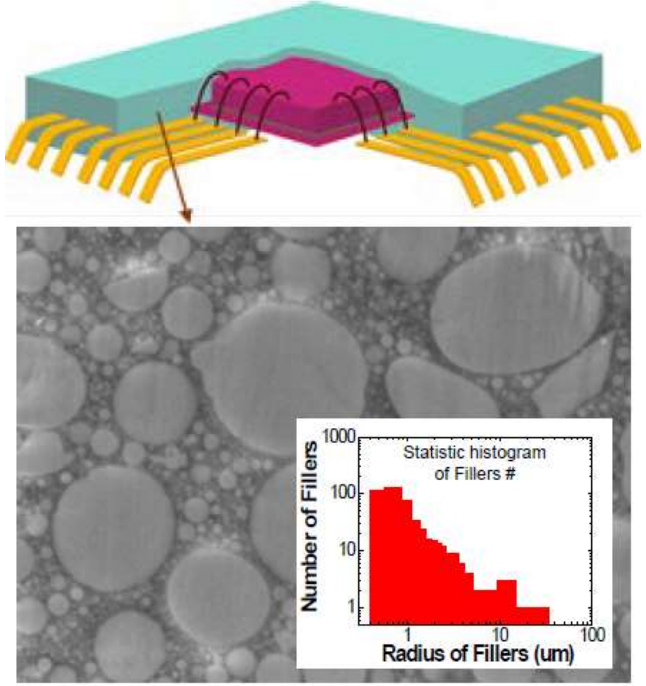


Percolation theory

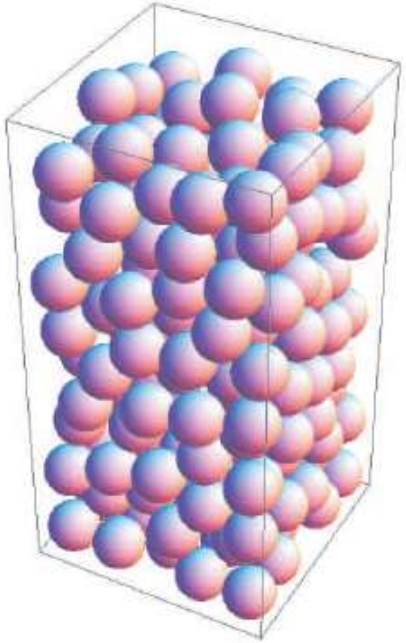


Small Volume fraction, contrast ratio **Large**

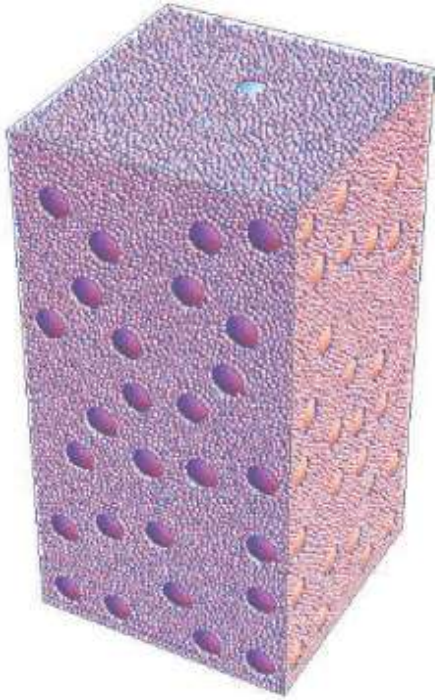
Packing in epoxy-glass mold compound



Filler ~5-50 micron

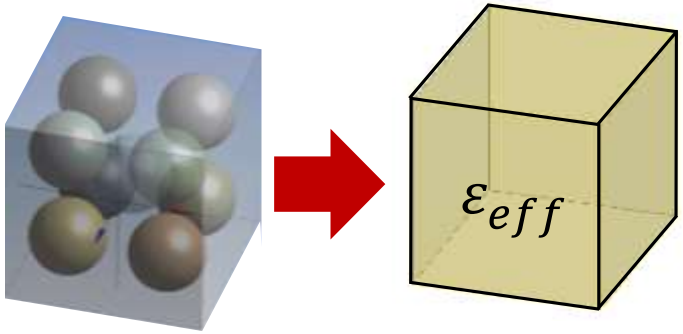


~60%

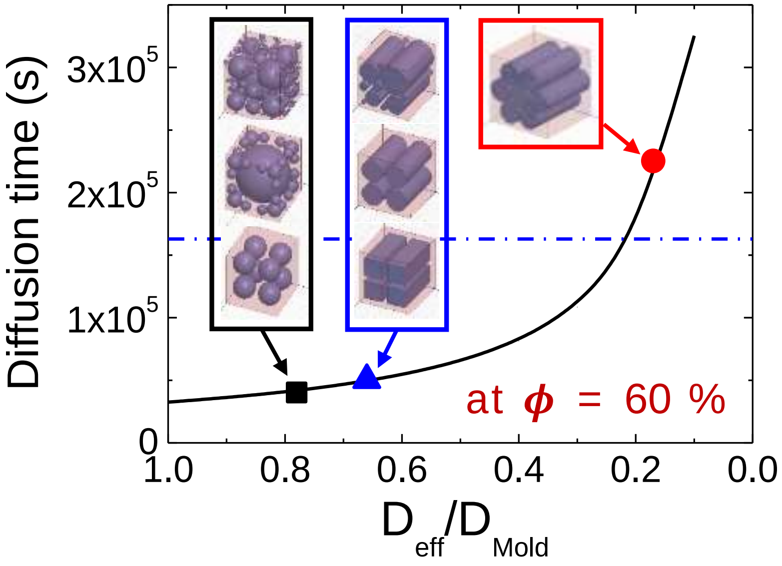


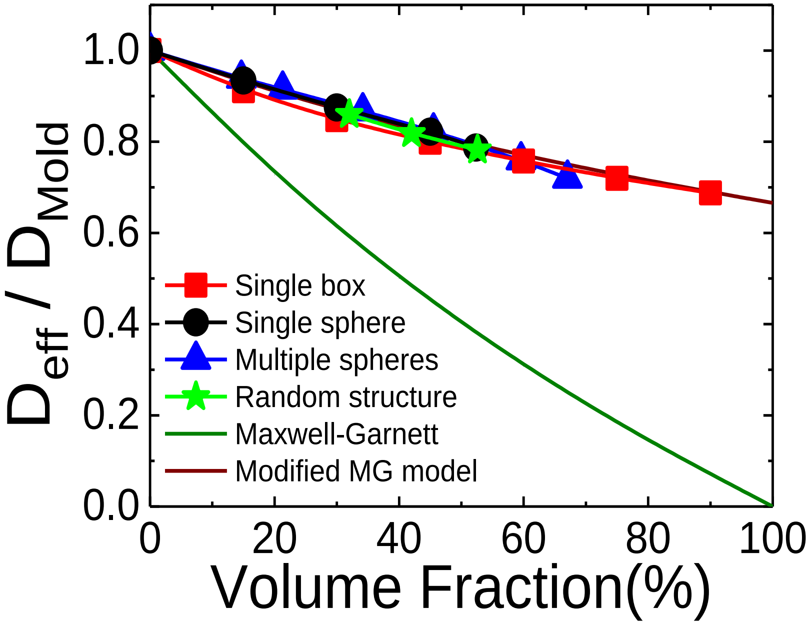
~80%

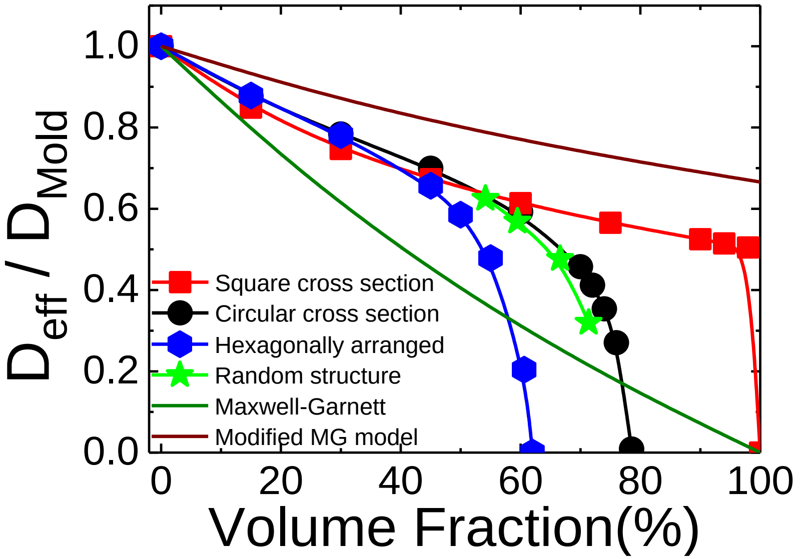
Moisture ingress in polymers & mold-compounds

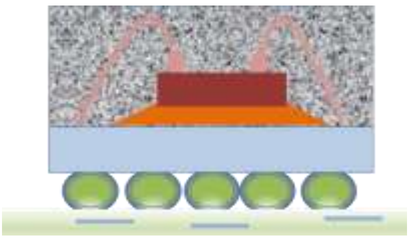


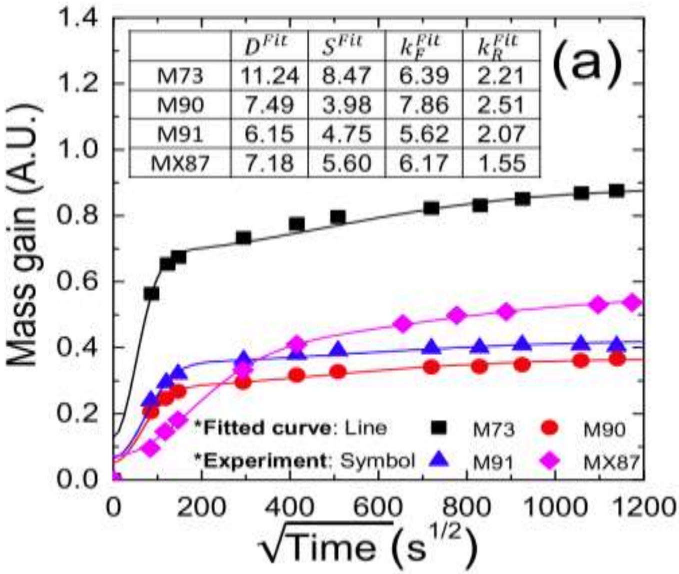
For moisture diffusion,
EMT model needs to be modified!





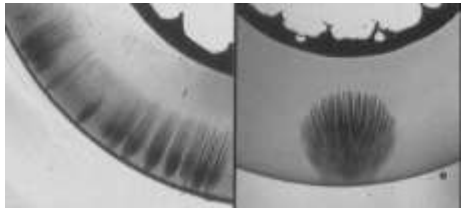


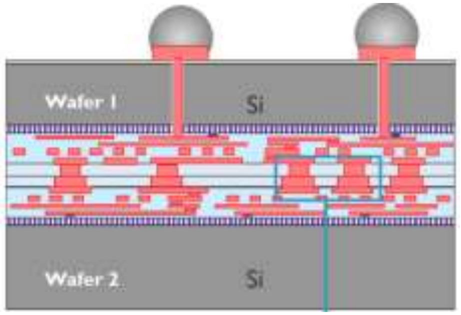


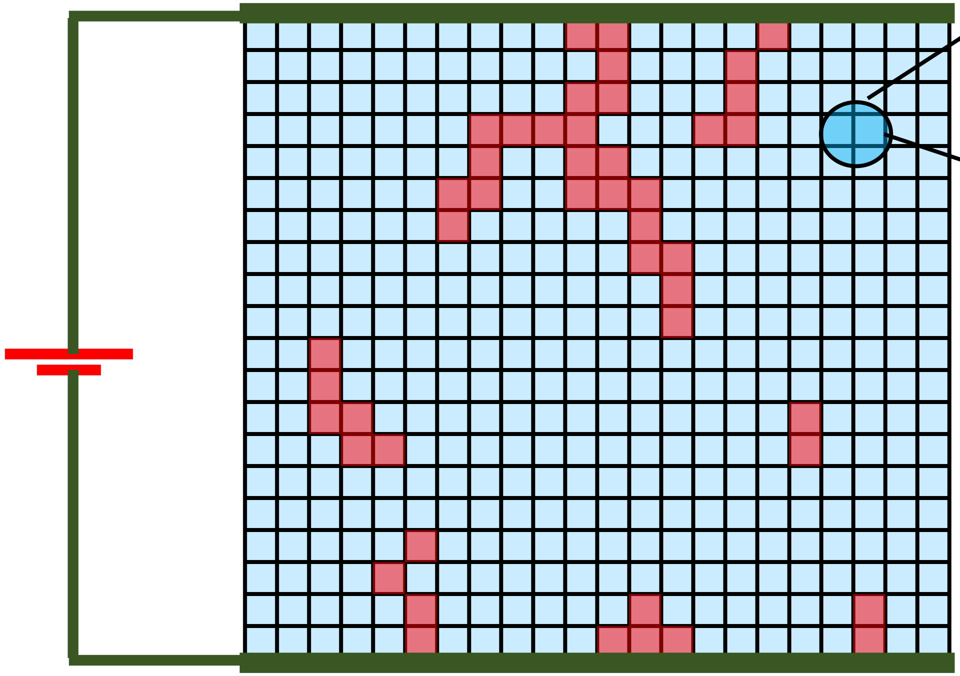


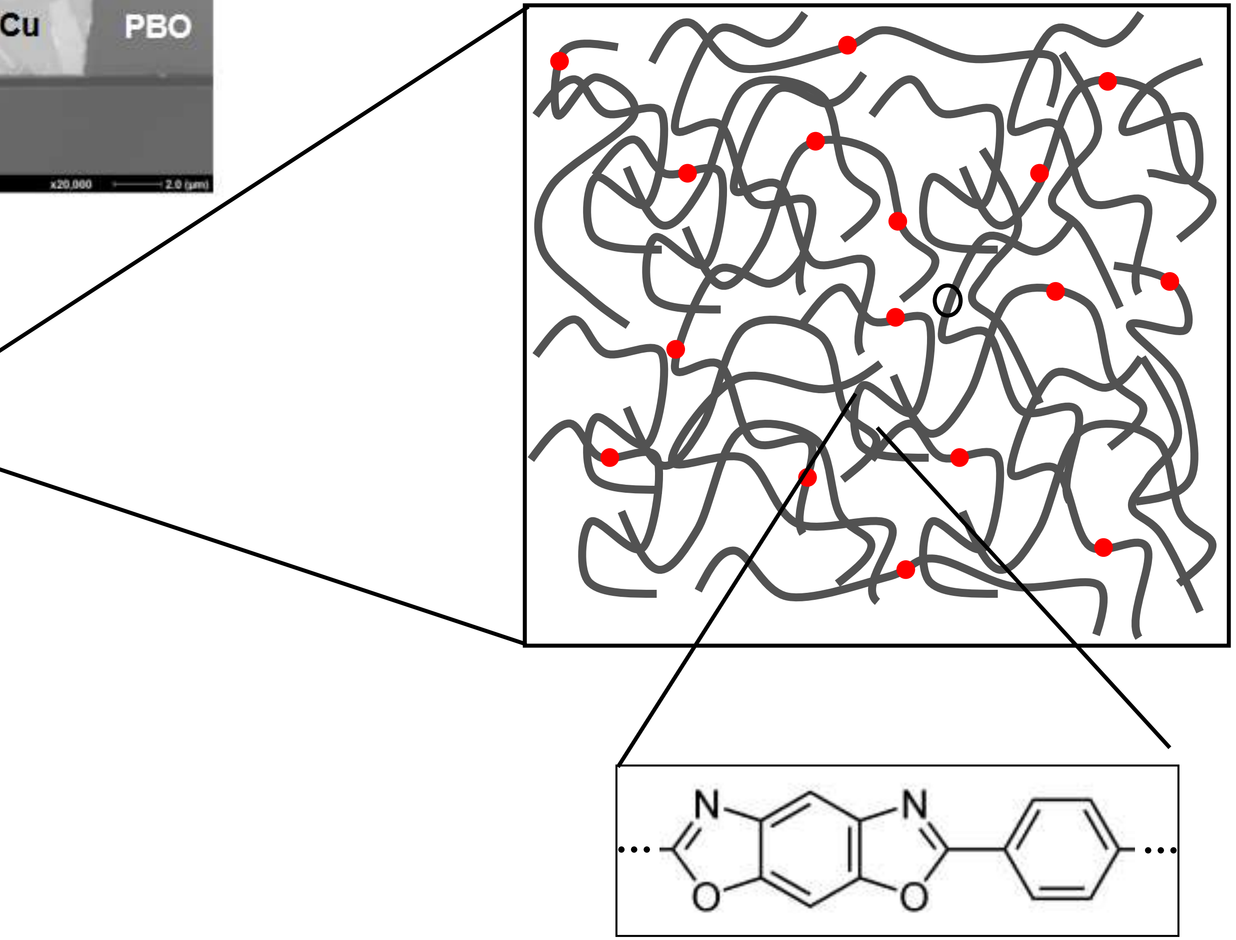
	D^{Fit}	S^{Fit}	k_F^{Fit}	k_R^{Fit}
M73	11.24	8.47	6.39	2.21
M90	7.49	3.98	7.86	2.51
M91	6.15	4.75	5.62	2.07
MX87	7.18	5.60	6.17	1.55

Dielectric Breakdown: BEOL/RDL/TSV Oxides



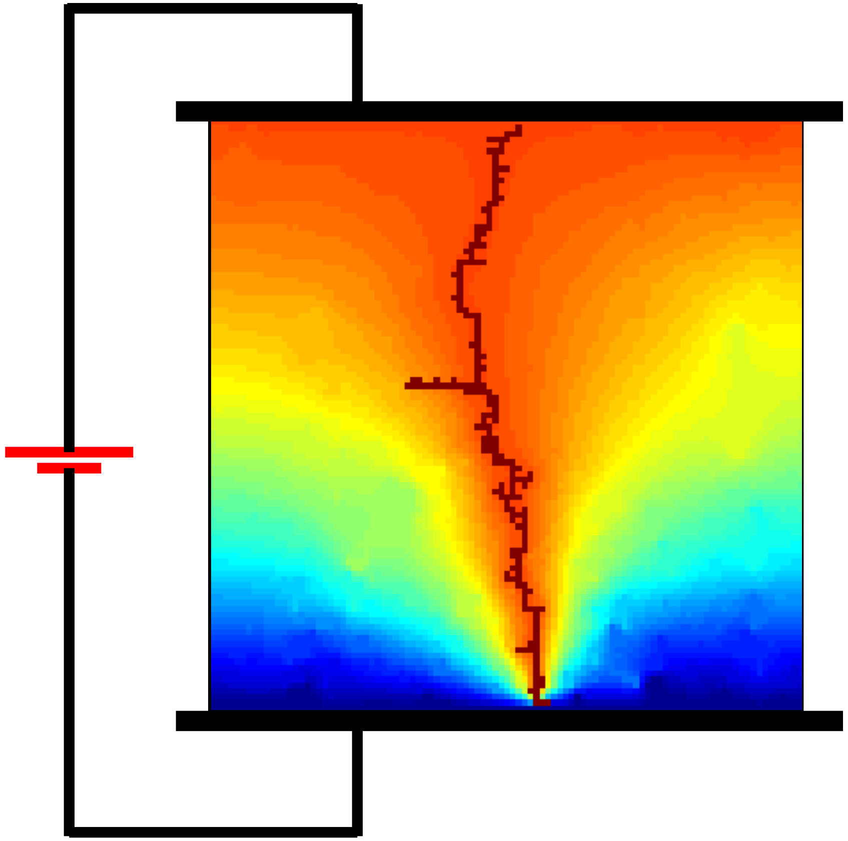






Poly-Benzo-Oxazole (PBO) monomer

Dielectric heating & breakdown rates



$$\frac{dN}{dt} = -N \times \frac{k_B T}{h} \exp\left(-\frac{\Delta G - aE}{kT}\right)$$

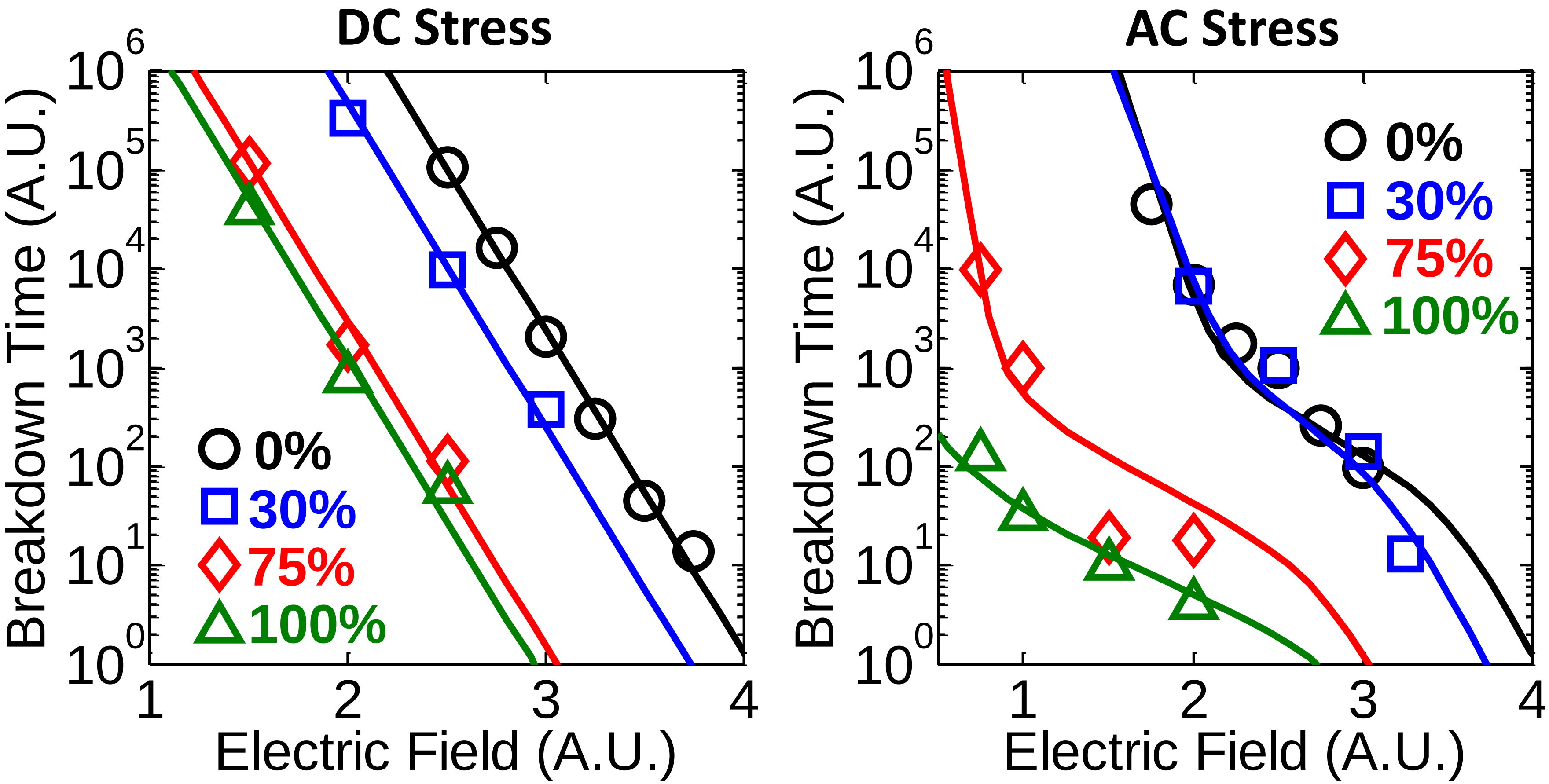
$$T_F = \frac{h}{kT}\log\left(\frac{1}{1-\eta}\right)\exp\left(\frac{\Delta G - aE}{kT}\right)$$

$$T(t) \approx T_0 + \frac{\omega\varepsilon_r''\varepsilon_0 E^2 T_d}{2h}\left[1 - e^{-\frac{2\beta t}{C_P\rho T_d}}\right]$$

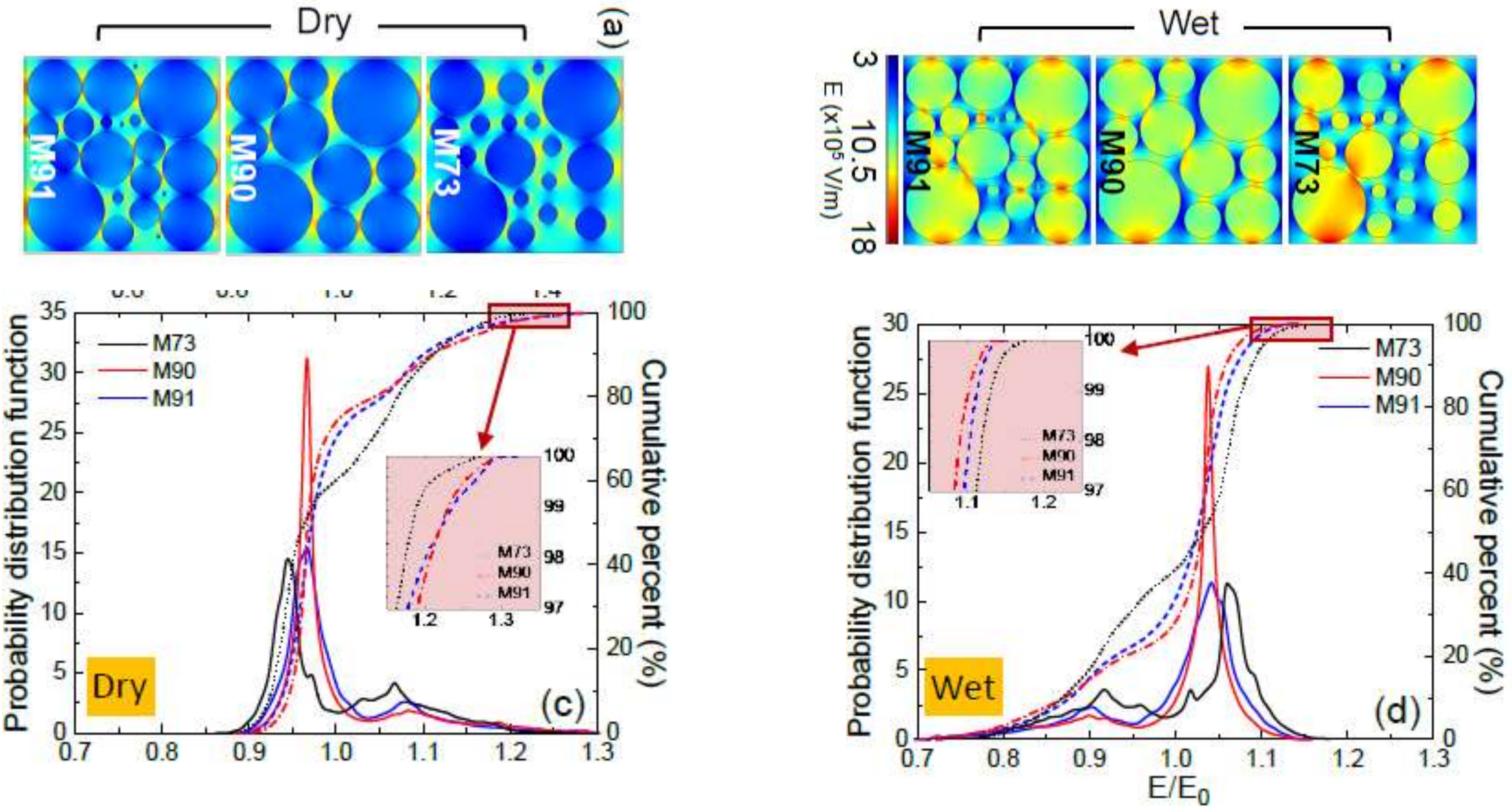
$$C_P\rho V\frac{dT}{dt} = \omega\varepsilon_r''\varepsilon_0 E^2 V - \beta A\left(T - T_0\right)$$

Humidity reduces lifetime

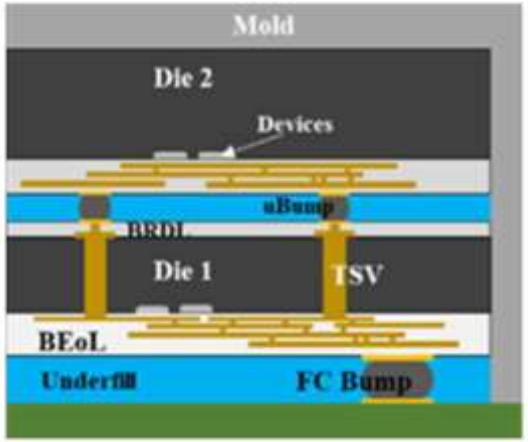
$$T_F \approx \frac{h}{k\left(T_0 + \Delta T\right)} \log\left(\frac{1}{1-\eta}\right) \exp\left(\frac{\Delta G - aE}{k\left(T_0 + \Delta T\right)}\right) \qquad \Delta T = \frac{\omega \varepsilon_r'' \varepsilon_0 E^2 T_d}{2\beta}$$

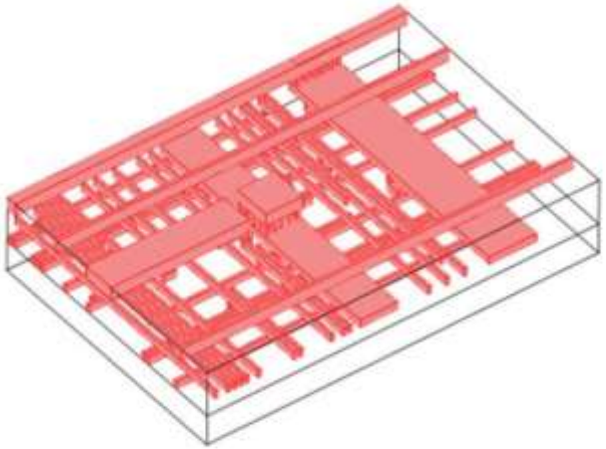


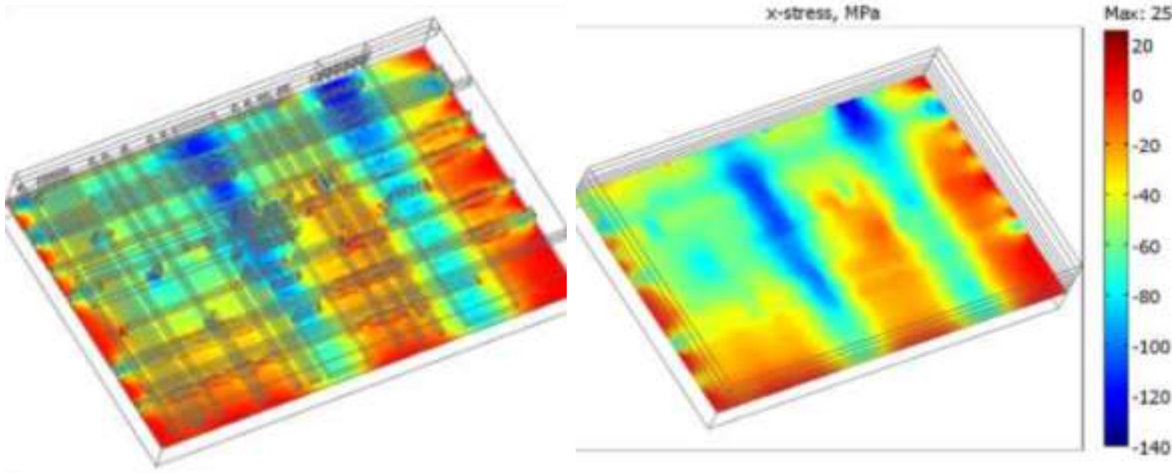
Dielectric breakdown in Mold-Compounds



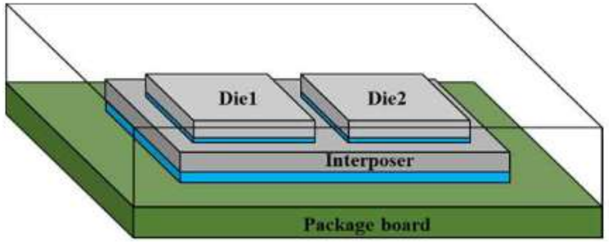
CPI stress aware Front-End design

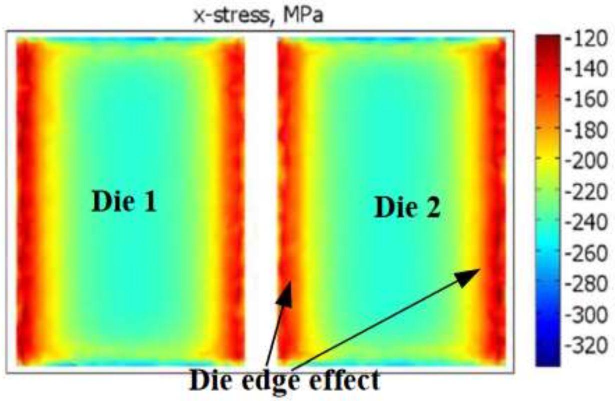


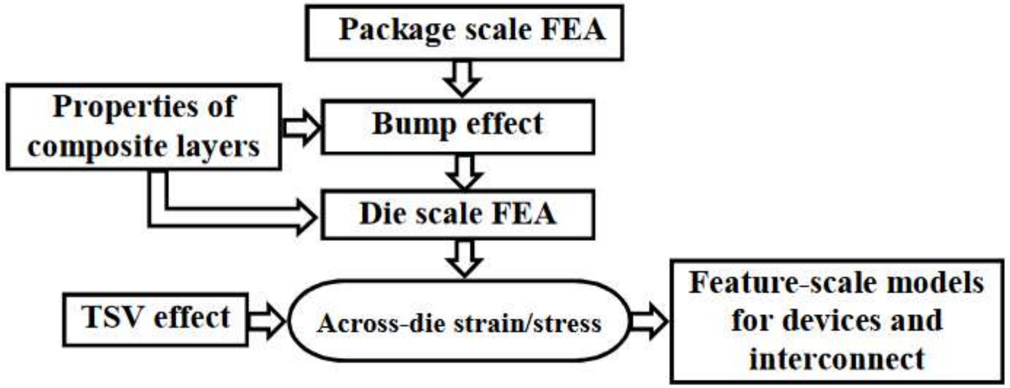




THERMO-MECHANICAL PROPERTIES OF COMPOSITE LAYERS






Package scale FEA

Properties of composite layers

Bump effect

Die scale FEA

TSV effect

Across-die strain/stress

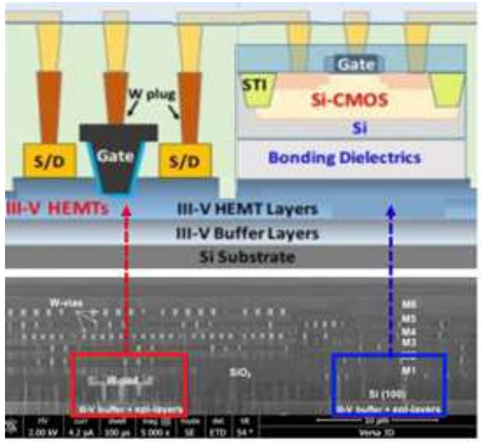
Feature-scale models for devices and interconnect

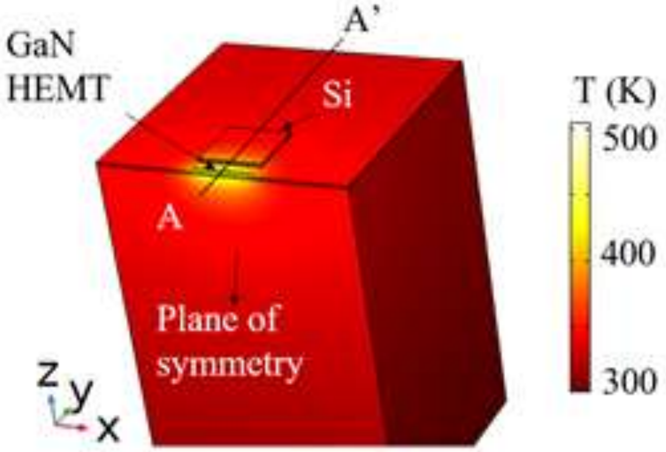
Figure 5. Multi-scale stress simulation flow.

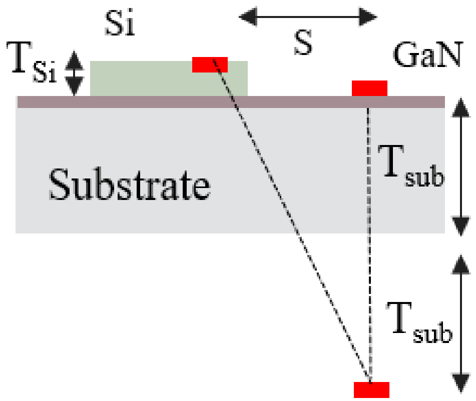
A. Kteyan et al., IRPS 2019

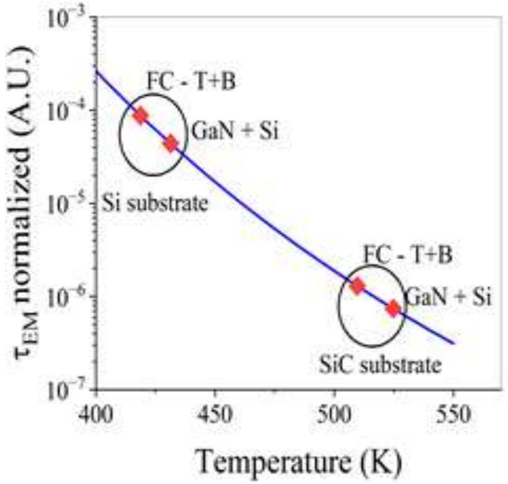
Thermal Crosstalk: Need of a Keep-out-Zone

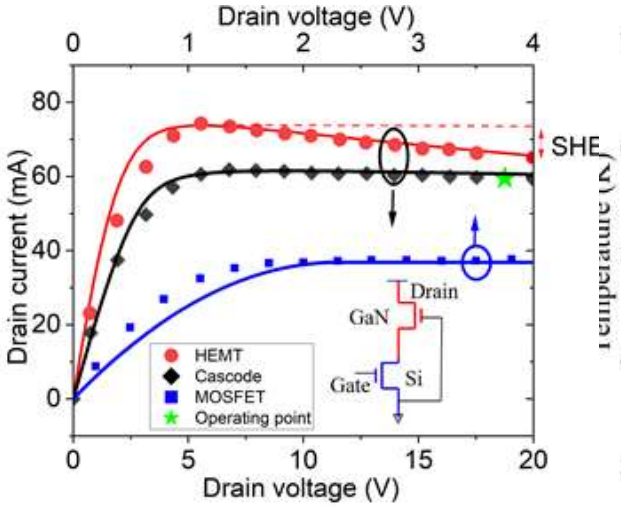
Sruthi M.P. et al, 2022.

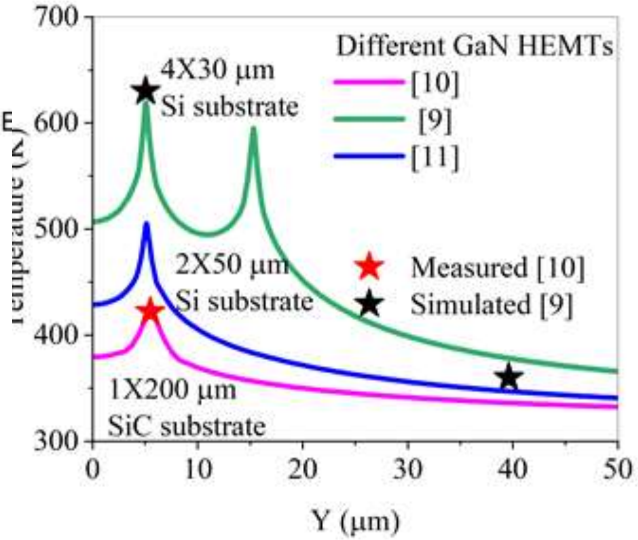


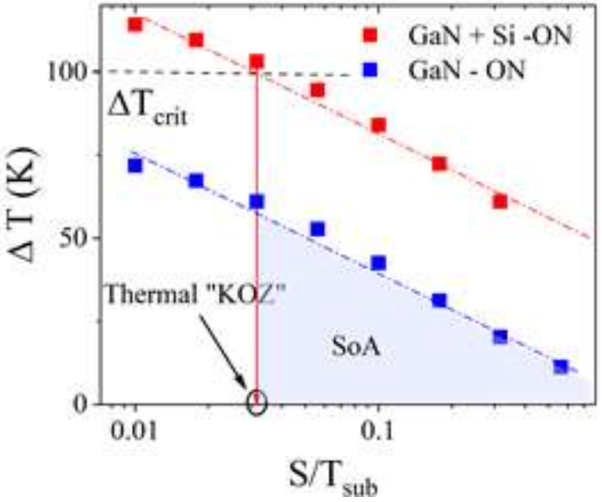


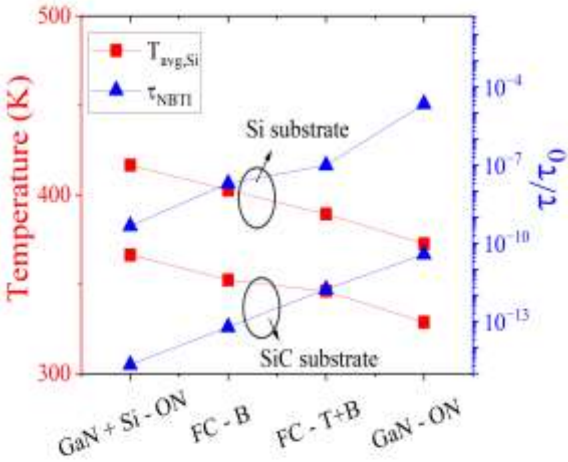












Outline

- Introduction: Moore's law is dead, long-live Moore's law
- Self-heating in logic transistors: An enduring challenge
- BEOL-integrated transistors: The next-frontier?
- The brave-new world of FeFET and NCFET
- Rethinking reliability of power-transistors
- Reliability of 3D Heterogeneously integrated Systems
- Packaging in extreme-environment: Biosensors
- Summary

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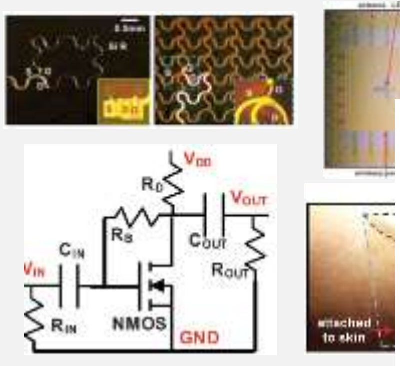
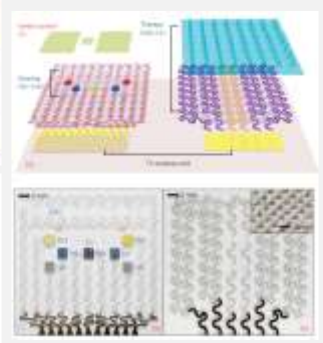
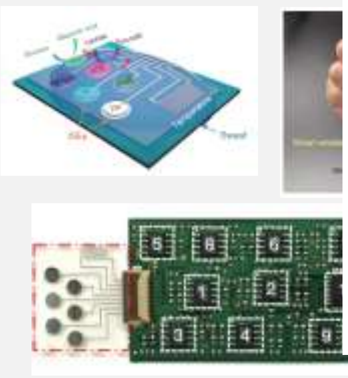
Extreme packaging: Pharmaceutical vs. Electroceutical



Kim *et al.*



ee *et al.*

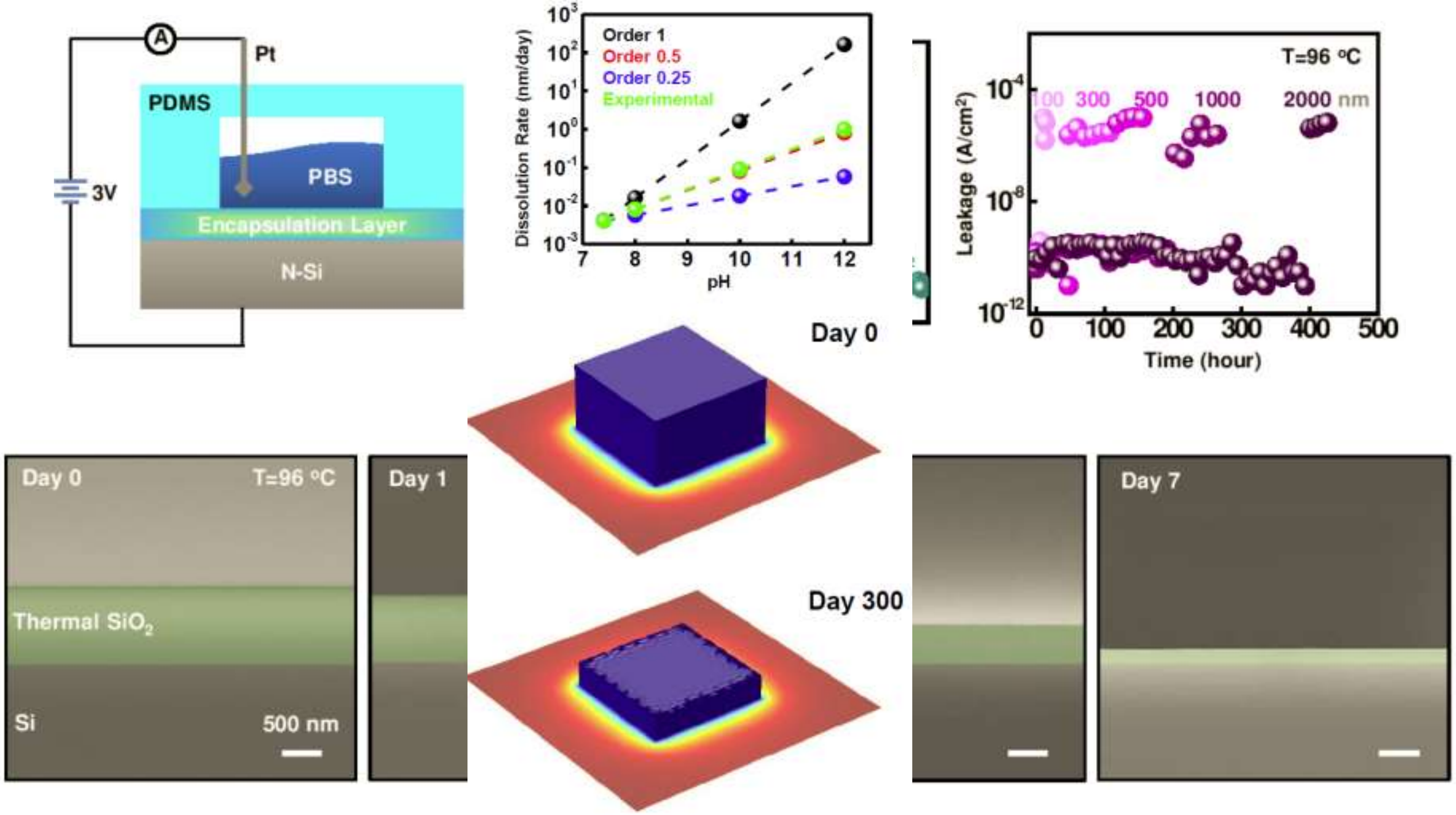


Gao *et al.*

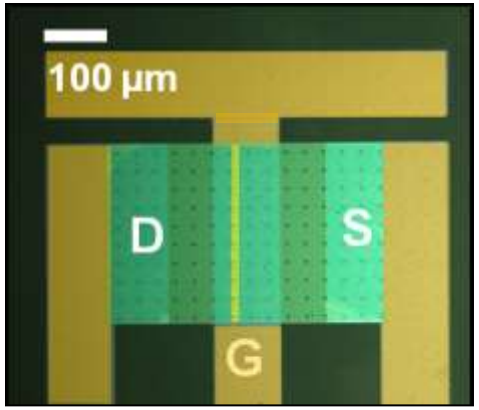
Schwartz *et al.*

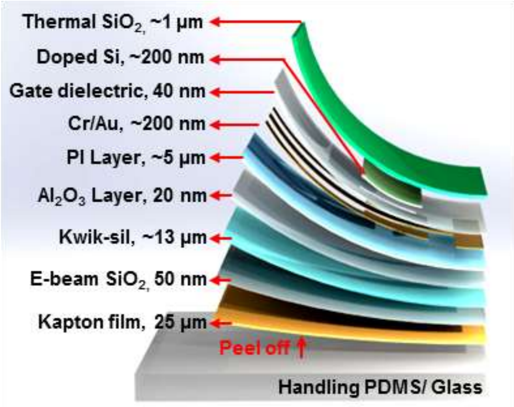
Kim *et al.*

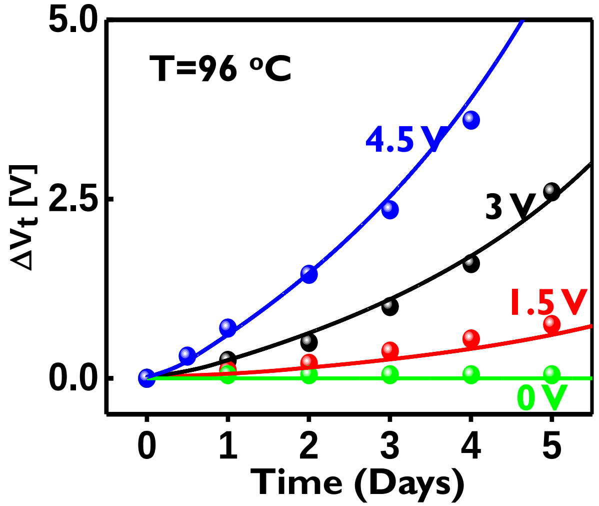
Extreme Packaging: Oxide dissolution in DI water



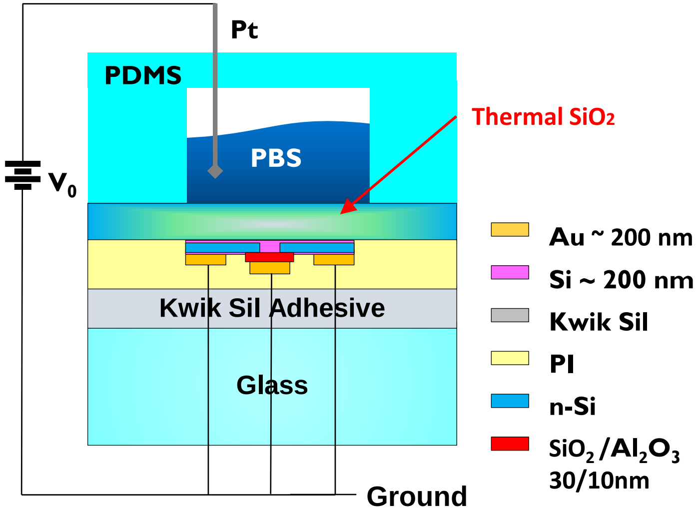
Extreme Packaging: Ion diffusion in encapsulants

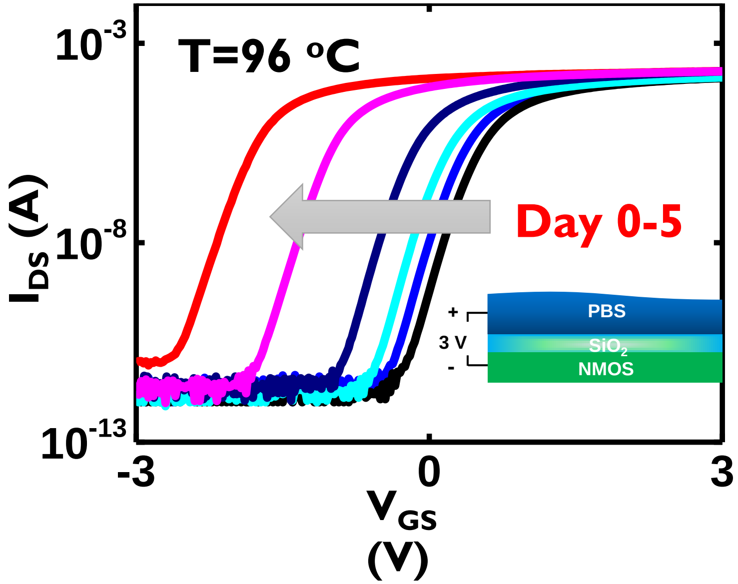




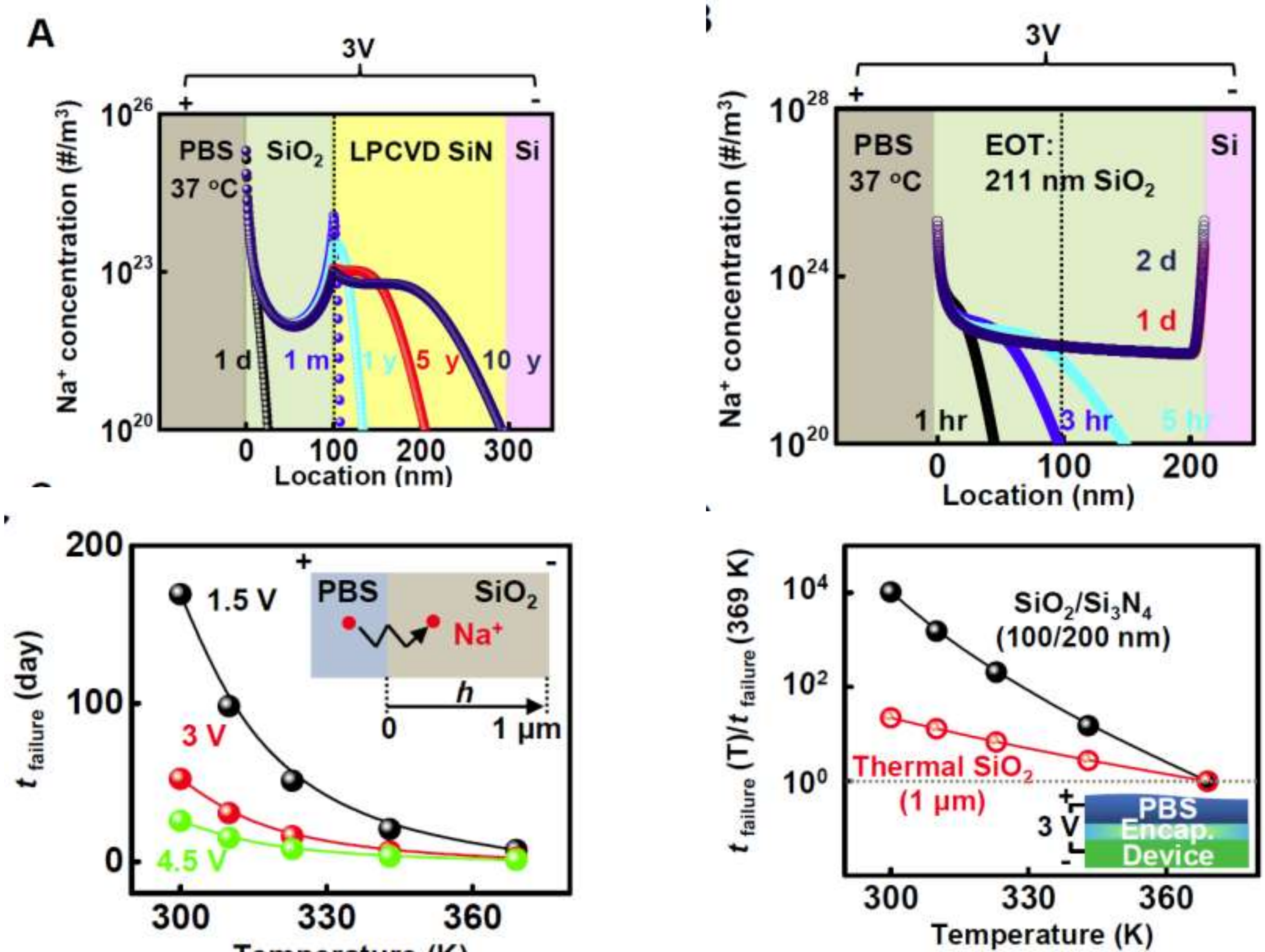


Xin Jin, TED, PNAS, 2016





Extreme Packaging and stacked encapsulant



Conclusions: Take-home points

- Moore's law is dead, long-live Moore's law
  - Moore's law will live through 3D integration. Thermal bottleneck is a concern.
- Self-heating in logic transistors: An enduring challenge
  - Serious challenge in application-specific design in a broad range of applications
- BEOL-integrated transistors: The next-frontier?
  - Performance is significant, but reliability could be a concern.
- The brave-new world of FeFET and NCFET
  - Most important reliability issues are classical. New degradation pathways exist.
- Rethinking reliability of power-transistors
  - Self-heating and reliability are first order concerns.
- Reliability of 3D Heterogeneously integrated Systems
  - Many new modes of degradation, especially in harsh environments. Front-end reliability physics can be selectively used for reliability issues involving chip-package interaction.
- New characterization techniques and modeling tools are essential.

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