IEEE 1979 SISC TECHNICAL PROGRAM

Technical Program Chairman:
Dirk Bartelink, Xerox Palo Alto Research Center, Palo Alto, CA 94304

SESSION I: MICROSCOPIC MODELS OF INTERFACES

8:45 AM – Thursday, 29 November 1979

Chairmen: John Brews, Bell Laboratories, Murray Hill, NJ; and Joe Maserjian, Jet Propulsion Laboratory, Pasadena, CA

1.1 *ESR Studies of Si/SiO_2 Interface Defects on (111) and (100) Silicon*
–E. H. Poindexter and P. J. Caplan, US Army Electronics Technology and Devices Laboratory (ERADCOM), Fort Monmouth, NJ; and B. E. Deal and R. R. Razouk, Research and Development Laboratory, Fairchild Camera and Instrument Corporation, Palo Alto, CA

1.2 *A Chemical Model of $Si-SiO_2$ Surface States – Revisited Ten Years Later*
–R. Schmidt, Bell Labs, Murray Hill, NJ

1.3 *Selection of III-V Compounds for Either Schottky Barrier or MIS Based Devices*
–W. E. Spicer, I. Lindau, P. Skeath, and C. Y. Su, Stanford University, Stanford, CA

1.4 *Local Atomic Structure of Trapped Charge Sites at the Si/SiO_2 Interface Using High Resolution XPS*
–F. J. Grunthaner, B. F. Lewis, and J. Maserjian, Jet Propulsion Laboratory, Pasadena, CA

1.5 *Impurity Induced Interface States*
–J. Snel, Philips Research Laboratories, Eindhoven, The Netherlands

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1.6 *Steam Oxidation of Refractory Metal Silicides*
–J. E. E. Baglin, F. M. d'Heurle, and S. Petersson, IBM T.J. Watson Res. Ct., Yorktown Heights, NY

SESSION II: PROCESS TECHNOLOGY:DIFFUSION AND GATE DIELECTRICS

1:30 PM – Thursday, 29 November 1979

Chairmen: Pallab Chatterjee, Texas Instruments, Inc., Dallas, TX; and T. P. Ma, Yale University, New Haven, CT

2.1 *Effect of Oxidation-Enhanced Boron Diffusion on Recessed-Oxide Isolation for MOSFET Integrated Cicuits*
–V.L. Rideout, F.F. Morehead, and B.L. Crowder, IBM T.J. Watson Res. Ct., Yorktown Heights, NY

2.2 *The Lateral Effect of Oxidation-Enhanced Diffusion (LOED) in <100> Silicon*
–A. M. Lin and R. W. Dutton, Stanford University, Stanford, CA, and D. A. Antoniadis, Massachusetts Institute of Technology, Cambridge, MA

2.3 *Diffusion of Aluminum into Thin Oxide Films on Silicon*
–F. M. Fowkes and Y.-H. Yeh, Lehigh University, Bethlehem, PA

2.4 *Improved Oxide of MOS Resulting from Backside Argon Implantation*
–B. H. Yun, IBM Data Systems, Division, East Fishkill Hopewell Junction, NY

2.5 *The Direct Thermal Nitridation of Silicon in an RF Activated N_2 Plasma*
–F. M. Erdmann and M. M. Beguwala, ERC Rockwell International, Anaheim, CA

2.6 *Thermally Grown Silicon Oxynitride Films: Characterization and Application*
–T. W. Ekstedt and J. Manoliu, Hewlett-Packard Laboratories, Palo Alto, CA

2.7 *Effects of SiN Encapsulation on the MOS Device Stability*
–R. C. Sun, J. T. Clemens, and J. T. Nelson, Bell Telephone Laboratories, Inc., Allentown, PA

2.8 *Time-Dependent Buildup of Interface States Following Pulsed e-Beam Irradiation*
–P. S. Winokur, H. E. Boesch, Jr., F. B. McLean, and J. M. McGarrity, Harry Diamond Laboratories, Adelphi, MD

SESSION III: INTERFACE CHARACTERIZATION

8:45 AM -- Friday, 30 November 1979

Chairmen: Bob Helms, Stanford University, Stanford, CA; and Dimitri Antoniadis, Massachusetts Institute of Technology, Cambridge, MA

3.1 *Charge Trapping Studies in SiO_2 Using High Current Injection from Si-Rich SiO_2 Films*
—D. J. DiMaria, R. A. Ghez, and D. W. Dong, IBM T. J. Watson Res. Ct, Yorktown Heights, NY

3.2 *Determination of Interface-State Density and Cross Section in n-MOS and p-MOS Capacitors by DLTS*
—T. J. Tredwell, Eastman Kodak Company, Rochester, NY; and C. R. Viswanathan, University of California, Los Angeles, CA

3.3 *Gate Current in MOS Devices as a Tool for Evaluation of Interface Characteristics in Short Channel Devices*
—B. Eitan and D. Frohman-Bentchkowsky, The Hebrew University of Jerusalem, Jerusalem, Israel

3.4 *An XPS/AES Study of Palladium Schottky Barriers on Hydrogenated Amorphous Silicon*
—J. H. Thomas III and D. E. Carlson, RCA Laboratories, Princeton, NJ

3.5 *Experimental Determination of Electron and Hole Tunneling Barriers of Ultrathin SiO_2 Films in MOS Structures*
—H. C. Card and K. K. Ng, Columbia University, New York, NY

3.6 *The Detection and Characterization of Flaws in SiO_2 Using a Si/SiO_2/Electrolyte Configuration*
—S. R Morrison, M. J. Madou, and K. W. Frese, Jr., SRI International, Menlo Park, CA

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3.7 *Time-Resolved Charge Injection Measurements of Schottky Barriers in Ultrahigh Vacuum*
—J. H. Slowik, L. J. Brillson, and C. F. Brucker, Xerox Webster Research Center, Webster, NY

SESSION IV: INTERFACE EFFECTS IN SMALL DEVICE STRUCTURES

1:30 PM — Friday, 30 November 1979

Chairmen: Al Tasch, Texas Instruments, Inc., Dallas, TX; and Bernd Hoefflinger, University of Dortmund, Germany

INVITED PAPER: *The Outer Limits of Si VLSI*
J. L. Moll, Hewlett-Packard Laboratories, Palo Alto, CA

4.1 *Comparison of Interconnection Capacitances on Silicon, Sapphire and Semi-Insulate Gallium Arsenide Substrates*
—H. T. Yuan, S. Y. Chiang, and Y. T. Lin, Texas Instruments Inc., Dallas, TX

4.2 *Electron Mobility in Inversion and Accumulation Layers on Thermally Oxidized Silicon Surfaces*
—S. C. Sun and J. D. Plummer, Stanford University, Stanford, CA

4.3 *Mobility and Saturation Velocity as Independent Parameters for Drift Velocity*
—K. K. Thornber, Bell Laboratories, Murray Hill, NJ

4.4 *Submicron-Channel High-Voltage MOSFET's*
—J. Tihanyi, Siemens AG, Munich, Germany

4.5 *Real Space Transfer of Hot Electrons in $Al_xGa_{1-x}As$-GaAs Heterostructures*
—K. Hess, B. G. Streetman, Y. Shichijo, and H. Morkoz, University of Illinois, Urbana, IL

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4.6 *High Field Electron Transport in SOS Layers*
—R. K. Cook and Jeffrey Frey, Cornell University, Ithaca, NY

SESSION V: FABRICATION, ANNEALING & CHARACTERIZATION OF THIN LAYERS PART I

8:45 AM – Saturday, 1 December 1979

Chairmen: Moiz Beguwala, Rockwell International, Anaheim, CA; and Murray Woods, Intel

INVITED PAPER: *Beam Annealing at Interfaces and Near-Interface Regions*
J. F. Gibbons, Stanford University, Stanford, CA

5.1 *Recent Results on RF Annealing: Radiation-Induced Electron Traps in MOS Structures*
—T. P. Ma and M. R. Chin, Yale University, New Haven, CT

5.2 *The Effect of Hydrogen Annealing on Interface States in Thermally Oxidized Silicon*
—R. R. Razouk and B. E. Deal, Fairchild Camera and Instrument Corporation, Palo Alto, CA

5.3 *Kinetics of CVD Silicon Dioxide Annealing*
—R. M. Swanson and T. M. Hall, Stanford University, Stanford, CA

5.4 *Oxidation Characteristics of Refractory Silicide Films*
—J. E. E. Baglin, F. M. d'Heurle, C. Lucchese, S. Petersson, and S. Zirinsky, IBM T. J. Watson Research Center, Yorktown Heights, NY

5.5 *Physical Properties of Steam Oxidized WSi_2*
—F. Mohammadi, J. Rouse, K. C. Saraswat, and C. R. Helms, Stanford University, Stanford, CA

SESSION VI: FABRICATION, ANNEALING & CHARACTERIZATION OF THIN LAYERS PART II

1:30 PM – Saturday, 1 December 1979

Chairmen: Dan DiMaria, IBM T. J. Watson Research Center, Yorktown Heights, NY and Yuji Okuto, Nippon Electric Company, Ltd., Kanagawa Prefecture, Japan

6.1 *A New Passivation Method of GaAs Surfaces by GaO_xN_y and GaO_xN_y-Based Multilayer*
—J. Nishizawa and I. Shiota, Tohoku University, Sendai, Japan

6.2 *Interface Properties of Plasma Grown GaAs Oxides*
—R. P. H. Chang, Bell Laboratories, Murray Hill, NJ

6.3 *MBE Growth of Thin Silicon Films on Sapphire and Spinel*
—J. C. Bean, Bell Laboratories, Murray Hill, NJ

6.4 *Studies of Semi-Insulating Polycrystalline Silicon (SIPOS) Using AES and PES*
—T. Adachi and C. R. Helms, Stanford University, Stanford, CA

6.5 *Examination of Thin Silicon Nitride Layers on MNOS Tunneling Oxides by X-Ray Photoelectron Spectroscopy*
—J. A. Wurzbach and F. J. Grunthaner, Jet Propulsion Laboratory, Pasadena, CA

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6.6 *Steady State Space Charge Distribution in LPCVD and APCVD Silicon Nitride Films*
—F. L. Hampton and J. R. Cricchi, Westinghouse Electric Corporation, Baltimore, MD