IEEE 1980 SISC PRELIMINARY PROGRAM

Technical Program Chairman:
Joe Maserjian, Caltech-Jet Propulsion Laboratory, Pasadena, CA 91103

SESSION I: MICROSCOPIC MODELS OF INTERFACES

8:45 AM – Thursday, 4 December 1980

Chairmen: John Brews, Bell Laboratories, Murray Hill, NJ; and Don Young, IBM T. J. Watson Research Center, Yorktown Heights, NY

1.1 *Chemical Modeling of Intermediate Oxidation States and Bond Rearrangement of the Si/SiO_2 Interface*
– F. J. Grunthaner, P. J. Grunthaner, R. P. Vasquez, J. A. Wurzbach, B. F. Lewis and J. Maserjian, Caltech-Jet Propulsion Laboratory, Pasadena, CA

1.2 *The Origin and Nature of Silicon Band Gap States at the Si/SiO_2 Interface*
– J. Singh and A. Madhukar, University of Southern California, Los Angeles, CA

1.3 *Impurity Segregation at the Si/SiO_2 Interface*
– R. W. Barton, J. Rouse, L. A. Schwarz and C. R. Helms, Stanford University, Stanford, CA

1.4 *Dual Electron Injection Structure Electrically-Alterable Read-Only-Memory Studies*
– D. J. Di Maria, K. M. De Meyer, and D. W. Dong, IBM T. J. Watson Research Center, Yorktown Heights, NY

1.5 *Toward a Model of Radiation-Induced Interface States in SiO_2 MOS Structures*
– F. B. McLean, P. S. Winokur, and H. E. Boesch, Jr., Harry Diamond Laboratories, Adelphi, MD

SESSION II: ANALYSIS AND CHARACTERIZATION TECHNIQUES

3:00 PM – Thursday, 4 December 1980

Chairmen: Peter Gray, General Elecectric CRD, Schenectady, NY; and Frank Grunthaner, Caltech-Jet Propulsion Laboratory, Pasadena, CA

2.1 *Oscillations in Fowler-Nordheim Tunneling as a Probe of the Si/SiO_2 Interface*
– N. Zamani and J. Maserjian, Caltech-Jet Propulsion Laboratory, Pasadena, CA

2.2 *Response of Si^{III} Centers at the Si-SiO_2 Interface to Surface Potential and Variable-Temperature Anneals*
– N. M. Johnson, D. K. Biegelsen and M. D. Moyer, Xerox Palo Alto Research Center, Palo Alto, CA; P. J. Caplan and E. H. Poindexter, Army Electronics Technology and Devices Laboratory, Fort Monmouth, NJ

2.3 *Thermally Stimulated Hole Currents in Thermal Silicon Dioxide*
– M. Bakowski, Chalmers University of Technology, Sweden

2.4 *Structural Analysis of Semiconductor Interfaces by Ion Scattering*
– L. C. Feldman, Bell Laboratories, Murray Hill, NJ

2.5 *Determination of Semiconductor Interface Potentials and Heterojunction Band Discontinuities by XPS*
– R. W. Grant, E. A. Krout, J. R. Waldrop and S. P. Kowalczyk, Rockwell Intern. Electronics Research Center, Thousand Oaks, CA

2.6 *Correlation of Impurities to Electron Traps in SiO_2*
– A. Hartstein and D. R. Young, IBM T. J. Watson Research Center, Yorktown Heights, NY

2.7 *Native Polarization Layer at the SOS Interface?*
– P. Krusius, C. Dube and J. Frey, Cornell University, Ithaca, NY

SESSION III: INTERFACE EFFECTS IN SMALL STRUCTURES

8:45 AM – Friday, 5 December 1980

Chairmen: Jeff Frey, Cornell University, Ithaca, NY; and Jim Plummer, Stanford University, Stanford, CA

3.1 *Crystalline Quality of Si Films Formed on the Si (111)/Cosilicide Structure by Molecular Beam, Solid Phase, and Laser-Induced Epitaxies*
– H. Ishiwara, S. Saitoh, and S. Furukawa, Tokyo Institute of Technology, Japan

3.2 *Applications of Scaling to Problems in High-Field Electronic Transport*
– K. K. Thornber, Bell Laboratories, Murray Hill, NJ

3.3 *High-Field Drift Velocity of Electrons in Silicon Inversion Layers as Determined by a Time-of-Flight Technique*
– J. A. Cooper, Jr., and D. F. Nelson, Bell Laboratories, Murray Hill, NJ

3.4 *Electron Mobility in N-Channel Depletion Type MOS Transistors*
– Y. Ohno and Y. Okuto, Nippon Electric Company, Japan

3.5 *Limits of Applicability of the Depletion Approximation and its Recent Augmentation*
– D. J. Bartelink, Xerox Palo Alto Research Center, Palo Alto, CA

SESSION IV: EFFECTS OF PROCESS TECHNOLOGY

3:00 PM – Friday, 5 December 1980

Chairmen: Jim Clemens, Bell Laboratories, Allentown, NJ; and Yuji Okuto, Nippon Electric Company, Japan

4.1 *Enhanced Diffusion in the Single Crystal Silicon Substrate During the Oxidation of a Deposited Polysilicon Doping Source*
– B. Swaminakan, L. Mei, A. M. Lin, and R. W. Dutton, Stanford Electronics Laboratories, Stanford, CA

4.2 *Growth Kinetics and Charge Properties of Thin Thermally Grown SiO_2 Layers on Silicon*
– H. Z. Massoud, C. P. Ho and J. D. Plummer, Stanford Integrated Circuits Laboratories, Stanford, CA

4.3 *Reduction of Electron Trapping in Oxides*
– S. K. Lai, D. R. Young, and J. A. Clalise, IBM T. J. Watson Research Center, Yorktown Heights, NY

4.4 *AlGaAs/GaAs JFET with Gate Junction Near the Growth Interface*
– T. J. Maloney and R. R. Saxena, Varian Associates, Palo Alto, CA

SESSION V: EFFECTS OF BEAM PROCESSING (SPECIAL DISCUSSION SESSION)

8:45 AM – Saturday, 6 December 1980

Chairmen: Dirk Bartelink, Xerox Palo Alto Research Center, Palo Alto, CA; and Jim Mayer, Cornell University, Ithaca, NY

5.1 *Overview of Recent Work*
– Jim Mayer

5.2 *Processing of 1μ Minimum Feature MOS Devices with Xray Lithography*
– H. J. Levinstein, Bell Laboratories, Murray Hill, NJ

5.3 *Some Implications of Beam Processing on Devices*
– Dirk Bartelink