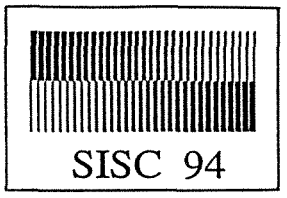

25th IEEE SISC 94

San Diego, California **Dec 8-10, 1994**

ABSTRACTS

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Technical Chair: **W. L. Warren**

Arrangements Chair: **R. E. Stahlbush**

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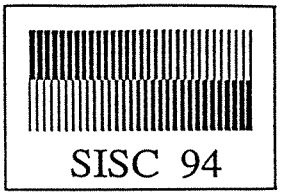

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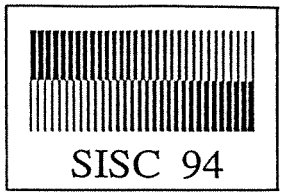

25th IEEE SISC 94

ELECTRON DEVICES SOCIETY

IEEE

San Diego, California

Dec 8-10, 1994

SESSION 1: Breakdown/Reliability

Thursday 12/8/94, 8:15 am - 10:20 am
Session Chair: Hisham Massoud, Duke University
Session Chair: Guido Groeseneken, IMEC

8:15 am Opening Remarks

8:30 am 1.1 **"An Engineering Model of VLSI Gate Oxide Breakdown,"** Chenming Hu, University of California, Berkeley, Berkeley, CA, USA (Invited)

9:05 am 1.2 **"Defect Production, Degradation, and Breakdown of Silicon Dioxide Films,"** D. J. DiMaria, IBM Watson Research Center, Yorktown Heights, NY, USA (Invited)

9:40 am 1.3 **"Determining the Causes of Oxide Breakdown,"** C. Felsch and E. Rosenbaum, University of Illinois at Urbana-Champaign, Urbana, IL, USA

10:00 am 1.4 **"A Two Dimensional Analysis of a Correlation Between the Interface Nano-roughness and Electric Current Capabilities in LPCVD Oxides Deposited on Polycrystalline Silicon,"** J.H. Klootwijk, C. Cobianu, V. Petrescu, H. van Kranenburg, P.J. Woerlee, and H. Wallinga, University of Twente, Enschede, The Netherlands

SESSION 2: Oxide Traps/Interface Traps

Thursday 12/8/94, 10:45 am - 12:00 pm

Session Chair: Max Schulz, Erlangen University
Session Chair: Beall Fowler, Lehigh University

10:45 pm 2.1 **"MOSFET Based Sensors for Molecular Hydrogen at Ambient Temperatures Using Palladium Alloy Gates,"** Robert C. Hughes, Sandia National Laboratories, Albuquerque, NM, USA (Invited)

11:20 pm 2.2 **"H-Bonds at Si/SiO_2 Interfaces-Their Role in a Novel Mechanism for Defect Generation, Defect Metastability and Defect Removal by Rapid Thermal Annealing,"** G. Lucovsky, Z. Jing, and J.L. Whitten, North Carolina State University, Raleigh, NC, USA

11:40 pm 2.3 **"Hydrogen Related SiO_2 Hole Traps with Small Cross Section,"** J.M.M. de Nijs, V.V. Afanas'ev, and P. Balk, DIMES, Delft, The Netherlands

POSTERS P1.1 - P4.3, Oral Summary

Thursday 12/8/94 12:00 pm - 12:30 pm
Session Chair: Mats Andersson, Chalmers University of Technology
Session Chair: Nelson Saks, Naval Research Laboratory

12:00 pm P1.1 **"High Field Related Wearout and Breakdown in Thin Silicon Oxide,"** D.J. Dumin, J.R. Maddux, R. Subramoniam, R.S. Scott, S. Vanchinathan, N.A. Dumin, K.J. Dickerson, and S. Mopuri, Clemson University, Clemson, SC, USA

12:03 pm P1.2 **"Effects of Reliability Screens on MOS Charge Trapping,"** M.R. Shaneyfelt, D.M. Fleetwood, J.R. Schwank, T.L. Meisenheimer, and P.S. Winokur, Sandia National Laboratories, Albuquerque, NM, USA

12:06 pm P1.3 **"Polarity Dependence of Dielectric Breakdown and its Impact on Oxide Scaling,"** L.K. Han, M. Bhat, D. Wristers, D.L. Kwong, and J. Fulford, The University of Texas, Austin, TX, USA

12:09 pm P1.4 **"Trap Generation in n-MOSFETs During Substrate Hot Electron Injection,"** M.J. Kivi and S. Taylor, Liverpool University, Liverpool, UK, and S.P. Zhao, National University of Singapore, Chai Chee Ind. Park, Singapore

12:12 pm P1.5 **"Enhanced n-MOSFET Hot Carrier Degradation Due to Cl-Rich Plasma Poly Etching,"** Xiao-Yu Li, Tomasz Brozek, and C.R. Viswanathan, University of California, Los Angeles, CA, USA, and Y.D. Chan, SEMATECH, Austin, TX, USA

12:15 pm P2.1 **"Effects of the Oxide-Charge Distribution Profile on Carrier Mobility in Silicon Inversion Layers,"** F. Gamiz, and J.A. Lopez-Villanueva, Universidad de Granada, Granada, Spain

12:18 pm P3.1 **"Electron Spin Resonance Detection of a New Hole Trapping Center in Thermally Grown SiO_2 on Si,"** J.F. Conley, Jr. and P.M. Lenahan, Pennsylvania State University University Park, PA, USA, and H.L. Evans and R.K. Lowry, Harris Semiconductor, Melbourne, FL, USA, and T.J. Morthorst, Harris Semiconductor, Findlay, OH, USA.

12:21 pm P4.1 **"Characterization of Two Types of Radiation-Induced Trapped Positive Charge,"** R.K. Freitag, D.B. Brown, and C.M. Dozier, Naval Research Laboratory, Washington, D.C., USA

12:24 pm P4.2 **"Time Dependence of Reversible Hole Traps,"** A.J. Lelis and T.R. Oldham, Army Research Laboratory, Adelphi, MD, USA

12:27 pm P4.3 **"Decay of Anomalous Positive Charge by Repeated Charging and Discharging,"** S. Panchapakesan and L. Trombetta, University of Houston, Houston, TX, USA

SESSION 3: Oxide Traps/Interface Traps Cont.

Thursday 12/8/94, 2:00 pm - 3:20 pm
Session Chair: Ed Nicollian, Univ. North Carolina-Charlotte
Session Chair: Ed Poindexter, Army Research Laboratory

2:00 pm 3.1 **"Dissociation Kinetics of Hydrogen-Passivated (100) Si/SiO_2 Interface Defects,"** Jim Stathis, IBM Watson Research Center, Yorktown Heights, NY, USA

2:20 pm 3.2 **"Electron Spin Resonance Analysis of the Passivation of P_{bo} and P_{b1} Defects at the (100) Si/SiO_2 Interface in Molecular Hydrogen,"** A. Stesmans, Universiteit Leuven,

Leuven, Belgium

2:40 pm 3.3 **"On the Nature of Annealing Induced Interfacial and Bulk Oxide Degradation in Si/SiO_2/Si Structures,"** R.A.B. Devine, CNET-France Telecom, Meylan, France, and W.L. Warren and D.M. Fleetwood, Sandia National Laboratories, Albuquerque, NM, USA.

3:00 pm 3.4 **"Density and Energy of Oxide-Trap Charge due to High-Field Stress,"** D.M. Fleetwood, Sandia National Laboratories, Albuquerque, NM, USA, and N.S. Saks, Naval Research Laboratory, Washington, D.C., USA

SESSION 4: Border Traps/APC

Thursday 12/8/94, 3:45 - 5:05
Session Chair: Dan Fleetwood, Sandia National Laboratories
Session Chair: Jim Stathis, IBM Watson Research Center

3:45 pm 4.1 **"Detection and Characterization of Border Traps in MOSFET's Using 3-Level Charge Pumping Technique,"** J.-L. Autran, B. Balland, and D. Babot, Institut National des Sciences Appliquees de Lyon, Villeurbanne, France

4:05 pm 4.2 **"A Low Frequency C-V Model to Characterize Interface and Near-Interface Oxide Traps in Thin Gate CMOS Devices,"** N.L. Cohen, M.G. Martin, R.E. Paulsen, and M.H. White, Lehigh University, Bethlehem, PA, USA

4:25 pm 4.3 **"Identity of Border Traps in SiO_2 Films,"** W.L. Warren, D.M. Fleetwood, M.R. Shaneyfelt, J.R. Schwank, and P.S. Winokur, Sandia National Laboratories, Albuquerque, NM, USA, and R.A.B. Devine, CNET-France Telecom, Meylan, France

4:45 pm 4.4 **"Evidence for Two Types of Slow States in Stressed Si-SiO_2 Systems,"** K.G. Druijf, J.M.M. de Nijs, E.v.d. Drift, E.H.A. Granneman, and P. Balk, DIMES, Delft, The Netherlands.

POSTERS P5.1 - P8.3, Oral Summary

Thursday 12/8/94, 5:05 - 5:45
Session Chair: T.-P. Ma, Yale University
Session Chair: Hsing-Huang Tseng, Motorola

5:05 pm P5.1 **"Novel Interpretation of XPS Measurements of Nitrided Silicon Oxide,"** D. Bouvet, J. Almeida, C. Coluzza, G. Margaritondo, P. Letourneau, and M. Dutoit, Swiss Federal Institute of Technology, Lausanne, Switzerland, and F. Pio, SGS-Thomson Microelectronics, Agrate Brianza, Italy.

5:08 pm P5.2 **"Fowler-Nordheim Injection in Plasma-Enhanced Chemical Vapor Deposited Silicon Dioxide Films with Nitrided Interface,"** D. Landheer, Y. Tao, D.-X. Xu, and G.I. Sproule, National Research Council of Canada, Ottawa, Canada

5:12 pm P5.3 **"Improvement of Sub-5nm Gate Oxides by Post-Oxidation Annealing in Nitric Oxide Ambient,"** Z.-Q. Yao, H.B. Harrison, and S. Dimitrijev, Griffith University, Nathan, Australia, and Y.T. Yeow, The University of Queensland, St. Lucia, Australia

5:15 pm P6:1 **"Effect of Surface Treatments on Electrical Properties of Deposited and Thermal Oxides,"** V. Misra, W.K. Henson, P.K. McLarty, J.R. Hauser, and J.J. Wortman, North Carolina State University, Raleigh, NC, USA

5:18 pm P6.2 **"Study of Stress-Induced Leakage Current in Ultra-Thin SiO_2,"** L.K. Han, H.H. Wang, J. Yan, M. Bhat, and D.L. Kwong, The University of Texas at Austin, Austin, TX, USA

5:21 pm P6.3 **"The Effects of Post-Annealing Treatments on Confinement Phenomena in SIMOX Structures,"** V.V. Afanasev, DIMES, Delft, The Netherlands, A.G. Revesz, Revesz Associates, Bethesda, MD, and H.L. Hughes, Naval Research Laboratory, Washington, D.C., USA

5:24 pm P6.4 **"Silicon Surface Passivation Control of High Temperature Photoluminescence in $Si/Si_{1-x}Ge_x/Si$ Quantum Wells,"** A. St. Amour and J.C. Sturm, Princeton University Princeton, NJ, USA, and Y. Lacroix and M.L.W. Thewalt, Simon Fraser University, Burnaby, Canada

5:27 pm P6.5 **"Thermal and Electrical Instabilities in Wafer Bonded SiO_2 Layers,"** Per Ericsson and Stefan Bengtsson, Chalmers University of Technology, Goteborg, Sweden

5:30 pm P6.6 **"Determination of Oxide Field Charge at the Top and Bottom Si/SiO_2 Interfaces of Silicon-on-Insulator Devices,"** Emil Arnold, Philips Laboratories, Briarcliff Manor, NY, USA

5:33 pm P6.7 **"Field Emission Schottky MOSFET,"** John Snyder and C.R. Helms, Stanford University, Stanford, CA, USA, and Yoshio Nishi, Hewlett Packard ULSI Research Laboratory, Palo Alto, CA, USA

5:36 pm P6.8 **"Contamination of the Silicon Surface and Oxidation Ambient and its Effects on Gate Oxide Integrity of Rapid Thermal Oxides,"** G.A. Hames, S.E. Beck, W.A. Lanford, J. Barnak, R.J. Nemanich, D.A. Bohling, and J.J. Wortman, North Carolina State University, Raleigh, NC, USA

5:39 pm P8.1 **"Observation of Two Types of Interface Traps in Thin Film Transistors Using Charge Pumping Technique,"** A. Balasinski, R. Sundaresan, F. Bryant, R. Hodges, K.W. Huang, J. Worley, and F.T. Liou, SGS-Thomson Microelectronics, Carrollton, TX, USA

5:42 pm P8.2 **"Impact of Device Scaling on the 1/f Drain Current Noise in MOSFET's,"** Ming-Horn Tsai, and T.-P. Ma, Yale University, New Haven, CT, USA

5:45 pm P8.3 **"A Physical Model of Two-Dimensionally Distributed Hot Electron Injection in Deep Submicron MOSFET's,"** Fumio Ootsuka, Y. Nonaka, K. Ichinose, and Shin'ichiro Matani, Hitachi Ltd., Tokyo, Japan.

SESSION 5: Nitrogen Containing Oxides

Friday 12/9/94, 8:15 am - 10:10 am

Session Chair: Lalita Manchanda, AT&T Bell Laboratories

Session Chair: Mizuho Morita, Tohoku University

8:15 am 5.1 **"Oxynitride Dielectrics Grown in N_2O and NO,"** Yoshio Okada and Phillip J. Tobin, Motorola, Austin TX, USA (Invited)

8:50 am 5.2 **"Removal of Nitrogen from N_2O Oxide by Rapid Thermal Oxidation in N_2O,"** E.C. Carr and R.A. Buhrman, Cornell University, Ithaca, NY, USA

9:10 am 5.3 **"Nitrogen Incorporation during SiO_2 Growth in N_2O,"** N.S. Saks and D.I. Ma, Naval Research Laboratory, Washington, DC, USA

9:30 am 5.4 **"Thickness Dependence of Boron Penetration Through Thin SiO_2 and Oxynitride Gate Dielectrics,"** K.S. Krisch, L. Manchanda, M.L. Green, L.C. Feldman, F.H. Baumann, and D. Brasen, AT&T Bell Laboratories, Murray Hill, NJ, USA, and J. Lai, Massachusetts Institute of Technology, Cambridge, MA, USA

9:50 am 5.5 **"Suppression of Boron Penetration in NO-Nitrided SiO_2,"** L.K. Han, G.W. Yoon, J. Yan, M. Bhat, and D.L. Kwong, The University of Texas at Austin, Austin, TX, USA

SESSION 6: Ultra-Thin Oxides/Advanced Technologies

Friday 12/9/94, 10:40 am - 12:15 pm
Session Chair: Ed Boesch, Jr., Army Research Laboratory
Session Chair: Akihiko Ishitani, NEC Corporation

10:40 am 6.1 **"Measurement and Modeling of Several PMOSFET Hot-Carrier Degradation Mechanisms,"** Reinout Woltjer, Philips Research Laboratories, Eindhoven, The Netherlands (Invited)

11:15 am 6.2 **"N_2O Oxynitride/CVD TEOS Stacked Gate Dielectric for Submicron Technology,"** Hsing-Huang Tseng, P.J. Tobin, C. Ramiah, and J.W. Miller, Motorola, Austin, TX, USA

11:35 am 6.3 **"Bias-Enhanced Interface State Passivation in Ultra-Thin Silicon Oxides,"** M.O. Andersson and Per Lundgren, Chalmers University of Technology, Goteborg, Sweden, and Anders Lundgren, ABB Hafo AB, Jarfalla, Sweden.

11:55 am 6.4 **"Silicon Nitride Thin Films Made by Jet Vapor Deposition,"** Xiewen Wang and T.-P. Ma, Yale University, New Haven, CT, USA

PANEL SESSION 7
Characterization and Growth of Ultra-Thin Oxides

Friday 2:00 pm - 4:00 pm
Panel Organizer and Moderator: Peter S. Winokur, Sandia National Laboratories

The invited panel members will discuss the latest measurement techniques for the characterization and growth of ultra-thin dielectrics in light of the National Technology Roadmap. The panel will discuss issues such as: an overview of the roadmap and its vision for the gate oxide of the future; required impurity levels, if they are achievable, and if they matter for device performance; the cost and feasibility of implementing the roadmap from a gas supplier and equipment perspective; various characterization tools, and alternative dielectrics to SiO_2. A preliminary list of speakers include:

C. Robert Helms, Stanford University, Stanford, CA, USA
Ralph Richardson, Air Products, Allentown, PA, USA
Frank Robertson, SEMATECH, Austin, TX, USA
Peter S. Winokur, Sandia National Laboratories, Albuquerque, NM, USA
Jimmie J. Wortman, North Carolina State University, Raleigh, NC, USA

SESSION 8: Interface Characterization

Saturday 12/10/94, 8:15 am - 10:10 am
Session Chair: Doug Buchanan, IBM Watson Research Center
Session Chair: Rod Devine, France Telecom/CNET

8:15 am 8.1 **"Cluster Analogs for Si/SiO_2 Interfaces and Their Structural Implications,"** F.R. McFeely, IBM Watson Research Center, Yorktown Heights, NY, USA (Invited)

8:50 am 8.2 **"Orientation Dependent Changes in Si/SiO_2 Interface Structures with Progress of Thermal Oxidation,"** T. Hattori, T. Aiba, K. Ohishi, H. Nohira, Y. Shimizu, and K. Yamauchi, Musashi Institute of Technology, Tokyo, Japan, and N. Tate and M. Katayama, Shin-Etsu Handotai Co. Ltd., Japan

9:10 am 8.3 **"A Study of Tunneling Current Oscillation Dependence on SiO_2 Thickness and Si Roughness at the Si/SiO_2 Interface,"** S. Zafar, Q. Liu, and E.A. Irene, University of North Carolina at Chapel Hill, Chapel Hill, NC, USA

9:30 am 8.4 **"Si/SiO_2 Interface Roughness Measured with X-ray Diffraction,"** K.W. Evans-Lutterodt, M.-T. Tang, M.L. Green, D. Brasen, K. Krisch, L. Manchanda, G.S. Higashi, and T. Boone, AT&T Bell Laboratories, Murray Hill, NJ, USA

9:50 am 8.5 **"Microroughness Characterization Using 2D Fourier Transform of AFM Images,"** Mats Bergh, M.O. Andersson, and Stefan Bengtsson, Chalmers University of Technology, Goteborg, Sweden

SESSION 9: Interface Characterization Cont.

Saturday 12/10/94, 10:40 am - 12:15 pm
Session Chair: Bill Lynch, Semiconductor Research Corporation
Session Chair: Bob Stahlbush, Naval Research Laboratory

10:40 am 9.1 **"*In-situ* TEM Study of Silicon Oxidation,"** J.M. Gibson, University of Illinois at Urbana-Champaign, Urbana, IL, USA (Invited)

11:15 am 9.2 **"Second Harmonic Generation from SiO_2/Si Interfaces,"** Hiroyuki Hirayama, Fuminori Ito, and Kohji Watanabe, NEC Corporation, Tsukuba, Japan

11:35 am 9.3 **"Channel Length Dependence of Random Telegraph Signal in MOSFET's,"** Ming-Horn Tsai and T.-P. Ma, Yale University, New Haven, CT, USA, and Terence Hook, IBM Corporation, Essex Junction, VT, USA

11:55 am 9.4 **"Conductance Modulations Induced by Single Electron Switching in Sub-Micron MOS Inversion Channels,"** H.H. Mueller and M.J. Schulz, University of Erlangen-Nurnberg, Erlangen, Germany