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34th IEEE Semiconductor Interface Specialists Conference

December 4-6, 2003
The Key Bridge Marriott, Washington, DC

ABSTRACTS

General Chair: Bob Wallace

Technical Chair: Carl-Mikael Zetterling

Arrangements Chair: Eric Vogel

Past Conference Chair: Lori Lipkin

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December 4-6, 2003
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SISC Ed Nicollian Award for Best Student Paper

In 1995 the SISC began presenting an award to the best student presentation of the SISC in honor of Professor E. H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental to establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology," published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author of either an oral or poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque and an honorarium sent to the winner after the Conference. To honor the winner, the award is announced at the conference taking place the following year.

The *2002 SISC Ed Nicollian Award for Best Student Paper* was given to **Wenjuan Zhu** of Yale University. The paper was entitled "Mobility extraction for MOSFET's made with ultra-thin high-k dielectrics: correct accounting of channel carriers." Co-authors are T.P. Ma, T. Tamagawa and W.Y. Wang

Those eligible and wishing to be considered for the 2003 SISC Ed Nicollian Award for Best Student Paper should contact the 2003 IEEE SISC Technical Chair immediately.

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This meeting is sponsored by the IEEE Electron Device Society.

The SISC also acknowledges support from the National Science Foundation.

Conference Agenda Overview

Wednesday, December 3, 2002

Registration:	18:00-21:00

Hospitality Suite: 20:00-23:00

Thursday, December 4, 2002

Registration:	08:00-17:00
Session 1 – High-K Integration:	08:00-09:25
Poster Session I – High-K Dielectrics:	09:25-09:45
Session 2 – Ferroelectrics and Oxynitrides:	10:15-11:35
Poster Session II – Non-silicon Interfaces:	11:35-11:55
Session 3 – Theory and Calculations:	13:30-14:50
Poster Session III – Theory and Reliability:	14:50-15:10
Session 4 – Interface Characterization:	15:40-17:20
Poster Session IV – Characterization and Late News:	17:20-17:45

Poster Reception: 19:00 (7 PM)
Hospitality Suite: 21:00-23:00

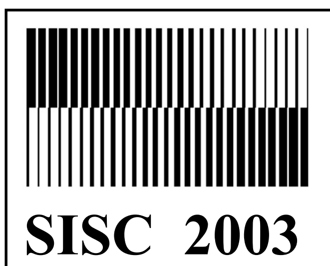
Friday, December 5, 2002

Registration:	08:00-17:00
Session 5 – High-K Processing:	08:00-09:40
Session 6 – Non-silicon Interfaces:	10:10-12:00
Optional Rump Sessions “High-K dielectrics” and “Non-silicon Interfaces”:	15:00

SISC Banquet and Limerick Contest: 19:00 (7 PM)
Hospitality Suite: 21:00-23:00

Saturday, December 6, 2002

Session 7 – Reliability:	08:00-09:40
Session 8 –High-K Characterization:	10:10-12:00



34th IEEE Semiconductor Interface Specialists Conference

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Advance Technical Program with late news

Thursday, December 4th, 2003

Session 1 - High-K Integration

8:00 AM Opening remarks

8:10 AM **S1.1 *Invited* Challenges for Dual Metal Gate Electrodes on HfO_2 Gate Dielectrics**
Jamie Schaeffer, *Motorola, USA*

8:45 AM **S1.2 Mixtures of HfO_2 and TiO_2 as High-k Gate Dielectrics**
F. Chen, B. Xia, C. Hella, X. Shi, W. L. Gladfelter, and S. A. Campbell, *University of Minnesota*

9:05 AM **S1.3 Hole trapping in mixed Al-Hf oxides on Si**
V. V. Afanas'ev and A. Stesmans, *Department of Physics, KU Leuven, Belgium*

Poster Session I: High-K Dielectrics

9:25 AM **P1 Chemical Structures of HfO_2/Si Interfacial Transition Layer**
T.Hattori[1],H.Nohira[1],M.B.Seman[1],Y.Takata[2], K.Kobayashi[3],S.Joumori[4],K.Nakajima[4], M.Suzuki[4],K.Kimura[4],Y.Sugita[5],O.Nakatsuka[6], A.Sakai[6],S.Zaima[6],T.Ishikawa[2] and S.Shin[2],
[1]Musashi Insutitute of Technology, Tokyo, [2]RIKEN/Spring-8, Hyogo, [3]JASRI/Spring-8, Hyogo, [4]Kyoto University, Kyoto, [5]Fujitsu Ltd., Tokyo, [6]Nagoya University, Nagoya, Japan

9:28 AM **P2 Improved Interface Properties of MOS Device with Gate Hafnium Oxynitride by Chemical Dry Cleaning**
Chin-Lung Cheng, Kuei-Shu Chang-Liao, and Tien-Ko Wang, *National Tsing Hua University, Hsinchu, Taiwan, R. O. C.*

9:31 AM **P3 Influence of surface treatment prior to ALD high-k dielectrics on the performance of SiGe surface-channel pMOSFETs**
D. Wu, P.-E. Hellström, H. Radamson, S.-L. Zhang and M. Östling, *KTH, Royal Institute of Technology, Sweden*;
E. Vainonen-Ahlgren, E. Tois, M. Tuominen, *ASM Microchemistry Ltd., Finland*

9:34 AM **P4 The Deposition of HfO_2 from Hf t-butoxide and Nitric Oxide**
Z. Zhang and S. A. Campbell, *University of Minnesota*

9:37 AM **P5 Epitaxial $SrTiO_3$ Films on Silicon: Profiling with Medium Energy Ion Scattering**
D.G. Starodub, L.V. Goncharova, E. Garfunkel, T. Gustafsson, *Rutgers University*, and D.G. Schlom, *Penn State University*

9:40 AM **P6 $HfSiO_4$ atomic layer deposition analysis by Mass Spectroscopy and XPS**
Moo-Sung Kim, Steven A. Rogers, Yun-Seok Kim[1], Jong-Ho Lee[1] and Ho-Kyu Kang[1],
Air Products and Chemicals Korea, Korea, [1]Samsung Electronics Co., Korea

9:43 AM COFFEE BREAK

Session 2 - Ferroelectrics and Oxynitrides

10:15 AM Opening remarks

10:20 AM **S2.1 *Invited* Integration of novel functional oxides with Si**
Alex Grishin, *KTH, Royal Institute of Technology, Sweden*

10:55 AM **S2.2 Impact of the Oxide Scaling on the SONOS Cell Endurance and Retention**
S. S. Chung, P. -Y. Chiang, George Chou*, C. T. Huang*, Paul Chen*,
National Chiao Tung University,Taiwan
**eMemory, Science-based Industrial Park, Hsinchu, Taiwan*

11:15 AM **S2.3 Monitoring Nitrogen Penetration into Silicon Channels for Si-Oxynitride-Gate MOSFETs using Electrical Parameters**
Khaled Ahmed, Philip Kraus, Chris Olsen, Jason Campbell, and Faran Nouri, *Applied Materials Inc.*

Poster Session II: Non-silicon Interfaces

11:35 AM **P7 Optical and electrical properties of amorphous $Gd_{(x)}Ga_{(0.4-x)}O_{(0.6)}$ films in $Gd_{(x)}Ga_{(0.4-x)}O_{(0.6)}/Ga_2O_3$ gate dielectric stacks on GaAs**
S. Zollner, R. Gregory, N. Medendorp, and M. Passlack, *Motorola, Inc., Semiconductor Products Sector, Tempe, AZ,*
D. Braddock*, Osemi Inc., Rochester, MN*

11:38 AM **P8 Current conduction processes in high-k GdGaO/GaO gate dielectric stacks on GaAs**
A. Chen, *Yale University*,
M. Passlack and N. Medendorp, *Motorola Inc*.,
D. Braddock*, Osemi Inc.*

11:41 AM **P9 Reductions in Interface Defects, D_{it}, by Post Oxidation Plasma-Assisted Nitridation of $GaN-SiO_2$ Interfaces in MOS Devices**
C. Bae and G. Lucovsky, *NC State Univ.*

11:44 AM **P10 Gate oxides formed in N_2O on 4H-SiC**
H.Ö. Olafsson, G.I. Gudjonsson,
E.Ö. Sveinbjornsson, *Chalmers University of Technology, Goteborg, Sweden*

11:47 AM **P11 Characteristics of PZT/Al_2O_3 stack on SiC demonstrated in a NVFET**
S.-M. Koo*, S. I. Khartsev, C.-M. Zetterling, A. M. Grishin, and M. Östling, *KTH, Royal Institute of Technology, Sweden*

11:50 AM **P12 Nanometer-scale measurements and modeling of electronic properties of stacking fault defects in SiC near metal/semiconductor interfaces**
Yi Ding, Kibog Park, Jonathan P. Pelz,
The Ohio State University,
K. C. Palle, M. K. Mikhov, B. J. Skromme, H. Meidia, S. Mahajan, *Arizona State University*,
A. V. Los, and M. S. Mazzola, *Mississippi State University*

11:53 AM Adjourn for LUNCH on your own

Session 3 - Theory and Calculations

1:30 PM Opening remarks

1:35 PM **S3.1 *Invited* First-principles calculations of the formation of the $SrTiO_3/Si$ interfaces**
Peter E. Bloechl, *Clausthal University of Technology, Germany*

2:10 PM **S3.2 A New Approach to Gate Stack Integrity Including the Role of Strain Relief in Suboxide Transition Regions**
G. Lucovsky, *NC State Univ.* and J.C. Phillips, *Rutgers Univ.*

2:30 PM **S3.3 Multilayer Metallic Gate Electrode for Depletion Suppression and Tunable Workfunction**
Steven C.H. Hung*, Judy L. Hoyt**,
James F. Gibbons, Ching-Huang Lu, Mike Deal, Yoshio Nishi, *Stanford University, *Applied Materials, **MIT*

How do I win the SISC Limerick Contest?

In order to win the Limerick contest at the SISC, your Limerick should reflect some (very funny) aspects related to the conference, its papers, or its attendees - especially the “good old chaps” of the conference. It can also have some very innovative and funny personal touch or jokes about science in general and semiconductor (interfaces) in particular. As an example, here was a finalist entry in the 2000 contest, which reflected on the evolution of a "rump session" that was held and peppered with remarks from several “good old chaps”…

We all enjoyed the rump session
and heard reliability tension
opinions flew 'round
the session broke down
The cause? Hot comment Injection

More examples will be shown in the session breaks. Don’t hesitate to ask if you have any questions. I’m looking forward to an entertaining Limerick contest!

Len Trombetta, University of Houston
Limerick Chair SISC 2003

Poster Session III: Theory and Reliability

2:50 PM **P13 Separate and Independent Control of Interfacial Band Alignments and Dielectric Constants in Transition Metal(Tm)-Rare Earth (Re) Complex Oxides**
G. Lucovsky, Yu Zhang, J.L. Whitten, *NC State Univ*., D.G. Schlom, *Penn State Univ*. and J.L. Freeouf, *Oregon Graduate Inst.*

2:53 PM **P14 A Novel Approach for Determination of Tunneling Mass, m_{eff} - Conduction Band Offset Energy, E_B, Products for Advanced Gate Dielectrics**
C.L. Hinkle, C. Fulton, R.J. Nemanich and G. Lucovsky, *NC State Univ*.

2:56 PM **P15 Electrical Characterization of Molecular Monolayers Formed by Direct Attachment to Si**
Curt A. Richter, Christina A. Hacker, and Lee J. Richter, *National Institute of Standards and Technology*

2:59 PM **P16 Soft gate oxide breakdown as a lifetime-limiting event in dynamic CMOS logic**
B. Kaczer, G. Groeseneken, *IMEC, Belgium*

3:02 PM **P17 Effect of Scaling on the Reliability of Flash EEPROMs under CHISEL Programming**
Deleep R. Nair, Nihar R. Mohapatra, S. Mahapatra, S. Shukuri* and J. Bude**, *Indian Institute of Technology, Bombay, India, *Hitachi Ltd., Tokyo, Japan, **Agere Systems, PA*

3:05 PM **P18 Simulation of Interface Roughness in DG-MOSFETs using Non-Equilibrium Green's Functions**
J Fonseca and S Kaya, *Ohio University*

3:08 PM	**COFFEE BREAK**

Session 4 - Interface Characterization

3:40 PM Opening remarks

3:45 PM **S4.1 *Invited* Creation mechanism of interface defects at the early stage of Si oxidation processes studied by UHV-ESR**
Satoshi Yamasaki, *Advanced Semiconductor Research Center (AIST), Japan*

4:20 PM **S4.2 Direct Evidence for the Origin of the H/D Isotope Effect of Hot-Electron Degradation of MOS Devices**
Zhi Chen, Jun Guo, and Pangleen Ong, *University of Kentucky*

4:40 PM **S4.3 Different types of positive charges generated near the oxide/Si interface**
C.Z.Zhao, J.F.Zhang, G.Groeseneken*, and R.Degraeve*, *Liverpool John Moores University, UK, *IMEC, Belgium*

5:00 PM **S4.4 Evolution of inherent density of Pb-type interface defects in (100)Si/SiO_2 structures as a function of oxidation and annealing temperature**
A. Stesmans and D. Pierreux, *University of Leuven, Belgium*

Poster Session IV: Characterization and Late News

5:20 PM **P19 Characterization of High-Field Stress-Induced Border Traps in JVD Si_3N_4 Transistors by Drain urrent Transient and 1/f Methods**
K.N.ManjulaRani,V.Ramgopal Rao and J.Vasi, *I.I.T. Bombay, India*

5:23 PM **P20 A new method to extract EOT of ultra-thin gate dielectric and its associated C-V curve**
Zhijiong Luo and T. P. Ma, *Yale University*

5:26 PM **P21 Direct Lateral Profiling of Channel-Hot-Carrier Induced Negative Oxide Charge and Interface Traps in nMOSFET's**
Chun-Yuan Lu, Chung-Min Lin, Chun-Yuan Lo, and Kuei-Shu Chang-Liao, *National Tsing Hua University, Hsinchu, TAIWAN, R. O. C.*

5:29 PM **P22 (Late News) Generalized Weibull Distribution for Improved Dielectric Reliability Assessment**
U. M. S. Costa1, V. N. Freire1, L. C. Malacarne2, R. S. Mendes2, S. Picoli Jr.2, E. F. da Silva Jr.3, E. A. de Vasconcelos3
1Universidade Federal do Ceará, Brazil
2Universidade Estadual de Maringá, Brazil
3Universidade Federal de Pernambuco, Brazil.

5:32 PM **P23 (Late News) Physical and Electrical Characterization of Ultrathin HfO2 Films Deposited on Ge(100)**
E.P. Gusev, H. Shang, M. Copel, M. Gribelyuk*, C. D'Emic, P. Kozlowski and T. Zabel,
*IBM Research and *Microelectronics, USA*

5:35 PM **P24 (Late News) Effects of high pressure hydrogen and deuterium annealing on HfO_2 gate dielectric**
Hokyung Park, Hyundoek Yang, Hyunjun Sim, Chandan B. Samantaray and Hyunsang Hwang
Kwangju Institute of Science and Technology, Korea

5:38 PM Closing remarks

5:43 PM Adjourn

7:00 PM	**Thursday evening POSTER reception**
9:00 PM	**Hospitality suite**

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Advance Technical Program

Friday, December 5th, 2003

Session 5 - High-K Processing

8:00 AM Opening remarks

8:05 AM **S5.1** ***Invited*** **Recent Developments in Understanding Local Effects and Device Properties of Hf-based High-k Dielectrics**
Glen Wilk,
ASM America, USA

8:40 AM **S5.2 Stability of Metal Oxide Buffer Layers During Reactive Metal Deposition**
M. Copel and M. C. Reuter*, IBM Research Division, TJ Watson Res. Center*

9:00 AM **S5.3 The Effects of Interfacial Layer Thickness and Processing on the Radiation Response of High-k/SiO_xN_y/Si(100) Gate Dielectric Stacks**
J.A. Felix[1], M.R. Shaneyfelt[2], D.M. Fleetwood[1], E. P. Gusev[3], R.D. Schrimpf[1], and C. D´Emic[3],
[1]*Vanderbilt University.*
[2]*Sandia National Laboratories,*
[3]*IBM Thomas J. Watson Research Center*

9:20 AM **S5.4 Threshold Voltage Instability in CMOS High-K Dielectrics: Comparison Between Hafnium and Aluminum Oxide**
S.Cimino[1], L.Pantisano[2], A.Paccagnella[1], and G.Groeseneken[2],
[1]*DEI, Universita' di Padova, Italy,*
[2]*IMEC, Belgium*

9:40 AM COFFEE BREAK

Session 6 - Non-silicon Interfaces

10:10 AM Opening remarks

10:15 AM **S6.1** ***Invited*** **Development and Characterization of Stacked Gate Dielectrics on GaAs**
Matthias Passlack, *Motorola, USA*

10:50 AM **S6.2 Oxygen and Oxide Bonding on GaAs(001)- c(2x8)/(2x4): An Atomic Understanding of Fermi Level Pinning and Unpinning**
M. J. Hale[1], J. Z. Sexton[1], S. I. Yi[1], D. L. Winn[1], M. Passlack[2], and A. C. Kummel[1],
[1]*University of California, San Diego,*
[2]*Motorola Inc.*

11:10 AM **S6.3 Comparison of (1120) and (0001) Surface Orientations in 4H-SiC Inversion Layers**
Gary Pennington, Neil Goldsman, James M. McGarrity, *UMD,*
Aivars Lelis and Charles J. Scozzie, *ARL*

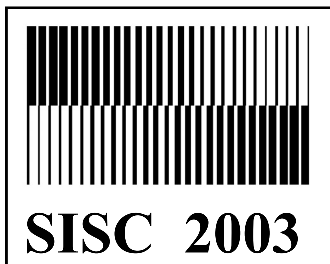
11:30 AM **S6.4 Spin Dependent Recombination of Interface/Near Interface Deep Level Centers in 6H Silicon Carbide MOSFETs**
David J. Meyer, Patrick. M. Lenahan*,*
The Pennsylvania State University,
Aivars Lelis, *U.S. Army Research Laboratory*

11:50 AM Closing remarks

12:00 PM Adjourn

3:00 PM Rump sessions:
1. High-K
2. Non-silicon Interfaces

7:00 PM BANQUET with LIMERICK Contest
9:00 PM Hospitality suite



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Advance Technical Program

Saturday, December 6th, 2003

Session 7 - Reliability

8:00 AM Opening remarks

8:05 AM **S7.1** ***Invited*** **Gate Dielectric Needs for Non-Classical CMOS**
H.-S. Philip Wong,
IBM T.J. Watson Research Center, USA

8:40 AM **S7.2 Model for NBTI in pMOSFETs with Ultrathin Gate Oxide Layers: Comparison Between Electron and Hole Injection**
M. Houssa[1,2], M. Aoulaiche[1], and J.L. Autran[1],
[1]L2MP, UMR CNRS 6137, University of Provence, Marseille, France,
[2]IMEC, Belgium

9:00 AM **S7.3 Which defect breaks down gate oxides?**
W.D.Zhang, J.F.Zhang, C.Z.Zhao, G.Groeseneken*, and R.Degraeve*, *Liverpool John Moores University, UK, *IMEC, Belgium*

9:20 AM **S7.4 Non-invasive nature of corona charging on thermal Si/SiO_2 structures; an electron spin resonance study**
M. Dautrich*, P.M. Lenahan*,
J.F. Conley, Jr.**, A.Y. Kang*,
**Penn State University,*
***Sharp Labs of America*

9:40 AM	**COFFEE BREAK**

Session 8 - High-K Characterization

10:10 AM Opening remarks

10:15 AM **S8.1** ***Invited*** **Suppression of Subcutaneous Oxidation during the Deposition of Amorphous $LaAlO_3$ on Silicon**
Darrell G. Schlom, *Penn State, USA*

10:50 AM **S8.2 Interface Tunneling Mechanism of HfO_2/ Dual Metal Gate Stack with Varying Interface Layer Thickness and Different Bias Polarities**
Y. H. Kim, R. Choi, R. Jha*, J.H. Lee*,
V. Misra* and J. C. Lee,
The University of Texas, Austin,
** North Carolina State University*

11:10 AM **S8.3 Physical structure of trapped electrons in atomic layer deposited hafnium oxide using $Hf(NO_3)_4$ precursor**
Andrew Y. Kang, Patrick. M. Lenahan,
The Pennsylvania State University, John F. Conley and Yoshi Ono, *Sharp Labs of America*

11:30 AM **S8.4 Inelastic Electron Tunneling Spectroscopy Study of Traps in Ultra-thin High-k Gate Dielectrics**
Wei He and T.P. Ma, *Yale University*

11:50 AM Closing remarks

12:00 PM	**End of SISC 2003**

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34th IEEE Semiconductor Interface Specialists Conference

December 4-6, 2003
The Key Bridge Marriott, Washington, DC

Session 1 - High-K Integration

Thursday, December 4, 2003
Session Chair: Bob Wallace

8:00 AM **Opening remarks**

8:10 AM **S1.1** ***Invited*** **Challenges for Dual Metal Gate Electrodes on HfO_2 Gate Dielectrics**
Jamie Schaeffer, *Motorola, USA*

8:45 AM **S1.2 Mixtures of HfO_2 and TiO_2 as High-k Gate Dielectrics**
F. Chen, B. Xia, C. Hella, X. Shi, W. L. Gladfelter, and S. A. Campbell,
University of Minnesota

9:05 AM **S1.3 Hole trapping in mixed Al-Hf oxides on Si**
V. V. Afanas'ev and A. Stesmans,
Department of Physics, KU Leuven, Belgium

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Poster Session I: High-K Dielectrics

Thursday, December 4, 2003
Session Chair: Carl-Mikael Zetterling

9:25 AM **P1 Chemical Structures of HfO_2/Si Interfacial Transition Layer**
T.Hattori[1],H.Nohira[1],M.B.Seman[1],Y.Takata[2],K.Kobayashi[3],S.Joumori[4],K.Nakajima[4], M.Suzuki[4],K.Kimura[4],Y.Sugita[5],O.Nakatsuka[6],A.Sakai[6],S.Zaima[6],T.Ishikawa[2] and S.Shin[2], [1]*Musashi Insutitute of Technology, Tokyo,* [2]*RIKEN/Spring-8, Hyogo,* [3]*JASRI/Spring-8, Hyogo,* [4]*Kyoto University, Kyoto,* [5]*Fujitsu Ltd., Tokyo,* [6]*Nagoya University, Nagoya, Japan*

9:28 AM **P2 Improved Interface Properties of MOS Device with Gate Hafnium Oxynitride by Chemical Dry Cleaning**
Chin-Lung Cheng, Kuei-Shu Chang-Liao, and Tien-Ko Wang,
National Tsing Hua University, Hsinchu, Taiwan, R. O. C.

9:31 AM **P3 Influence of surface treatment prior to ALD high-k dielectrics on the performance of SiGe surface-channel pMOSFETs**
D. Wu, P.-E. Hellström, H. Radamson, S.-L. Zhang and M. Östling,
KTH, Royal Institute of Technology, Sweden;
E. Vainonen-Ahlgren, E. Tois, M. Tuominen,
ASM Microchemistry Ltd., Finland

9:34 AM **P4 The Deposition of HfO_2 from Hf t-butoxide and Nitric Oxide**
Z. Zhang and S. A. Campbell,
University of Minnesota

9:37 AM **P5 Epitaxial $SrTiO_3$ Films on Silicon: Profiling with Medium Energy Ion Scattering**
D.G. Starodub, L.V. Goncharova, E. Garfunkel, T. Gustafsson,
Rutgers University, and D.G. Schlom, *Penn State University*

9:40 AM **P6 $HfSiO_4$ atomic layer deposition analysis by Mass Spectroscopy and XPS**
Moo-Sung Kim, Steven A. Rogers, Yun-Seok Kim[1], Jong-Ho Lee[1] and Ho-Kyu Kang[1], *Air Products and Chemicals Korea, Korea,* [1]*Samsung Electronics Co., Korea*

9:43 AM **COFFEE BREAK**

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Session 2 - Ferroelectrics and Oxynitrides

Thursday, December 4, 2003
Session Chair: Andre Stesmans

10:15 AM **Opening remarks**

10:20 AM **S2.1** ***Invited*** **Integration of novel functional oxides with Si**
Alex Grishin,
KTH, Royal Institute of Technology, Sweden

10:55 AM **S2.2 Impact of the Oxide Scaling on the SONOS Cell Endurance and Retention**
S. S. Chung, P. -Y. Chiang, George Chou*, C. T. Huang*, Paul Chen*,
National Chiao Tung University,Taiwan
**eMemory, Science-based Industrial Park, Hsinchu, Taiwan*

11:15 AM **S2.3 Monitoring Nitrogen Penetration into Silicon Channels for Si-Oxynitride-Gate MOSFETs using Electrical Parameters**
Khaled Ahmed, Philip Kraus, Chris Olsen,
Jason Campbell, and Faran Nouri,
Applied Materials Inc.

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Poster Session II: Non-silicon Interfaces

Thursday, December 4, 2003
Session Chair: Art Edwards

11:35 AM **P7 Optical and electrical properties of amorphous $Gd_{(x)}Ga_{(0.4-x)}O_{(0.6)}$ films in $Gd_{(x)}Ga_{(0.4-x)}O_{(0.6)}/Ga_2O_3$ gate dielectric stacks on GaAs**
S. Zollner, R. Gregory, N. Medendorp, and M. Passlack,
Motorola, Inc., Semiconductor Products Sector, Tempe, AZ,
D. Braddock*, Osemi Inc., Rochester, MN*

11:38 AM **P8 Current conduction processes in high-k GdGaO/GaO gate dielectric stacks on GaAs**
A. Chen, *Yale University*,
M. Passlack and N. Medendorp, *Motorola Inc*.,
D. Braddock*, Osemi Inc.*

11:41 AM **P9 Reductions in Interface Defects, D_{it}, by Post Oxidation Plasma-Assisted Nitridation of GaN-SiO_2 Interfaces in MOS Devices**
C. Bae and G. Lucovsky,
NC State Univ.

11:44 AM **P10 Gate oxides formed in N_2O on 4H-SiC**
H.Ö. Olafsson, G.I. Gudjonsson, E.Ö. Sveinbjornsson,
Chalmers University of Technology, Goteborg, Sweden

11:47 AM **P11 Characteristics of PZT/Al_2O_3 stack on SiC demonstrated in a NVFET**
S.-M. Koo*, S. I. Khartsev, C.-M. Zetterling,
A. M. Grishin, and M. Östling, *KTH, Royal Institute of Technology, Sweden*

11:50 AM **P12 Nanometer-scale measurements and modeling of electronic properties of stacking fault defects in SiC near metal/semiconductor interfaces**
Yi Ding, Kibog Park, Jonathan P. Pelz,
The Ohio State University,
K. C. Palle, M. K. Mikhov, B. J. Skromme, H. Meidia, S. Mahajan,
Arizona State University,
A. V. Los, and M. S. Mazzola,
Mississippi State University

11:53 AM **Adjourn for LUNCH on your own**

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Session 3 - Theory and Calculations

Thursday, December 4, 2003
Session Chair: Bernie Mrstik

1:30 PM **Opening remarks**

1:35 PM **S3.1** ***Invited*** **First-principles calculations of the formation of the $SrTiO_3$/Si interfaces**
Peter E. Bloechl,
Clausthal University of Technology, Germany

2:10 PM **S3.2 A New Approach to Gate Stack Integrity Including the Role of Strain Relief in Suboxide Transition Regions**
G. Lucovsky,
NC State Univ.
and J.C. Phillips,
Rutgers Univ.

2:30 PM **S3.3 Multilayer Metallic Gate Electrode for Depletion Suppression and Tunable Workfunction**
Steven C.H. Hung*, Judy L. Hoyt**, James F. Gibbons, Ching-Huang Lu, Mike Deal, Yoshio Nishi,
*Stanford University, *Applied Materials, **MIT*

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Poster Session III: Theory and Reliability

Thursday, December 4, 2003
Session Chair: Lori Lipkin

2:50 PM **P13 Separate and Independent Control of Interfacial Band Alignments and Dielectric Constants in Transition Metal(Tm)-Rare Earth (Re) Complex Oxides**
G. Lucovsky, Yu Zhang, J.L. Whitten, *NC State Univ.*,
D.G. Schlom, *Penn State Univ.*
and J.L. Freeouf, *Oregon Graduate Inst.*

2:53 PM **P14 A Novel Approach for Determination of Tunneling Mass, m_{eff} -Conduction Band Offset Energy, E_B, Products for Advanced Gate Dielectrics**
C.L. Hinkle, C. Fulton, R.J. Nemanich and G. Lucovsky,
NC State Univ.

2:56 PM **P15 Electrical Characterization of Molecular Monolayers Formed by Direct Attachment to Si**
Curt A. Richter, Christina A. Hacker, and Lee J. Richter,
National Institute of Standards and Technology

2:59 PM **P16 Soft gate oxide breakdown as a lifetime-limiting event in dynamic CMOS logic**
B. Kaczer, G. Groeseneken,
IMEC, Belgium

3:02 PM **P17 Effect of Scaling on the Reliability of Flash EEPROMs under CHISEL Programming**
Deleep R. Nair, Nihar R. Mohapatra, S. Mahapatra, S. Shukuri* and J. Bude**,
*Indian Institute of Technology, Bombay, India, *Hitachi Ltd., Tokyo, Japan, **Agere Systems, PA*

3:05 PM **P18 Simulation of Interface Roughness in DG-MOSFETs using Non-Equilibrium Green's Functions**
J Fonseca and S Kaya,
Ohio University

3:08 PM **COFFEE BREAK**

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Session 4 - Interface Characterization

Thursday, December 4, 2003
Session Chair: Matt Copel

3:40 PM **Opening remarks**

3:45 PM **S4.1** ***Invited*** **Creation mechanism of interface defects at the early stage of Si oxidation processes studied by UHV-ESR**
Satoshi Yamasaki,
Advanced Semiconductor Research Center (AIST), Japan

4:20 PM **S4.2 Direct Evidence for the Origin of the H/D Isotope Effect of Hot-Electron Degradation of MOS Devices**
Zhi Chen, Jun Guo, and Pangleen Ong,
University of Kentucky

4:40 PM **S4.3 Different types of positive charges generated near the oxide/Si interface**
C.Z.Zhao, J.F.Zhang, G.Groeseneken*, and R.Degraeve*,
*Liverpool John Moores University, UK, *IMEC, Belgium*

5:00 PM **S4.4 Evolution of inherent density of Pb-type interface defects in (100)Si/SiO_2 structures as a function of oxidation and annealing temperature**
A. Stesmans and D. Pierreux,
University of Leuven, Belgium

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Poster Session IV: Characterization and Late News

Thursday, December 4, 2003
Session Chair: Eric Vogel

5:20 PM **P19 Characterization of High-Field Stress-Induced Border Traps in JVD Si_3N_4 Transistors by Drain urrent Transient and 1/f Methods**
K.N.ManjulaRani,V.Ramgopal Rao and J.Vasi, *I.I.T. Bombay, India*

5:23 PM **P20 A new method to extract EOT of ultra-thin gate dielectric and its associated C-V curve**
Zhijiong Luo and T. P. Ma, *Yale University*

5:26 PM **P21 Direct Lateral Profiling of Channel-Hot-Carrier Induced Negative Oxide Charge and Interface Traps in nMOSFET's**
Chun-Yuan Lu, Chung-Min Lin, Chun-Yuan Lo, and Kuei-Shu Chang-Liao, *National Tsing Hua University, Hsinchu, TAIWAN, R. O. C.*

5:29 PM **P22 (Late News) Generalized Weibull Distribution for Improved Dielectric Reliability Assessment**
U. M. S. Costa1, V. N. Freire1, L. C. Malacarne2, R. S. Mendes2, S. Picoli Jr.2, E. F. da Silva Jr.3, E. A. de Vasconcelos3
1Universidade Federal do Ceará, Brazil, 2Universidade Estadual de Maringá, Brazil, 3Universidade Federal de Pernambuco, Brazil.

5:32 PM **P23 (Late News) Physical and Electrical Characterization of Ultrathin HfO_2 Films Deposited on Ge(100)**
E.P. Gusev, H. Shang, M. Copel, M. Gribelyuk*, C. D'Emic, P. Kozlowski and T. Zabel, *IBM Research and *Microelectronics, USA*

5:35 PM **P24 (Late News) Effects of high pressure hydrogen and deuterium annealing on HfO2 gate dielectric**
Hokyung Park, Hyundoek Yang, Hyunjun Sim, Chandan B. Samantaray and Hyunsang Hwang, *Kwangju Institute of Science and Technology, Korea*

5:38 PM **Closing remarks**

5:43 PM **Adjourn**

7:00 PM **Thursday evening POSTER reception**

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Session 5 - High-K Processing

Friday, December 5, 2003
Session Chair: Steve Campbell

8:00 AM **Opening remarks**

8:05 AM **S5.1** ***Invited*** **Recent Developments in Understanding Local Effects and Device Properties of Hf-based High-k Dielectrics**
Glen Wilk,
ASM America, USA

8:40 AM **S5.2 Stability of Metal Oxide Buffer Layers During Reactive Metal Deposition**
M. Copel and M. C. Reuter,
IBM Research Division, TJ Watson Res. Center

9:00 AM **S5.3 The Effects of Interfacial Layer Thickness and Processing on the Radiation Response of High-k/SiO_xN_y/Si(100) Gate Dielectric Stacks**
J.A. Felix[1], M.R. Shaneyfelt[2], D.M. Fleetwood[1], E. P. Gusev[3], R.D. Schrimpf[1], and C. D´Emic[3],
[1]*Vanderbilt University.*
[2]*Sandia National Laboratories,*
[3]*IBM Thomas J. Watson Research Center*

9:20 AM **S5.4 Threshold Voltage Instability in CMOS High-K Dielectrics: Comparison Between Hafnium and Aluminum Oxide**
S.Cimino[1], L.Pantisano[2], A.Paccagnella[1], and G.Groeseneken[2],
[1]*DEI, Universita' di Padova, Italy,*
[2]*IMEC, Belgium*

9:40 AM **COFFEE BREAK**

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Session 6 - Non-silicon Interfaces

Friday, December 5, 2003
Session Chair: Sima Dimitrijev

10:10 AM **Opening remarks**

10:15 AM **S6.1** ***Invited*** **Development and Characterization of Stacked Gate Dielectrics on GaAs**
Matthias Passlack,
Motorola, USA

10:50 AM **S6.2 Oxygen and Oxide Bonding on GaAs(001)- c(2x8)/(2x4): An Atomic Understanding of Fermi Level Pinning and Unpinning**
M. J. Hale[1], J. Z. Sexton[1], S. I. Yi[1], D. L. Winn[1], M. Passlack[2], and A. C. Kummel[1],
[1]*University of California, San Diego,*
[2]*Motorola Inc.*

11:10 AM **S6.3 Comparison of (1120) and (0001) Surface Orientations in 4H-SiC Inversion Layers**
Gary Pennington, Neil Goldsman,
James M. McGarrity, *UMD,*
Aivars Lelis and Charles J. Scozzie, *ARL*

11:30 AM **S6.4 Spin Dependent Recombination of Interface/Near Interface Deep Level Centers in 6H Silicon Carbide MOSFETs**
David J. Meyer, Patrick. M. Lenahan,
The Pennsylvania State University,
Aivars Lelis, *U.S. Army Research Laboratory*

11:50 AM **Closing remarks**

12:00 PM **Adjourn**

3:00 PM **Rump sessions:**
1. **High-K**
2. **Non-silicon Interfaces**

7:00 PM **BANQUET with LIMERICK Contest**

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Session 7 - Reliability

Saturday, December 6, 2003
Session Chair: Ben Kaczer

8:00 AM **Opening remarks**

8:05 AM **S7.1 *Invited* Gate Dielectric Needs for Non-Classical CMOS**
H.-S. Philip Wong,
IBM T.J. Watson Research Center, USA

8:40 AM **S7.2 Model for NBTI in pMOSFETs with Ultrathin Gate Oxide Layers: Comparison Between Electron and Hole Injection**
M. Houssa[1,2], M. Aoulaiche[1], and J.L. Autran[1],
[1]L2MP, UMR CNRS 6137, University of Provence, Marseille, France,
[2]IMEC, Belgium

9:00 AM **S7.3 Which defect breaks down gate oxides?**
W.D.Zhang, J.F.Zhang, C.Z.Zhao, G.Groeseneken*, and R.Degraeve*,
*Liverpool John Moores University, UK, *IMEC, Belgium*

9:20 AM **S7.4 Non-invasive nature of corona charging on thermal Si/SiO_2 structures; an electron spin resonance study**
M. Dautrich*, P.M. Lenahan*, J.F. Conley, Jr.**, A.Y. Kang*,
**Penn State University,*
***Sharp Labs of America*

9:40 AM **COFFEE BREAK**

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Session 8 - High-K Characterization

Saturday, December 6, 2003
Session Chair: J. F. Zhang

10:10 AM **Opening remarks**

10:15 AM **S8.1** ***Invited*** **Suppression of Subcutaneous Oxidation during the Deposition of Amorphous $LaAlO_3$ on Silicon**
Darrell G. Schlom,
Penn State, USA

10:50 AM **S8.2 Interface Tunneling Mechanism of HfO_2/ Dual Metal Gate Stack with Varying Interface Layer Thickness and Different Bias Polarities**
Y. H. Kim, R. Choi, R. Jha*, J.H. Lee*, V. Misra* and J. C. Lee,
The University of Texas, Austin,
** North Carolina State University*

11:10 AM **S8.3 Physical structure of trapped electrons in atomic layer deposited hafnium oxide using $Hf(NO_3)_4$ precursor**
Andrew Y. Kang, Patrick. M. Lenahan,
The Pennsylvania State University,
John F. Conley and Yoshi Ono,
Sharp Labs of America

11:30 AM **S8.4 Inelastic Electron Tunneling Spectroscopy Study of Traps in Ultra-thin High-k Gate Dielectrics**
Wei He and T.P. Ma,
Yale University

11:50 AM **Closing remarks**

12:00 PM **End of SISC 2003**