SISC 2004

35th IEEE Semiconductor Interface Specialists Conference

December 9-11, 2004
The Catamaran Resort Hotel, San Diego, CA

Technical Program

Thursday, December 9, 2004

Session 1 – Gate Electrodes
Chair: C. M. Zetterling

08:00 **Welcome and opening remarks**

08:10 **1.1 *Invited* – Metal Gate Electrodes for CMOS Applications** Veena Misra, *North Carolina State University*

08:45 **1.2 – Characterization of Mobility with Candidate Metal Electrodes on HfO2** H.R. Lazar, R. Jha, and V. Misra, *North Carolina State University*, Y.H Kim, R.Choi, and J. Lee, *University of Texas at Austin*

09:05 **1.3 – Threshold tuning of fully silicided (FUSI) CMOS by silicide/dielectric interface modification** M. Copel, C. Cabral Jr., R. Pezzi and J. Kedzierski, *IBM Research Division*

Poster Session I: Gate Electrodes and High-κ
Chair: E. M. Vogel

09:25 **P-1 – An Improved Methodology for Gate Electrode Work Function Extraction in SiO_2 and High-k Gate Stack Systems Using Terraced Oxide Structures** G. A. Brown, G. Smith, J. Saulters, K. Matthews, H.-C. Wen, , P. Majhi (*Philips assignee*) and B. H. Lee (*IBM assignee*), *International SEMATECH*

09:28 **P-2 – Separating Interface Traps from Bulk Traps in High-k Gated MOSFETs Using Rise Time and Fall Time Dependence of Charge Pumping Current** H. M. Bu and T. P. Ma, *Yale University*

09:31 **P-3 – Characterization of Hot-Carrier and Plasma-Etching-Induced Interface Traps and Oxide Charges in HfO_xN_y Gated MOSFET's** K.-S. Chang-Liao, C.-Y. Lu, S.-H. Wang, and C.-H. Chang, *National Tsing Hua University*

09:34 **P-4 – A Study of Charge Trapping Dynamics in HfSiON Dielectrics Using the Single Stage Inverter Circuit**
C. Y. Kang, R. Choi, B. H. Lee (*IBM assignee*) and G. Bersuker, *International SEMATECH*
J. C. Lee, *University of Texas at Austin*

09:37 **P-5 – Determination of Interfacial Charge Density near the Poly-Si/High-κ Interface in MIS Devices** K. Z. Ahmed and P. A. Kraus, *Applied Materials, Inc.*

09:40 **P-6 – Chemical Analysis of High-k Gate Stack Interfaces** P. S. Lysaght, J. Barnett, N. Moumen (*IBM assignee*), B. Foran, M. Campin, G. Bersuker and H. R. Huff, *International SEMATECH*

09:43 COFFEE BREAK

Session 2 – High-κ Gate Dielectrics – I
Chair: R. M. Wallace

10:15 **Opening remarks**

10:20 **2.1 – *Invited* - Atomic layer deposition of high-k gate dielectrics onto Ge and III-V semiconductors** Martin M. Frank, V. K. Paruchuri, M. Copel, E. P. Gusev, and H. Shang, *IBM Semiconductor Res. And Dev. Center*

D. Starodub, T. Gustafsson, E. Garfunkel, C.-L. Hsueh, and Y.J. Chabal, *Rutgers University*
J. Grazul and D. A. Muller, *Cornell University*
G. D. Wilk, *ASM America*
M. Gribelyuk, *IBM Microelectronics Division*

10:55 **2.2 – Potential imaging of P+ poly-Si high-K gate stacks with HfO_2 gate dielectric: evidence for an oxide dipole** R. Ludeke, V. Narayanan, E.P. Gusev, E. Cartier and S. J. Chey, *IBM T. J. Watson Research Center*

11:15 **2.3 – Band alignment between (100)Si and complex rare-earth/transition metal oxides** V.V. Afanas'ev and A. Stesmans, *Univ. of Leuven*
C. Zhao and M. Caymax, *IMEC* T. Heeg and J. Schubert, *Forschungszentrum Jülich* Y. Jia and D.G. Schlom, *Penn State University* G. Lucovsky, *North Carolina State University*

Poster Session II: High-κ
Chair: M. Copel

11:35 **P-7 – The interface between single crystalline $LaAlO_3$ and silicon** D. O. Klenov and S. Stemmer, *University of California, Santa Barbara*
D. G. Schlom, *Pennsylvania State University*
H. Li, *Motorola*

11:38 **P-8 – Optimization of (a) compound semiconductor/dielectric, and (b) internal dielectric interfaces for GaAs and GaN MOS devices: processing and functionality** C. L. Hinkle, C. Krug, and G. Lucovsky, *North Carolina State University*
M. Passlack, *FreeScale Semiconductor*

11:41 **P-9 – High permittivity $Hf_xTi_{1-x}O_2$ gate dielectrics** M. Li, Z. Zhang, W. L. Gladfelter, and S. A. Campbell, *University of Minnesota*

11:44 **P-10 - Remote plasma CVD deposition of MOS devices with Zr,Si oxynitride alloys: local chemical bonding, thermal stability, electrical performance and reliability** B. Ju, C. L. Hinkle, G. Lucovsky, *North Carolina State University*

11:47 **P-11 - Experimental analysis of a Ge-HfO_2-TaN gate stack with a large amount of interface states** J. A. Croon, B. Kaczer, G. S. Lujan, S. Kubicek, G. Groeseneken (*also Univ. of Leuven*) and M. Meuris, *IMEC*

11:50 **P-12 - Charge Compensation Effect in Hafnium Titanate Multi-metal Oxide n-MOSFETs** S. J. Rhee, C. S. Kang, C. Y. Kang, C. H. Choi, M. Zhang, S. Krishnan, M. S. Akbar and J. C. Lee, *The University of Texas at Austin*

11:53 Adjourn for LUNCH on your own

Session 3 – Interfaces and Defects
Chair: A. Edwards

13:30 **Opening remarks**

13:35 **3.1** – *Invited* - **Interface Passivation for SiO_2 on 4H-SiC**
John R. Williams, S. Wang, T. Isaacs-Smith, and C. Ahyi, *Auburn University*
S. Dhar, A. Franceschetti, S. T. Pantelides and L. C. Feldman, *Vanderbilt University*
G. Chung, *Dow Corning Corporation*

14:10 **3.2 - Self-organizations at dielectric interfaces in high-k gate stacks with SiO_2 interlayers: surface roughness scattering of channel electrons and holes at Si-SiO_2 interfaces, and fixed charge at internal dielectric interfaces between SiO_2 and high-k alternatives** G. Lucovsky, *North Carolina State University*
J. C. Phillips, *Rutgers University*

14:30 **3.3 - Oxygen profiles in SiO_2/SiC structures and their relation with C clusters** F. C. Stedile, G. V. Soares, B. C. Ferrera, L. C. Goedtel, *IQ-UFRGS* I. J. R. Baumvol, *CCET-UCS*
C. Radtke, *CEA, DSM-DRECAM-SPCSI-SIMA*

How do I win the SISC Limerick Contest?

In order to win the Limerick contest at the SISC, your Limerick should reflect some (very funny) aspects related to the conference, its paper, or its papers, or its attendees – especially the "good old chaps" of the conference. It can also have some very innovative and funny personal touch or jokes about science in general and semiconductor (interfaces) in particular. As an example, here was a finalist entry in the 2000 contest, which reflected on the evolution of a "rump session" that was held and peppered with remarked from several "good old chaps"…

We all enjoyed the rump session
and heard reliability tension
opinions flew 'round
the session broke down
The cause? Hot comment Injection

More examples will be shown in the session breaks. Don't hesitate to ask if you have any questions. I'm looking forward to an entertaining Limerick contest!

Len Trombetta, University of Houston
Limerick Chair SISC 2003

Poster Session III: SiC and SiO_2
Chair: A. J. Lelis

14:50 **P-13 – Characterization and Modeling of Inversion-layer Electron Transport on Implanted Regions in 4H-SiC MOSFETs** Y. A. Zeng and M. H. White, *Lehigh University*
M. K. Das and A. K. Agarwal, *Cree, Inc.*

14:53 **P-14 - Paramagnetic Interface/Near Interface Deep Level Centers in 4H Silicon Carbide MOSFETs** D. J. Meyer, M. S. Dautrich and P. M. Lenahan, *The Pennsylvania State University*
A. Lelis, *U. S. Army Research Laboratory*
L. Lipkin, *Cree, Inc.*

14:56 **P-15 - Si-SiO_2 Interface Degradation in SONOS Nonvolatile Memory Devices Stressed by Hot Electron Injection or Hot Hole Injection** Y. Wang and M. H. White, *Lehigh University*

14:59 **P-16 – Electrical and physical characterization on ultra-thin SiO_2 dielectrics around the nanometer** C. Leroux, P. Mur, N. Rochat, D. Rouchon, R.Truche and G. Reimbold, *CEA-LETI/D2NT*
G. Ghibaudo, *IMEP (UMR CNRS/INPG/UJF)*

15:02 **P-17 - Channel Current Reduction Due to Gate Oxide Breakdown in MOSFETs** H. Hosoi, Y. Kamakura and K. Taniguchi, *Osaka University*

15:05 COFFEE BREAK

Session 4 – High-κ Gate Dielectrics – II
Chair: H. H. Tseng

15:35 **Opening Remarks**

15:40 **4.1 Characterizing Hf-Based Gate Dielectric Properties Using Ultra-Short Pulse I-V Measurements** C. D. Young, R. Choi, B. H. Lee (*IBM assignee*), P. Zeitzoff, J. H. Sim, H. R. Harris, G. A. Brown and G. Bersuker, *International SEMATECH*

16:00 **4.2 - Interatomic diffusion between Hf-silicate and interfacial SiO_2 layers** Y. Kosaka, T. Yamasaki and C. Kaneta, *Fujitsu Laboratories Limited*

16:20 **Late News Oral #1 - Significant C-V Curve Distortion in Accumulation Regime of Poly-Si/High-k MOS Capacitors due to Fermi-Level Pinning** N. Yasuda, H. Satake, and T. Nabatame, *AIST*
A. Toriumi , *AIST* and *The University of Tokyo*

16:40 **Late News Oral #\2 - A Suppression of Interfacial Oxide Formation by Oxygen-Scavenging Technique to Reduce EOT to < 0.7nm of "Undoped"HfO_2/Si Gate Stacks** C. Choi, C.-Y. Kang, S. J. Rhee, M. S. Akbar, S. A. Krishnam, M. Zhang, and J. C. Lee, *The University of Texas at Austin,*

Poster Session IV: High-κ
Chair: G. Wilk

17:00 **P-18 – Improvement of Electrical Properties of HfO2 Gate Stacks and Effects of Annealing on Charge in the Stacks** Z. Zhang, M. Li and S. A. Campbell, *University of Minnesota*

17:03 **P-19 - The Role of Interfacial Oxides in Mobility Improvement in HfO_2 Gate Stacks** J. J. Peterson, S. A. Krishnan, C. D. Young, B.-H. Lee, J. Barnett, G. A. Brown, J. Gutt, S. Gopalan, P. D. Kirsch (*IBM assignee*), H.-J. Li (*Infineon assignee*), N. Moumen (*IBM assignee*), P. Lysaght, G. Bersuker, P. M. Zeitzoff , M. I. Gardner (*AMD assignee*) and H. R. Huff, *International SEMATECH*

17:06 **P-20 - Charge Trapping in SiO_2/ALD-HfO_2 Gate Stacks** Y. Zhao, A. J. Bronczyk, H. Wu and M. H. White, *Lehigh University*

17:09 **P-21 – Effects of Bulk Nitrogen in HfO_xN_y Gate Dielectric on Current Conduction and Charge Trapping Properties of MOS Devices** K.-S. Chang-Liao, C.-L. Cheng and T.-K. Wang, *National Tsing Hua University*

17:12 **P-22 - Spectroscopic studies of coupled d-states transition metal/rare earth complex oxides: is this a viable approach for band edge engineering in CMOS devices?** G. Lucovsky, Y. Zhang, L. Edge, C. C. Fulton, Y. Zou, R. J. Nemanich, and H. Ade, *North Carolina State University*
D.G Schlom, *Pennsylvania State University*

17:15 **Late News Poster #1 - Band edge states derived from Jahn-Teller term splittings in high-k dielectrics: bias-dependent interfacial trapping in gate stacks for advanced Si devices** G. Lucovsky, C. Fulton, R. Nemanich, *North Carolina State University*
L. Edge and D. Schlom, *Penn State University*
and J. Luning, *Stanford Synchrotron Research Labs*

17:18 **Late News Poster #2 - Intrinsic Effect of a Nitrogen Atom for Reduction in Leakage Current through Hf-based High-k Gate Dielectrics - Nitrogen Induced Atomistic Cutoff of "O Vacancy Mediated Leakage Paths"** N. Umezawa, K. Shiraishi, T. Ohno1, H. Watanabe, T. Chikow, K. Torii, K. Yamabe, K. Yamada, H. Kitajima and T. Arikado,

NIMS, Univ. Tsukuba, Osaka Univ., Selete, Waseda Univ.

17:21 **Late News Poster #3 - Permittivity Increase of Yttrium Doped HfO2 through Structural Phase Transformation** K. Kita, K. Kyuno and A. Toriumi, *The University of Tokyo*

17:24 **Late News Poster #4 - Ti metal gate with appropriate workfunction for ALD-HfO2 NMOS Devices** H. Yang, S. Choi, S. Huh, and H. Hwang, *Gwangju Institute of Science and Technology*

17:27 **Late News Poster #5 - Surface Cleaning and Preparation Related Aspects of the Germanium Surface Chemistry** B. Onsia, M. Caymax, T. Conard, S. De Gendt, A. Delabie, M. Heyns, P. Mertens, M. Meuris, S. Sioncke, S. Van Elshocht, J. Van Steenbergen, *IMEC,* C. Vinckier, *Univ. of Leuven*, and A. Theuwis, *Umicore*

17:30 **Adjourn**

19:00 Thursday Evening Poster Reception

SISC 2004

35th IEEE Semiconductor Interface Specialists Conference

December 9-11, 2004
The Catamaran Resort Hotel, San Diego, CA

Technical Program

Friday, December 10, 2004

Session 5 – Oxide Reliability
Chair: L. Selmi

08:00 **Opening Remarks**

08:05 **5.1 *Invited* – Silicon Nanocrystals: Physics and Memory Technologies** Ramachandran Muralidhar, R. Rao, R. F. Steimle, M. Sadd, C. T. Swift, B. Hradsky, S. Straub, T. Merchant, M. Stoker, S.G. H. Anderson, M. Rossow, J. Yater, B. Acred, K. Harber, E. J. Prinz, and B. E. White Jr., *FreeScale Semiconductor*

08:40 **5.2 Reaction-Dispersive H+ Transport Model for NBTI in pMOSFETs** M. Houssa, M. Aoulaiche, S. De Gendt, G. Groeseneken (*also Univ. of Leuven*) and M. Heyns, *IMEC* A. Stesmans, *University of Leuven*

09:00 **5.3 Static and Dynamic NBTI of Strained Channel pMOSFETs**
H.-N. Lin and T.-Y. Huang, *National Chiao-Tung University* H.-C. Lin, *National Nano Device Laboratories* C.-H. Ko, C.-H. Ge, C.-C. Huang and M.-H. Chi, *Taiwan Semiconductor Manufacturing Company*

09:20 **5.4 The influence of recovery and temperature on the NBTI power-law exponent** B. Kaczer, R. Degraeve, V. Arkhipov, N. Collaert, G. Groeseneken (*also Univ. of Leuven*) and M. Goodwin (*Texas Instruments affiliate*), *IMEC*

9:40 BREAK

Session 6 – Theory and Hydrogen
Chair: P. Blochl

10:10 **Opening Remarks**

10:15 **6.1 *Invited* - Hydrogen interactions with semiconductors, oxides, and their interfaces** Chris G. Van de Walle, *University of Californi, Santa Barbara*

10:50 **6.2 Density functional studies of the origin of a residual charge in HfO_2 and at the HfO_2/Si interface** J. Gavartin and A. Shluger, *University College London*
A. S. Foster, *Helsinki University of Technology*
L. Fonseca, *FreeScale Semiconductor*

11:10 **6.3 Dramatic Enhancement of Phonon Energy Coupling at the SiO_2/Si Interface Due to Rapid Thermal Processing of the Gate Oxide** Z. Chen and J. Guo, *University of Kentucky*

11:30 **6.4 On the role of hydrogen and holes in positive charge formation in gate oxides** C. Z..Zhao and J. F..Zhang, *Liverpool John Moores University*

11:50 **Adjourn for Lunch**

15:00 Optional Friday Afternoon Rump Sessions

19:00 Friday Evening ***Conference Banquet and Limerick Contest***

SISC 2004

35th IEEE Semiconductor Interface Specialists Conference

December 9-11, 2004
The Catamaran Resort Hotel, San Diego, CA

Technical Program

Saturday, December 11, 2004

Session 7 – High-κ Gate Dielectrics – III
Chair: M. Houssa

08:00 **Opening Remarks**

08:05 **7.1 *Invited* - Ge Surface Passivation for High Performance MOSFETs** Krishna C. Saraswat, C. O. Chui, A. N., H. Kim and P. McIntyre, *Stanford University*

08:40 **7.2 – HfO_2 high-κ gate dielectrics on germanium by molecular beam deposition** A. Dimoulas, G. Mavrou, G. Vellianitis, E. Evangelou, N. Boukos and A. Travlos, *NCSR DEMOKRITOS* M. Houssa and M. Caymax, *IMEC*

09:00 **7.3 – Point defects at interfacial layers in stacks of (100)Ge with nm-thin HfO_2 and $GeO_x(N_y)$ insulators probed by electron spin resonance** A. Stesmans and V. V. Afanas'ev, *University of Leuven*

09:20 **7.4 – In-Situ Interface Characterization and Real-Time Depth Profiling of High-K Dielectrics Stacks by Open Circuit Potential Measurements Coupled with Atomic Force Microscopy** V. K. Paruchuri and E. P. Gusev, *IBM Semiconductor Research and Development Center* H. F. Okorn-Schmidt, *SEZ AG*

9:40 BREAK

Session 8 – High-κ Gate Dielectrics – IV
Chair: K. Ahmed

10:10 **Opening Remarks**

10:15 **8.1 *Invited* - On the methodology for Reliability Characterization of MOS Devices with high-k Gate Dielectrics** Andreas Kerber, *Infineon Technologies AG*

10:50 **8.1 – Impact of enhanced localized degradation on time-to-breakdown in high-k oxides** T. Kauerauf, G. Groeseneken, H. Maes, *IMEC and University of Leuven* Ph. J. Roussel and R. Degraeve, *IMEC*

11:10 **8.2 - Tunneling Spectroscopy Study of Traps in MOS Structures with High-k Gate Dielectrics** M. Wang, W. He and T. P. Ma, *Yale University*

11:30 **8.3 - AC stress induced threshold voltage shift in TiN/Hf-Silicate NMOSFETs** R. Choi, R. Harris, B-H. H Lee (*IBM assignee*), K. Mathews, M. Pendley, C. D. Young, J. H. Sim, and G. Bersuker I*nternational SEMATECH*

11:50 **Closing Remarks**

12:00 End of SISC 2004