36th IEEE Semiconductor Interface Specialists Conference

December 1 – 3, 2005
Key Bridge Marriott, Arlington, VA

ABSTRACTS

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Technical Chair: Glen Wilk

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SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, “MOS Physics and Technology,” published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author or either an oral or poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque and an honorarium sent to the winner after the conference. To honor the winner, the award is announced at the conference taking place the following year.

The *2004 SISC Ed Nicollian Award for Best Student Paper* was given to Miaomiao Wang of Yale University, New Haven, Connecticut. The paper was entitled “Tunneling Spectroscopy Study of Traps in MOS Structures with High-k Gate Dielectrics,” with co-authors W. He and T.P. Ma.

Those eligible and wishing to be considered for the 2005 SISC Ed Nicollian Award should contact the 2005 IEEE SISC Technical Chair immediately.

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This meeting is sponsored by the IEEE Electron Devices Society

Conference Agenda Overview

Wednesday, November 30, 2005

Registration	6:00pm – 9:00pm

Hospitality Suite: 9:00pm – midnight

Thursday, December 1, 2005

Registration	8:00am – 5:00pm
Session 1: Gate Electrodes	8:00am – 9:25am
Poster Session 1: Gate Electrodes and High-k	9:25am – 9:43am
Session 2: High-k Reliability I	10:15am – 11:30am
Poster Session 2: High-k Gate Dielectrics I	11:30am – 11:51am
Session 3: High-k/Metal Gate Interfaces	1:30pm – 2:25pm
Poster Session 3: High-k Gate Dielectrics II	2:25pm – 2:46pm
Session 4: Oxide Reliability	3:15pm – 4:30pm
Poster Session 4: Memory, SiO_2 and High-k	4:30pm – 4:51pm

Poster Reception: 7:00pm – 10:00pm
Hospitality Suite: 9:00pm – midnight

Friday, December 2, 2005

Registration	8:00am – 5:00pm
Session 5: Non-Volatile Memory Technologies	8:00am – 10:00am
Session 6: Memory and High-k Reliability II	10:30am – 12:05pm
Informal Rump Sessions (Optional) – Topics TBD	3:00pm – 5:00pm

SISC Banquet and Limerick Contest: 7:00pm – 10:00pm
Hospitality Suite: 10:00pm – midnight

Saturday, December 3, 2005

Session 7: Defects and Traps	8:20am – 9:50am
Session 8: Theory and High-k	10:20am – 12:05pm

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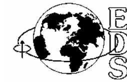

December 1 – 3, 2005
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Session 1: Gate Electrodes

Thursday, December 1, 2005
Session Chair: J. Chambers

8:00 AM **Welcome and Opening Remarks**

8:10 AM **1.1 *Invited* – Performance and threshold-voltage control in high-k/metal-gate FETs,** E. Cartier, *IBM*

8:45 AM **1.2 - Tantalum-carbo-nitride electrodes and the impact of interface chemistry on MOSFET device characteristics,** J. Schaeffer, R. Gregory, L. Fonseca, C. Capasso, D. Werho, H. Tseng, D. Gilmer, W. Chang, B. Hu, Y. Liang, E. Luckowski, D. Triyoso, M. Raymond, B. Taylor, R. Hegde, Y. Chiu, B. White, P. Tobin, *Freescale Semiconductor*

9:05 AM **1.3 - Process-induced work function modulations of $Ta_xAl_{1-x}N_y$ metal gate electrodes,** H. Alshareef, K. Choi, H. Wen, R. Harris, H. Luan, M. Quevedo-Lopez, P. Majhi, B. Lee, *International SEMATECH*

Poster Session 1: Gate Electrodes and High-k

Thursday, December 1, 2005
Session Chair: V. Afanas'ev

9:25 AM **P-1 - Determination of effective workfunction for fully silicided (FUSI) Ni-Silicide gate on HfSiON,** K. Takahashi, M. Terai, T. Hase, T. Tatsumi, *NEC*

9:28 AM **P-2 - Influence of continuous work function variation on electric properties by combinatorial materials deposition method**, K. Ohmori, P. Ahmet, D. Kukuruznyak, T. Nagata, K. Nakajima, K. Shiraishi, K. Yamabe, H. Watanabe, K. Yamada, G. Richter, T. Wagner, K. Chang, M. Green, T. Chikyow, *National Institute for Materials Science, Japan*

9:31 AM **P-3 - The composition effects of hafnium (Hf) and tantalum (Ta) in Hf_xTa_yN metal gate on the thermal stability of MOS Devices,** C. Cheng, K. Chang-Liao, T. Wang, T. Wang, H. Wang, *National Formosa University, Taiwan*

9:34 AM **P-4 - Substrate crystallographic effects on local titanium nitride work function,** N. Gaillard, D. Mariolle, M. Gros-Jean, A. Bsiesy, *ST Microelectronics*

9:37 AM **P-5 - Realization of ultrathin metal inserted poly-Si stack (UT-MIPS) structure using a atomic vapor deposition (AVD®) system,** S. Han, H. Jung, Y. Kim, H. Lim, M. Kim , J. Lee, M. Young, Yu, N. Lee, H. Baik, Y. Chung, W. Park, D. Y. Ko, O. Boissière, J. Lindner, *Samsung Electronics Co.*

9:40 AM **P-6 - Observations of NBTI-induced atomic scale defects,** J. Campbell, P. Lenahan, A. Krishnan, S. Krishnan, *Penn State University*

9:43AM **BREAK**

Session 2: High-k Reliability I

Thursday, December 1, 2005
Session Chair: M. Houssa

10:15 AM **2.1 – *Invited* – Device and Reliability Characteristics of HfSiON-CMOSFETs**, M. Takayanagi, *Toshiba*

10:50 AM **2.2 – Improved BTI Characteristics for Bulk versus Interface Process Enhancements in Metal Gate HfO_2 based MOSFETS**, S. Kalpat, H. Tseng, R. Hegde, M. Ramon, A. Haggag, M. Moosa, P. Tobin, B. White, *Freescale Semiconductor*

11:10 AM **2.3 - Enhanced reliability in ultra-scaled HfSiON gate dielectrics through suppressed crystallization**, M. Quevedo-Lopez, S. Krishnan, P. Kirsch, H. Li, J. Peterson, B. Lee, G. Pant, B. Gnade, M. Kim, R. Wallace., *International SEMATECH*

Poster Session 2: High-k Gate Dielectrics I

Thursday, December 1, 2005
Session Chair: M. Niwa

11:30 AM **P-7 – Asymmetries in the electrical activity of intrinsic grain-boundary and O-atom vacancy defects in HfO_2/ZrO_2, and at their interfaces with SiO_2: a possible show-stopper for CMOS high-k devices**, G. Lucovsky, C. Fulton, C. Hinkle, S. Lee, J. Lüning, *North Carolina State University*

11:33 AM **P-8 - Spectroscopic studies of differences in band edge electronic structure in transition metal elemental and complex oxides, and silicate alloys with different short, intermediate and long range order,** C. Fulton, G. Lucovsky, L. Edge, N. Stoute, T. Seo, and J. Lüning, *North Caroline State University*

11:36 AM **P-9 – Engineering the interface properties of HfO_2 by Ti addition,** D. Triyoso, R. Gregory, X. Wang, M. Ramon, S. Zollner, R. Hegde , D. Roan, P. Tobin, B. White, *Freescale Semiconductor*

11:39 AM **P-10 – Electrical and reliability characteristics of HfSiO MOSFET annealed in F_2 ambient** M. Chang, M. Jo, H. Park, M. Rahman and B. Lee, R. Choi, H. Hwang, *Gwangju Institute of Science and Technology*

11:42 AM **P-11 – High crystallization temperature and low fixed charge density of $HfLaO_x$ films,** Y. Yamamoto, K. Kita, K. Kyuno, A. Toriumi , *University of Tokyo*

11:45 AM **P-12 – Electron energy band alignment at interfaces of (100)Ge with Gd_2O_3 and LaHfOx,** V. Afanas'ev, S. Shamuilia, A. Dimoulas, A. Stesmans, M. Houssa, *University of Leuven*

11:48 AM **P-13 – Band offsets at interfaces of (100)Si with MBD-grown $LaAlO_3$, $LaScO_3$, and Sc_2O_3,** V. Afanas'ev, L. Edge, A. Stesmans, D. Schlom, *University of Leuven*

11:51 AM **Adjourn for Lunch**

Session 3: High-k/Metal Gate Interfaces

Thursday, December 1, 2005
Session Chair: D. Triyoso

1:30 PM **3.1 – *Invited* - Interface Band Alignment at High-k / Metal Gate Structures: Interface Dipoles and Internal Fields,** R. Nemanich, *North Carolina State University*

2:05 PM **3.2 - Effects of intrinsic and extrinsic reactions at metal/high-k interfaces on electrical properties of gate stacks**, H. Watanabe, S. Yoshida, Y. Watanabe, E. Mishima, K. Kawamura, Y. Kita, T. Shimura, K. Yasutake, Y. Akasaka, Y. Nara, K. Shiraishi, K. Yamada, *Osaka University*

Poster Session 3: High-k Gate Dielectrics II

Thursday, December 1, 2005
Session Chair: M. Frank

2:25 PM **P-14 – Germanium p-MOSFETs fabricated using molecular beam deposited TaN/ HfO_2/GeO_xN_y gate stack,** A. Ritenour, R.Z. Lei, A. Dimoulas, G. Mavrou, Y. Panayiotatos, D. Antoniadis, W. Tsai, *MIT*

2:28 PM **P-15 - A new twin gated-diode measurement for the interface characterization of ultra-thin oxynitride and high-k gate dielectric MOSFETs**, G. Lee, S. Chung, A. Mao, W. Lin, C. Yang, Y. Hsieh, K. Chu, L. Cheng, W. Yu, H. Tai, L. Hsu, C. Lee, C. Chang, C. Chen, T. Liu, C. Huang, W. Shiau, H. Meng, C. Tsai, S. Tzou, S. Sun, *National Chiao Tung University*

2:31 PM **P-16 - Depth profiling of border traps in MOS capacitors with HfO_xN_y gate dielectric by charge-pumping technique,** K. Chang-Liao, C. Lu, S. Wang, C. Cheng, *National Tsing Hua University, Taiwan*

2:34 PM **P-17 - Effects of irradiation and bias-temperature stress on charge trapping in HfO_2 gate dielectrics,** X.. Zhou, D. Fleetwood, L. Tsetseris, R. Schrimpf, S. Pantelides, J. Felix, E. Gusev, C. D'Emic, *Vanderbilt University*

2:37 PM **P-18 - Hot carrier reliability study of high-k MOSFET after high pressure pure D_2 annealing and subsequent annealing in N_2,** M.S. Rahman, H. Park, M. Chang, B. Lee, R. Choi, H. Hwang, *Gwangju Institute of Science and Technology, Korea*

2:40 PM **P-19 - Single Hf atoms in the ultrathin SiO_2 interlayer between the HfO_2 dielectric and Si substrate: How do they modify the interface?** S. Rashkeev, K. van Benthem, S. Pantelides, S. Pennycook, *Oak Ridge National Laboratory*

2:43 PM **P-20 – Electron tunneling spectroscopy study of MOS structures with $LaAlO_3$ and $LaScO_3$ gate dielectrics,** M. Wang, W. He, T. Ma, L. Edge, D. Schlom, *Yale University*

2:46 PM **BREAK**

Session 4: Oxide Reliability

Thursday, December 1, 2001
Session Chair: B. Kaczer

3:15 PM **4.1 *Invited* – Elementary Considerations in Reliability Physics: How a simple model illuminates the mechanism of NBTI Degradation, resolves a 40-year old puzzle, and establishes a protocol for lifetime extrapolation,** M.A. Alam, *Purdue University*

3:50 AM **4.2 - Effects of 'On-The-Fly' Measurement Temperature on Negative Bias Temperature Instability**, M. Chang, J. Zhang, G. Groeseneken, *Liverpool John Moores University*

4:10 PM **4.3 - Investigation of Channel-length dependent Time-to-Breakdown (t_{BD}) with variable frequency charge pumping,** M. Zahid, R. Degraeve, T. Kauerauf, G. Groeseneken, J. Zhang, *Liverpool John Moores University*

Poster Session 4: Memory, SiO_2 and High-k

Thursday, December 1, 2005
Session Chair: K. Ahmed

4:30 PM **P-21 – Characterization of $Ge_2Sb_2Te_5$ and Sb-excess $Ge_2Sb_{2+x}Te_5$ chalcogenide thin film for phase change memory applications**, K. Choi, S. Ryu, S. Yoon, N. Lee, Y. Park, S. Lee, B. Yu, *Electronics and Telecommunications Research Institute*, *Korea*

4:33 PM **P22 – Effects of Polycrystalline Silicon-Germanium and Silicon Heating Layers on Phase-Change Memory Operation,** S. Lee, K. Choi, S. Ryu, S. Yoon, N. Lee, Y. Park, S. Kim, S. Lee, B. Yu, *Electronics and Telecommunications Research Institute*, *Korea*

4:36 PM **P-23 – Identification of Defect Structure in 4H Silicon Carbide MOSFETs with Thermally Grown Oxides via Magnetic Resonance and Transmission Electron Microscopy**, M. Dautrich, P. Lenahan, A. Lelis, T. Zheleva, *Penn State University*

4:39 PM **P-24 – SiO_2-SiO_2 Charge Trapping Devices**, M. Kim, S. Chae, C. Kim, J. Lee, S. Tiwari, *Cornell University*

4:42 PM **P-25 – Fundamental modeling of Group V dopant diffusivity and clustering in strained Si and SiGe alloys,** M. Haran, P. Clancy, *Cornell University*

4:45 PM **P-26 – First Principles Study of HfO_2/SiO_2 Interfaces: Intrinsic and Extrinsic Defect Properties,** J. Ha, P. McIntyre, K. Cho, *Stanford University*

4:48 PM **P-27 – A Novel EOT Extraction Method for Ultrathin High-k Gate Dielectrics,** D. Guo, L. Song, T. Ma, *Yale University*

4:51 PM **Adjourn**

7 – 10 P.M. Thursday Evening ***Poster Reception***

Session 5: Non-Volatile Memory Technologies

Friday, December 2, 2005
Session Chair: H.H. Tseng

8:00 AM **Morning Announcements**

8:10 AM **5.1 *Invited* – Floating Gate Flash Memory Technology,** K. Parat, *Intel*

8:45 AM **5.2 *Invited* – New Memory Concepts: from Silicon Nanocrystal Technologies to Molecular Memories,** B. de Salvo, *LETI, France*

9:20 AM **5.3 Physical Understanding of the Endurance Mechanisms in the ONO Layer of a SONOS Flash Memory Devices**, C. Chen, P. Chiang, S. Chung, T. Chen, G. Chou, C. Chu, *National Chiao Tung University, Taiwan*

9:40 AM **5.4 SONOS-type Non-volatile Memory with All Silicon Nitride Dielectric Stack,** F. Yeh, Y. Liu, X. Wang, T. Ma, *Yale University*

10:00 AM **BREAK**

Session 6: Memory and High-k Reliability II

Friday, December 2, 2005
Session Chair: A. Lelis

10:30 AM **6.1 *Invited* - DRAM Memory Technologies**, K. Kim, G. Jeong, *Samsung Electronics Co.*

11:05 AM **6.2 Nitrogen in poly-Si/HfSiO gate stacks: carrier mobility impact of traps and fixed charge,** M. Frank, K. Maitra, E. Cartier, B. Linder, P. Jamison, M. Gordon, M. Copel, *IBM*

11:25 AM **6.3 NBTI and charge trapping in HfO_2 based pMOSFETs,** L. Song, X. Wang, T. Ma, *Yale University*

11:45 AM **6.4 H_2/D_2 isotopic effect on negative bias temperature instabilities in SiO_x/HfSiON/TaN gate stacks,** M. Houssa, M. Aoulaiche, A. Stesmans, S. De Gendt, G. Groeseneken, M. Heyns, *IMEC*

12:05 PM **Adjourn – Technical Committee / Invited Speaker Luncheon**

3:00 – 5:00 PM **Optional Rump Sessions – Topics TBD**

7 – 10 P.M. Friday Evening ***Conference Banquet and Limerick Contest***

Session 7: Defects and Traps

Saturday, December 3, 2005
Session Chair: A. Kerber

8:20 AM **Morning Announcements**

8:30 AM **7.1 - Modification of interfacial SiO_2 layer in high-k gate stacks,** G. Besuker, C. S. Park, J. Barnett, P. Lysaght, P. Kirsch, B. Lee, P. Lenahan, J. Ryan, J. Greer, A. Korkin, *International SEMATECH*

8:50 AM **7.2 - Fast relaxation of trapped charges and its implications for characterizing high-k gate dielectrics,** R. Choi, B. Lee, K. Mathur, C. Young, Y. Zhao, G. Bersuker, *International SEMATECH*

9:10 PM **7.3 - Inherent point defects in thermal (100) tensile strained-Si/SiO_2 entities probed by electron spin resonance,** A. Stesmans, P. Somers, V. Afanas'ev, *University of Leuven*

9:30 AM **7.4 – Experimental estimation of the width of the hot-carrier-degraded region and the density of locally-generated hetero-interface traps in as SiGe/Si heterostructure,** T. Tsuchiya, S. Mishima, M. Sakuraba, J. Murota, *Shimane University, Japan*

9:50 AM **BREAK**

Session 8: Theory and High-k

Saturday, December 3, 2005
Session Chair: B.H. Lee

10:20 AM **8.1 – Defect energy levels in HfO_2 and related high dielectric constant gate oxides,** J. Robertson, K. Xiong, S. Clark, *Cambridge University*

10:40 AM **8.2 – Ion scattering study of oxygen diffusion in ultrathin high-k metal oxide gate stacks** L. Goncharova, D. Starodub, R. Barnes, E. Garfunkel, T. Gustafsson, *Rutgers University*

11:00 AM **8.3 – Reduction in oxygen vacany formation energy caused by nitrogen incorporation in Hf-based high-k dielectrics,** N. Umezawa, K. Shiraishi, Y. Akasaka, S. Inumiya, A. Uedono, S. Miyazaki, T. Chikyow, T. Ohno, Y. Nara, and K. Yamada, *NIMS, Japan*

11:20 AM **8.4 – Unpinned SiN/GaAs interface for enhancement-mode MISFET application,** W. Li, Y. Liu, X. Wang, T. Ma, *Yale University*

11:40 AM **8.5 – Suppression of chemical phase separation and transition metal (Zr, Hf) oxide crystallization in Zr and HfSi oxynitride alloy high-k dielectrics for CMOS applications,** G. Lucovsky, B. Ju, and J. Lüning, *North Carolina State University*

12:00 PM **Closing Remarks**