37th IEEE Semiconductor Interface Specialists Conference

December 7-9, 2006
Catamaran Resort Hotel, San Diego, CA

ABSTRACTS

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Technical Chair: Matt Copel

Arrangements Chair: Ben Kaczer

Ex-Officio: Eric Vogel

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This meeting is sponsored by the IEEE Electron Devices Society

CONFERENCE AGENDA OVERVIEW

Wednesday, December 6, 2006

Registration: 6:00pm-9:00pm / Hotel Lobby Area
Hospitality Room: 9:00pm-Midnight / Suite 308

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Thursday, December 7, 2006

Kon Tiki Ballroom

Registration 8:00am-5:00pm
Session 1 – High-κI ..... 8:00am-9:20 am
Poster Session I ..... 9:20 am-9:44 am
Session 2 – NBTI and Reliability 10:15 am-11:35am
Poster Session II 11:35am-11:59am
Session 3 – NVRAM and High-κ ..... 1:30pm-2:50 pm
Poster Session III ..... 2:50 pm-3:11 pm
Session 4 – Dielectrics on High Mobility Substrates I ..... 3:35 pm-4:20 pm
Poster Session IV ..... 4:20 pm-4:58 pm

Poster Reception: 7:00pm-10:00pm / Birch Aquarium

Hospitality Room: 10:00pm-Midnight / Suite 308

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Friday, December 8, 2006

Kon Tiki Ballroom

Registration ..... 8:00am-12 noon
Session 5 – Theory 8:00am-9:40am
Session 6 – High-*κ*II 10:10am-11:50am
Optional Rump Session 3:00pm-5:00pm

SISC Banquet and Limerick Contest: 7:00pm-10:00pm / Rousseau Suite
Hospitality Room: 10:00pm-Midnight / Suite 308

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Saturday, December 9, 2006

Kon Tiki Ballroom

Session 7 – High-*κ* III 8:20am-10:00am
Session 8 – Dielectrics on High Mobility Substrates II 10:20am-12noon

SISC 2006

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IEEE

SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology," published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author or either an oral or poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque and an honorarium sent to the winner after the conference. To honor the winner, the award is announced at the conference taking place the following year.

The *2005 SISC Ed Nicollian Award for Best Student Paper* was given to Frank C. Yeh of Yale University, New Haven, Connecticut. The paper was entitled "SONOS-type Non-volatile Memory with All Silicon Nitride Dielectric Stack" with co-authors Y. X. Liu, X. W.Wang and T. P. Ma.

Those eligible and wishing to be considered for the 2006 SISC Ed Nicollian Award should contact the 2006 IEEE SISC Technical Chair immediately.

SISC 2006

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Session 1 – High-κ I

Thursday, December 7, 2006
Session Chair: J. Robertson

8:00 AM **Welcome and Opening Remarks**

8:05 AM **1.1 *Invited* – Challenges in achieving low PMOS Threshold Voltages with Metal Gate Electrodes on Scaled High κ Dielectrics,** Sri Samevadam, *Freescale Semiconductor*

8:40 AM **1.2 - Characterization of TiN/HfO_2/SiO_2 MOSFETs by extracting mobility from magnetoresistance measurements,** L. Thevenod, M. Cassé, W. Desrat, M. Mouis, G. Reimbold, and F. Boulanger, *CEA-DRT/LETI*

9:00 AM **1.3 - Role of soft-optical phonon scattering in aggressively scaled HfO_2 MOSFETs with metal gates: Thickness and temperature dependent mobility studies,** P. Srinivasan, B. P. Linder, V. Narayanan and E. Cartier, *New Jersey Inst. Of Tech.*

Poster Session I

Thursday, December 7, 2006
Session Chair: V. Afanas'ev

9:20 AM **P.1 - Aluminum nitride, oxide, and oxynitride capping layers for poly-Si/HfSiO threshold voltage control,** Martin M. Frank, K.-L. Lee, V. Narayanan, B. P. Linder, E. A. Cartier, V. K. Paruchuri, P. C. Jamison, G. Singco, M. Copel, N. Bojarczuk, P. Flaitz, M. Gribelyuk, S. Guha, R. Jammy, and M. Chudzik, *IBM*

9:23 AM **P.2 - Scalability of Higher-κ Si Doped HfO_2 down to EOT = 0.6 nm in Purely Direct Tunneling Regime**, Kazuyuki Tomida, Koji Kita and Akira Toriumi, *University of Tokyo, Japan*

9:26 AM **P.3 - Elements Redistribution of TiN/HfSiON gate stack in High-Temperature Annealing Enhanced by Oxygen Incorporation,** Takeo Matsuki, Seiji Inumiya, Nobuyuki Mise, Takahisa Eimori, and Yasuo Nara, *Semiconductor Leading Edge Technologies, Japan*

9:29 AM **P.4 - ZrO_2 addition and capping layer studies to improve HfO_2 film quality,** D. H. Triyoso, R. I. Hegde, R. Gregory, X-D Wang, J. Schaeffer, N. Ramani, S. B. Samavedam, and B. E. White, Jr., *Freescale Semiconductor*

9:32 AM **P.5 - Understanding of the thermal stability of the "high κ"/metal gate stack via 2 "high κ" and metal deposition techniques,** V. Cosnier, P. Besson, V. Loup, L. Vandroux2, S. Minoret, M. Cassé, X. Garros, J-M. Pedini, S. Lhostis, and K. Dabertrand, *STMicroelectronics, France*

9:35 AM **P.6 - Electron spin resonance study of as-deposited and annealed $(HfO_2)_x(SiO_2)_{1-x}$ high-κ dielectrics on Si,** P. T. Chen, B. B. Triplett, Y. Nishi, P. H. Kasai, J. J. Chambers, and L. Colombo, *Stanford University*

9:38 AM **P.7 - Charge Trapping Study of High-κ Gated MOSFETs With the PASHEI Technique,** L. Y. Song, X. W. Wang, T. P. Ma, H.-H.Tseng, and P. J. Tobin, *Yale University*

9:41 AM **P.8 - Profiling Border Trap Density and Energy Distribution along the Gate Dielectric Bulk of High-κ Gated MOS Devices,** Kuei-Shu Chang-Liao, Chun-Yuan Lu, Chun-Chang Lu, Ping-Hung Tsai, and Tien-Ko Wang, *National Tsing Hua University, Taiwan*

9:44AM **BREAK**

Session 2 – NBTI and Reliability

Thursday, December 7, 2006
Session Chair: B. H. Lee

10:15 AM **Opening Remarks**

10:20 AM **2.1 – *Invited* - Multi-Vibrational Hydrogen Release: A dielectric breakdown model for ultra-thin SiO_2/SiON and high-κ stack**, Guillame Ribes, *STMicroelectronics, France*

10:55 AM **2.2 – NBTI Analysis Methodology for High-κ Gate Stacks**, G. Bersuker, A. Neugroschel, R. Choi, C. Cochrane, P. Lenahan, D. Heh, C. Young, C.Y. Kang, B.H. Lee, and R. Jammy, *Sematech*

11:15 AM **2.3 - Comparison of metal/dielectric energy barriers measured with internal photoemission and ballistic electron emission microscopy (BEEM)**, W. Cai, K. B. Park, S. E. Stone, and J. P. Pelz, *Ohio State University*

Poster Session II

Thursday, December 7, 2006
Session Chair: J. Chambers

11:35 AM **P.9 – Highly Nitrogen-incorporated SiON using the Novel Plasma Nitridation Process**, Dong-Chan Kim, Seong-Hoon Jeong, Jin-Hwa Heo, Mann-Ho Cho, Myoung-Bum Lee, Sang-Bom Kang, Siyoung Choi, Dae-Won Moon, U-In Chung, and Joo-Tae Moon, *Samsung Electronics, S. Korea*

11:38 AM **P.10 - Electron-Stimulated Desorption of 1H and 2H Atoms from MOS Interfaces - Simulation with Si Surface and Homogenous Electron Injection,** Toshiki Mori and Satoru Watanabe, *Fujitsu, Japan*

11:41 AM **P.11 – Single Trap Characterization in SON MOSFETs by Random Telegraph Signal Analysis,** S. Ferraton, L. Militaru, A. Souifi, S. Monfray, and T. Skotnicki, *LPM, INSA de Lyon , France*

11:44 AM **P.12 – Back-interface Characterization of SOI MOSFETs using Transient Charge Pumping,** C. Sandhya, N. Mani Bharath, and V. Ramgopal Rao, *IIT Bombay, India*

11:47 AM **P.13 – Electric and interface characteristics of Si_3N_4 films formed by directly radical nitridation on Si (110) and Si (100) surfaces,** Masaaki Higuchi, Tomoyuki Suwa, Takashi Aratani, Tatsufumi Hamada, Akinobu Teramoto, Takeo Hattori, Shigetoshi Sugawa, Tadahiro Ohmi, Seiji Shinagawa, Hiroshi Nohira, and Eiji Ikenaga, *Tohoku University, Japan*

11:50 AM **P.14 – Silicon substrate surface orientation (100) and (110) impact on negative and positive bias temperature instability on hafnium silicate TiN metal gated MOSFETs,** M. Aoulaiche, M. Houssa, S. De Gendt, G. Groeseneken, H. Maes, and M.M. Heyns, *IMEC, Belgium*

11:53 AM **P.15 – The Instability of the SiGe/Si-Hetero-Interface in Hetero-MOSFETs due to Bias Stress,** Toshiaki Tsuchiya, Seiji Mishima, Masao Sakuraba, and Junichi Murota, *Shimane University, Japan*

11:56AM **P.16– Charge Trapping and Detrapping in Ultra-thin (EOT<1nm) SiO_2/HfO_2 Gate Dielectrics,** Yanli Zhang, Zhian Jin, Gan Wang, and Marvin H. White, *Lehigh University*

11:59AM **Adjourn for Lunch**

Session 3 – NVRAM and High-κ

Thursday, December 7, 2006
Session Chair: R. Nemanich

1:30 PM **Opening Remarks**

1:35 PM **3.1 – *Invited* - Embedded FRAM Technology,** T. Moise, *Texas Instruments*

2:10 PM **3.2 - Barrier Engineering for Non-Volatile Memory Application**, Yanxiang Liu, Sun Il Shim, Frank C. Yeh, X. W. Wang, and T. P. Ma, *Yale University*

2:30 PM **3.3 - Physical and Electrical Characterization of $HfSi_x/HfO_2$ Gate Stacks for High-Performance nMOSFET Application**, S. Yoshida, Y. Kita, T. Ando, K. Tai, H. Iwamoto, T. Shimura, H. Watanabe, and K. Yasutake, *Osaka University, Japan*

Poster Session III

Thursday, December 7, 2006
Session Chair: P. Lenahan

2:50 PM **P.17 – Direct observation of resistive memory switching in NiO thin film,** Sejin Kim, Jung-Bin Yun, Sunae Seo, Myoung-Jae Lee, Seung-Eon Ahn, Dong-Chul Kim, In-Kyeoug Yoo, Seungbum Hong, and Hyunjung Shin, *Kookmin University, S. Korea*

2:53 PM **P.18 - Improved Performance of Nonvolatile Memory Device with Band Offset Tuning in HfAlO Charge-Trapping Layer**, P.-H. Tsai, K.-S. Chang-Liao, C.-Y. Liu, T.-K. Wang, P. J. Tzeng, L.S. Lee, and M.-J. Tsai, *National Tsing Hua University, Taiwan*

2:56 PM **P.19 - Electrical Performance of Damascene Metal Gate MOSFETs with Crystalline Gd_2O_3 Gate Dielectric,** R. Endres, Y. Stefanov, and U. Schwalke, *Darmstadt University of Technology, Germany*

2:59 PM **P.20 - Influence of Si substrate orientation on growth and electrical properties of epitaxial Gd_2O_3 thin films for high-κ application,** H. J. Osten, Arpuba Laha, and A. Fissel, *University of Hannover, Germany*

3:02 PM **P.21 - Intrinsic Electronically-Active Defects in Transition Metal Elemental Oxides,** G. Lucovsky, S. Lee, H. Seo, L. B. Fleming, M. D. Ulrich, and J. Lüning, *NC State University*

3:05 PM **P.22 - Ta-Sc-N intermixed metal gate structure for low work function metal gate for future MOSFET technology** Musarrat Hasan, Hokyoung Park, Hyejung Choi, Dongsoo Lee and Hyunsang Hwang, *Gwangju Institute of Science and Technology, S. Korea*

3:08 PM **P.23 – Microstructure Evolution of Tantalum Nitride films deposited by Plasma Enhanced Atomic Layer Deposition for Gate Electrode Application,** Raghavasimhan Sreenivasan, Paul McIntyre, and Krishna Saraswat, *Stanford University*

3:11 PM **BREAK**

Session 4 – Dielectrics on High Mobility Substrates I

Thursday, December 7, 2006
Session Chair: K. Ahmed

3:35 PM **Opening Remarks**

3:40 PM **4.1 - CV characterization of Ge/HfO_2 MOSFETs passivated with a thin epitaxial Si layer**, B. De Jaeger, B. Kaczer, M. A. Pourghaderi, M. Houssa, M. Meuris, and M. Heyns, *IMEC, Belgium*

4:00 PM **4.2 - Fabrication of Ge MOS Capacitors on Si Substrates using Selective Ge Epitaxy and Surface Passivation Techniques,** Jungwoo Oh, Cristiano Krug, Prashant Majhi, Rusty Harris, Hsing-Huang Tseng, Paul Kirsch, and Raj Jammy, *Sematech*

Poster Session IV

Thursday, December 7, 2006
Session Chair: M. Takayangi

4:20 PM **P.24 – Metal Gate HfO_2 MOS Structures on GaAs Substrate with SiGe Interface Passivation Layer**, InJo Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, and Jack C. Lee, *University of Texas at Austin*

4:23 PM **P.25 – Ge-MIS interface states studied by conductance technique,** Noriyuki Taoka, Keiji Ikeda, Yoshimi Yamashita, Masatomi Harada, Toyoji Yamamoto, Naoharu Sugiyama, and Shin-ichi Takagi, *MIRAI-ASRC, Japan*

4:26 PM **P.26 – Interface state Density measurement at GeO_xN_y-Ge interface for Ge MIS Applications**, Abhijit Pethe and Krishna Saraswat, *Stanford University*

4:29 PM **P.27 – In-situ studies of initial oxidation of bare InAs surfaces and oxide/InAs interfaces,** C. L. Chang, V. Shutthanandan, and S. Ramanathan, *Harvard University*

4:32 PM **P.28 – The Effects of Germanium Interfacial Passivation Layer Thickness on Electrical Characteristics of HfO_2 MOSCAP on GaAs Substrate,** Hyoung-Sub Kim, Injo Ok, Manhong Zhang, Feng Zhu, Lu Yu, Tackhwi Lee, and Jack C. Lee, *University of Texas, Austin*

4:35 PM **P.30 – Investigation of charge trapping properties of high-κ on GaAs with silicon interface passivation layer,** Feng Zhu, S. Koveshnikov, I. Ok, H. S. Kim, M. Zhang, V. Tokranov, M. Yakimov, S. Oktyabrsky, W. Tsai and J. C. Lee, *University of Texas, Austin*

4:38PM **4.3 – *Invited*** – **Opportunities for Advanced Technology in Telecommunications,** L. Smarr, *Director, California Institute for Telecommunications and Information Technology*

4:58 PM **Adjourn**

7 – 10 P.M. Thursday Evening ***Poster Reception and Buffet***
Birch Aquarium (transportation provided)

Session 5 – Theory

Friday, December 8, 2006
Session Chair: G. Reimbold

8:00 AM **Morning Announcements**

8:05 AM **5.1 *Invited* – When defects approach a device size,** A. Shluger, *University College London, UK*

8:40 AM **5.2 Atomistic Model Structure of the Si(100)-HfO_2 Interface Generated by Ab Initio Molecular Dynamics,** P. Broqvist and A. Pasquarello, *ITP EPFL, Switzerland*

9:00 AM **5.3 Remote Phonon Scattering in Si and Ge Substrates with SiO_2 and HfO_2 Gate Insulators: Does the Electron Mobility Determine Short Channel Performance?** T. P. O'Regan and M. V. Fischetti, *University of Massachusetts*

9:20 AM **5.4 Bonding and Work Function Control at Metal – HfO_2 interfaces,** J. Robertson and K. Tse, *Cambridge University, UK*

9:40 AM **BREAK**

Session 6 – High-κ II

Friday, December 8, 2006
Session Chair: H. Watanabe

10:10 AM **Opening Remarks**

10:15 AM **6.1 *Invited* - What happens at high-κ dielectric interfaces?** K. Shiraishi, *University of Tsukuba, Japan*

10:50 AM **6.2 Comparison of ZrO_2/Ge(100) and HfO_2/Ge(100) Bonding and Electronic Structure,** Tyler J. Grassman, Sarah R. Bishop, Andrew C. Kummel, Chi On Chui and Wilman Tsai, *University of California, San Diego*

11:10 AM **6.3 Effect of Thermal Dry Oxidation on Stacked TiN/HfO_2/SiO_2/Si Structures,** J.-J. Ganem, I. Trimaille, J. V. Bardeleben, J.-L. Cantin and V. Narayanan, *University of Pierre et Marie Curie, France*

11:30 AM **6.4 Criticality of controlling oxygen incorporation into HfO_2/Si/GaAs gate stacks,** M. H. Zhang, F. Zhu , I. J. Ok , H. S. Kim, L. Yu, M. Oye, J. Hurst, B. Cobb, S. Lewis, A. Holmes and Jack C. Lee, *University of Texas at Austin*

11:50 AM **Adjourn – Technical Committee / Invited Speaker Luncheon**

3:00 – 5:00 PM **Optional Rump Sessions – Topics TBD**

7 – 10 P.M. Friday Evening ***Conference Banquet and Limerick Contest***

Session 7 – High-κ III

Saturday, December 9, 2006
Session Chair: D. Triyoso

8:20 AM **Morning Announcements**

8:25 AM **7.1 *Invited* – The search for a high performance metal gate/high-κ n-mosfet,** S. Guha, *IBM*

9:00 AM **7.2 - The origin of V_{FB} shift in Metal/HfLaO/SiO_2/Si systems,** Yoshiki Yamamoto, Koji Kita, Kentaro Kyuno and Akira Toriumi, *University of Tokyo, Japan*

9:20 AM **7.3 - Nature and thermal stability of the (100)Si/$LaAlO_3$ interface probed by paramagnetic point defect,** A. Stesmans, K. Clémer, V. V. Afanas'ev, L. F. Edge and D. G. Schlom, *University of Leuven, Belgium*

9:40 AM **7.4 – Internal photoemission from Si into amorphous and epitaxial oxide insulators: Sc_2O_3, Lu_2O_3, and $LaLuO_3$,** V. V. Afanas'ev, S. Shamuilia, A. Stesmans, L. F. Edge, W. Tian, D. G. Schlom, J. M. J. Lopes, M. Roeckerath, and J. Schubert, *University of Leuven, Belgium*

10:00 AM **BREAK**

Session 8 – Dielectrics on High Mobility Substrates II

Saturday, December 9, 2006
Session Chair: M. Frank

10:20 AM **Opening Remarks**

10:25 AM **8.1 *Invited* – Opportunities and Challenges for high-κ/III-V MOSFETs,** P. Ye, *Purdue University*

11:00 AM **8.2 – Improvement of interfacial characteristics for Si-passivated Ge/HfO_2 MOSFETs,** K. Martens, B. Kaczer, P. Zimmermann, B. De Jaeger, M. Meuris, G. Groeseneken, and H. Maes, *IMEC, Belgium*

11:20 AM **8.3 – Improved passivation and characterization of the Ge/HfSiO interface enabling surface channel Ge pFETs,** H. J. Na, C. Krug, S. Joshi, D. Heh, P. D. Kirsch, R. Choi, B. H. Lee, R. Jammy, S. K. Banerjee, and J. C. Lee, *University of Texas at Austin*

11:40 AM **8.4 – A Reliable pMOSFET SiGe S/D Engineering with Very Good Hot Carrier and NBTI Reliabilities for 65nm Node and Beyond CMOS Device Applications,** Steve S. Chung, D. C. Huang, Y. J. Tsai, C. S. Lai, C. H. Tsai, P. W. Liu, Y. H. Lin, C. T. Tsai, G. H. Ma, S. C. Chien, and S. W. Sun, *National Chiao Tung University, Taiwan*

12:00 PM **Closing Remarks**