

SISC 2010

**41st IEEE
Semiconductor Interface
Specialists Conference**

December 2-4, 2010 (Tutorial: Dec 1)
The Catamaran Hotel, San Diego, CA
www.ieeesisc.org



CONFERENCE PROGRAM

General Chair: Martin Frank

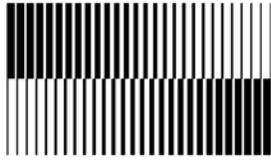
Technical Chair: John Robertson

Arrangements Chair: Michel Houssa

Ex-Officio: Dina Triyoso

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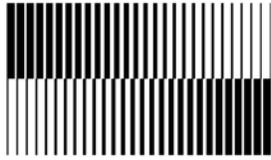
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SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, “MOS Physics and Technology,” published by Wiley Interscience.

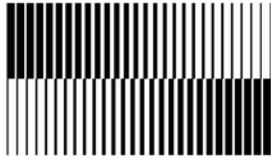
The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author or either an oral or poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

Winner of the 2009 SISC Ed Nicollian Award for Best Student Paper:

Jacopo Franco, imec, Leuven, and KU Leuven, Belgium

“Impact of Si-Passivation Thickness and Processing
on NBTI Reliability of Ge and SiGe pMOSFETs”

with B. Kaczer, A. Stesmans, V. V. Afanas'ev, K. Martens,
M. Aoulaiche, T. Grasser, J. Mitard, G. Groeseneken



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Wednesday Evening Tutorial

Wednesday, December 1, 2010, 8:00 PM

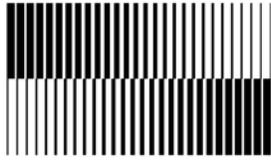
First introduced at SISC 2008, the Wednesday evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

Dr. Matthias Passlack

TSMC Europe, Leuven, Belgium

“Interface state analysis on non-silicon semiconductors and the role of heterostructures”

Non-silicon semiconductors are considered as alternative channel materials to enable and facilitate CMOS scaling beyond silicon. Both materials comprising column IV (e.g. Ge) and compounds formed from columns III and V (e.g. Ga, In, As, Sb) elements of the periodic table are of interest. Electrical interface characterization which has been traditionally silicon centric needs to embrace their different electronic properties to ensure accurate interface state analysis and to exploit new opportunities. In a first part, this tutorial will propose a flow chart for admittance-voltage characterization of interfaces formed between dielectrics and alternate channel materials commencing with basic physics and concluding with selection of measurements parameters and models for trap quantification. During a second part, an interface characterization technique suitable for direct bandgap semiconductors and relying on carrier recombination (photoluminescence intensity) is discussed. Finally, exploitation of heterostructures at dielectric/semiconductor interfaces and related implications for the impact of interface states on device performance are examined.



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Conference Agenda Overview

Wednesday, December 1, 2010

Registration	6:00 PM – 8:00 PM
Hospitality Room	8:00 PM – Midnight
Evening Tutorial	8:00 PM – 9:30 PM

Thursday, December 2, 2010

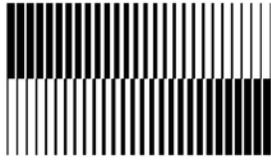
Registration	8:00 AM – 5:00 PM
Session 1 – High-k Oxides	8:00 AM – 9:30 AM
Poster Preview Session 1 - High-k Oxides	9:30 AM – 9:55 AM
Session 2 - III-V's	10:25 AM – 11:45 AM
Poster Preview Session 2 - Ge, III-Vs	11:45 AM – 12:05 PM
Session 3 - Devices	1:30 PM – 2:30 PM
Poster Preview Session 3 - III-Vs, Memory	2:30 PM – 2:50 PM
Session 4 - Memory	3:20 PM – 5:00 PM
Poster Preview Session 4 - Memory, Reliability, Interfaces	5:00 PM – 5:20 PM
Poster Reception	7:00 PM – 10:00 PM
Hospitality Room	9:30 PM – Midnight

Friday, December 3, 2010

Registration	8:00 AM – Noon
Session 5 - III-Vs	8:00 AM – 10:00 AM
Session 6 - Ge	10:30 AM – 12:30 PM
Technical Committee / Invited Speaker Luncheon	12:30 PM – 2:00 PM
Rump Session	3:00 PM – 5:30 PM
Conference Banquet and Limerick Contest	7:00 PM – 10:00 PM
Hospitality Room	10:00 PM – Midnight

Saturday, December 4, 2010

Session 7 - Oxides	8:00 AM – 10:00 AM
Session 8 - High-k Oxides	10:30 AM – 12:35 PM



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Conference Program

Session 1 - High-k Oxides

Thursday, December 2, 2010

Session Chair: M. M. Frank

- 8:00 AM Welcome and opening remarks
- 8:15 AM 1.1 *Invited - Materials and Processes for High-k Metal Gate Stacks for 28 nm and Beyond*, P. Kirsch, *SEMATECH*
- 8:50 AM 1.2 - **Kinetics of Interfacial Layer Scavenging and Dipole Formation for Ultimate Scaling of Hf-based High-k Gate Dielectrics**, T. Ando¹, H. Arimura², R. Haight¹, M. Copel¹, H. Watanabe², and V. Narayanan¹, ¹*IBM*, ²*Osaka University, Japan*
- 9:10 AM 1.3 - **Study of Trap Distribution in Ultra-thin Dielectrics by Inelastic Electron Tunneling Spectroscopy**, Z. Liu, S. Cui, and T.P. Ma, *Yale University*

Poster Preview Session 1 - High-k Oxides

Thursday, December 2, 2010

Session Chair: M. M. Frank

- 9:30 AM Poster Introduction
- 9:35 AM P.1 - **Passivation of High-k Bulk and Interface Defects by Incorporating La into Hf-silicate and its Impact on Carrier Mobility**, M. Saeki, H. Arimura, N. Kitano, T. Hosoi, T. Shimura, and H. Watanabe, *Osaka University, Japan*
- P.2 - **Interfacial Design of High-k/Ge Gate Stacks with ZrO₂ Dielectrics for Scaled Ge-based MOS Devices**, T. Hosoi¹, G. Okamoto¹, I. Hideshima¹, A. Kasuya¹, K. Kutsuki¹, J. Harries², A. Yoshigoe², Y. Teraoka², T. Shimura¹, and H. Watanabe¹, ¹*Osaka University, Japan*, ²*Japan Atomic Energy Agency, Japan*

P.3 - Innovative Characterization Methods to Investigate High-k Metal Gate Stack Work Function, M. Charbonnier¹, C. Leroux¹, G. Ghibaudo², F. Martin¹, H. Grampeix¹, F. Boulanger¹, and G. Reimbold¹, ¹*CEA-LETI-MINATEC, France*, ²*IMEP Minatec, France*

P.4 - First Principles Investigation of Flat-Band Shift in a Lanthanum Doped Gate Stack Si/SiO₂/HfO₂:La₂O₃, E. Nadimi¹, R. Ötting², P. Plänitz², M. Trentzsch³, T. Kelwing³, R. Carter³, and C. Radehaus², ¹*Technische Universität Chemnitz, Germany*, ²*GWT-TUD GmbH, Germany*, ³*Global Foundries, Germany*

P.5 - The Role of Oxygen in High-k/SiO₂ Interfacial Dipoles on the Schottky Barrier Height at Metal-Semiconductor Interfaces, B. E. Coss¹, W.-Y. Loh², P. Majhi², R. Jammy², R. M. Wallace¹, and J. Kim¹, ¹*UT Dallas*, ²*SEMATECH*

P.6 - A Comparative Study on the Effect of Post Deposition Annealing on the Physical Property and Electrical Reliability of Hf_{1-x}Zr_xO_y Gate Dielectrics, H.-S. Jung^{1,2}, S. Y. Lee¹, S.-H. Rha¹, H. K. Kim¹, Y. J. Chung¹, J.-M. Park², W.-H. Kim², M.-W. Song², N.-I. Lee², and C. S. Hwang¹, ¹*Seoul National University, Korea*, ²*Samsung, Korea*

P.7 - Charge Trapping in LaLuO₃ MOS Capacitors Using a New 3-Pulse CV Technique, N. Sedghi¹, W. Davey¹, I. Z. Mitrovic¹, S. Hall¹, J. M. J. Lopes², and J. Schubert², ¹*University of Liverpool, UK*, ²*Research Centre Jülich, Germany*

P.8 - Integration of LaLuO₃/TiN Gate Stack in Strained-SiGe p-MOSFETs, W. Yu^{1,2}, B. Zhang^{1,2}, Q. T. Zhao¹, J.-M. Hartmann³, D. Buca¹, A. Nichau¹, J. M. J. Lopes¹, J. Schubert¹, K. Bourdelle⁴, X. Wang², and S. Mantl¹, ¹*Research Centre Jülich, Germany*, ²*Chinese Academy of Sciences, China*, ³*CEA-LETI-MINATEC, France*, ⁴*SOITEC, France*

P.9 - Energy Spin Dependent Trap Assisted Tunneling in Gd₂O₃ Dielectrics, B. C. Bittel¹, P. M. Lenahan¹, E. Lipp², and M. Eizenberg², ¹*The Pennsylvania State University*, ²*Technion-Israel Institute of Technology, Israel*

P.10 - Monolayer Passivation of Ge(100) Surface via Nitridation and Oxidation, J. S. Lee, S. R. Bishop, T. Kaufman-Osborn, E. A. Chagarov, and A. C. Kummel, *UC San Diego*

P.11 - Crystallization of Thick Amorphous GeO₂ on Ge to α -quartz Structure - Experimental Evidence and Crystallization Model, S. K. Wang¹, K. Kita^{1,2}, T. Nishimura^{1,2}, K. Nagashio^{1,2}, and A. Toriumi^{1,2}, ¹*The University of Tokyo, Japan*, ²*JST-CREST, Japan*

P.12 - Impact of Low Temperature O₂ Annealing for Stabilizing LaLuO₃/Ge Gate Stacks without Additional Interface Layer Formation, T. Tabata^{1,2}, C. H. Lee¹, T. Nishimura^{1,2}, K. Kita^{1,2}, and A. Toriumi^{1,2}, ¹*The University of Tokyo, Japan*, ²*JST-CREST, Japan*

9:55 AM Break

Session 2 - III-V's
Thursday, December 2, 2010
Session Chair: R. M. Wallace

- 10:25 AM Opening remarks
- 10:30 AM 2.1 **Invited - High Performance InGaAs Quantum Well FETs with High-k Dielectrics**, M. Radosavljevic, *Intel*
- 11:05 AM 2.2 - **Calculation of Electron and Hole Mobility in Inversion Layers of MOS Systems with III-V Channels and High-k Insulators**, T. O'Regan, Y. Zhang, and M. V. Fischetti, *University of Massachusetts Amherst*
- 11:25 AM 2.3 - **Self-Aligned Gate-First In_{0.7}Ga_{0.3}As N-MOSFETs with an InP Capping Layer for Performance Enhancement**, X. Gong, Ivana, H.-C. Chin, Z. Zhu, and Y.-C. Yeo, *National University of Singapore, Singapore*

Poster Preview Session 2 - Ge, III-Vs
Thursday, December 2, 2010
Session Chair: R. M. Wallace

- 11:45 AM P.13 - **Atomic Structures, Models, and Band Offsets of Ge:GeO:GeO₂ Interfaces**, L. Lin¹, J. Robertson¹, and K. Xiong², ¹*University of Cambridge, UK*, ²*UT Dallas*
- P.14 - **Energetics of Hydrogen in Ge and GeO₂ Interfaces**, K. Xiong¹, L. Lin², J. Robertson², and K. Cho¹, ¹*UT Dallas*, ²*University of Cambridge, UK*
- P.15 - **Fermi Level De-pinning of Aluminium Contacts to Germanium Using Thin ALD Al₂O₃ Interfacial Layer**, D. R. Gajula¹, D. Tantraviwat¹, Y. H. Low¹, P. T. Baine¹, M. Modreanu², B. M. Armstrong¹, and D. W. McNeill¹, ¹*Queen's University Belfast, UK*, ²*Tyndall National Institute, Ireland*
- P.16 - **ALD Temperature Dependence of Slow Trap Properties at ALD-Al₂O₃/InP Interfaces**, N. Taoka¹, M. Yokoyama¹, S. H. Kim¹, T. Hoshii¹, R. Iida¹, S. Lee¹, R. Suzuki¹, Y. Urabe², N. Miyata², T. Yasuda², H. Yamada³, N. Fukuhara³, M. Hata³, M. Takenaka¹, and S. Takagi¹, ¹*The University of Tokyo, Japan*, ²*National Institute of Advanced Industrial Science and Technology (AIST), Japan*, ³*Sumitomo Chemical Co., Japan*
- P.17 - **Passivation of InGaAs and InAs by ALD Precursors**, E. A. Chagarov¹, J. B. Clemens¹, M. Holland², R. Droopad³, J. Shen¹, and A. C. Kummel¹, ¹*UC San Diego*, ²*University of Glasgow, UK*, ³*Texas State University-San Marcos*
- P.18 - **Interfacial Layer Defect Response of Metal/High-k/GaAs C-V Characteristics**, A. M. Sonnet, C. L. Hinkle, and E. M. Vogel, *UT Dallas*

P.19 - Low Temperature ALD Growth of Al₂O₃ Gate Dielectric for GaSb pMOSFETs, M. Xu and P. D. Ye, *Purdue University*

P.20 - Band Alignment at Interfaces of (100)InP with Atomic-Layer Deposited Al₂O₃, V. V. Afanas'ev¹, Hsing-Yi Chou¹, A. Stesmans¹, D. Lin², P. K. Hurley³, and S. B. Newcomb⁴, ¹*KU Leuven, Belgium*, ²*imec, Belgium*, ³*Tyndall National Institute, Ireland*, ⁴*Glebe Scientific Ltd., Ireland*

P.21 - Infrared Spectroscopic Characterization of Wet Chemical Processes and Trimethylaluminum Treatments of III-V Surfaces, W. Cabrera, and Y. Chabal, *UT Dallas*

P.22 - In-situ Atomic Layer Deposition-Al₂O₃ on Freshly MBE Grown GaAs, M. L. Huang¹, Y. H. Chang¹, P. Chang¹, C. A. Lin¹, J. Kwo¹, T.-W. Pi², and M. Hong¹, ¹*National Tsing Hua University, Taiwan*, ²*National Synchrotron Radiation Research Center, Taiwan*

P.23 - Interfacial Electronic Structure of Ga₂O₃(Gd₂O₃) Grown on n-Ge Studied by Synchrotron Radiation Photoemission, T.-W. Pi¹, W. C. Lee², M. L. Huang², L. K. Chu², T. D. Lin², T. H. Chiang², Y. C. Wang², J. Kwo², and M. Hong², ¹*National Synchrotron Radiation Research Center, Taiwan*, ²*National Tsing Hua University, Taiwan*

P.24 - InGaAs Channel IFQW-MOSFET: Effect of InAlAs Interfacial Passivation Layer and (NH₄)₂S Treatment on the Electrical Behavior, A. Alian^{1,2}, C. Merckling¹, G. Brammertz¹, M. Meuris¹, K. De Meyer^{1,2}, M. Heyns^{1,2}, and T. Y. Hoffmann¹, ¹*imec, Belgium*, ²*KU Leuven, Belgium*

12:05 AM Adjourn for lunch

Session 3 - Devices

Thursday, December 2, 2010

Session Chair: S. Takagi

1:30 PM Opening remarks

1:35 PM 3.1 *Invited - Nanowire Transistors: Performance Limits, Strain Engineering, Reduction of Parasitic Resistance*, Y.-C. Yeo, *National University of Singapore, Singapore*

2:10 PM 3.2 - **InAs and In_{0.7}Ga_{0.3}As Buried Channel MOSFETs with ALD Gate Dielectrics**, F. Xue, H. Zhao, Y. Chen, Y. Wang, F. Zhou, and J. Lee, *UT Austin*

Poster Preview Session 3 - III-Vs, Memory

Thursday, December 2, 2010

Session Chair: X. Garros

- 2:30 PM P.25 - **Charged Defect Quantification in Pt/Al₂O₃/In_{0.53}Ga_{0.47}As/InP MOS Capacitors**, R. D. Long^{1,2}, B. Shin², S. Monaghan¹, K. Cherkaoui¹, J. Cagnon³, S. Stemmer³, P. C. McIntyre² and P. K. Hurley¹, ¹*Tyndall National Institute, Ireland*, ²*Stanford University*, ³*UC Santa Barbara*
- P.26 - **Improved Electrical Characteristics of ALD HfO₂, Al₂O₃ Based n-Channel MOSFETs on InP Substrate with Postgate SF₆ Plasma Treatment**, Y. Wang, Y.-T. Chen, H. Zhao, F. Xue, F. Zhou, and J. C. Lee, *UT Austin*
- P.27 - **Origin of Interfacial Gap States in Ga₂O₃ Layer Grown on GaAs Surface and Interface Passivation by F and Gd**, W. Wang, R. M. Wallace, and K. Cho, ¹*UT Dallas*
- P.28 - **The Effect of Graphite Surface Condition on Composition and Morphology of ALD Al₂O₃**, A. Pirkle¹, S. McDonnell¹, B. Lee¹, J. Kim¹, L. Colombo², and R. M. Wallace¹, ¹*UT Dallas*, ²*Texas Instruments*
- P.29 - **First Principles Study of the Energetics of Ideal GaAs Surfaces and Adsorption of Al and O as a Function of Surface Orientation**, G. Hegde, G. Klimeck, and A. Strachan, *Purdue University*
- P.30 - **Transient Dielectric Polarization of Al₂O₃ Block Layer as a Possible Origin for the Temperature Dependence of Program Characteristics in SANOS Devices**, H. Kusai, Y. Higashi, S. Fujii, J. Fujiki, N. Yasuda, and K. Muraoka, *Toshiba, Japan*
- P.31 - **Low-Voltage, High-Speed Charge-Trap Memory Cell with Excellent High Temperature Retention**, J. Yang¹, X. Sun¹, S. Cui¹, T. P. Ma¹, L. Kornblum², and M. Eizenberg², ¹*Yale University*, ²*Technion-Israel Institute of Technology, Israel*
- P.32 - **Voltage- and Temperature- Dependent Reliability of the Set/Reset Switching in TiN/HfO₂/Pt Resistive RAM**, Y. Y. Chen^{1,2}, L. Goux¹, L. Pantisano¹, X. P. Wang¹, R. Degraeve¹, B. Govoreanu¹, M. Jurczak¹, D. J. Wouters^{1,2}, L. Altimime¹, and G. Groeseneken^{1,2}, ¹*imec, Belgium*, ²*KU Leuven, Belgium*
- P.33 - **Noise Analysis Based Model of Unstable Parameters and Solution for Achieving Improved Characteristics in Resistance Random Access Memory**, D. S. Lee, J.-M. Lee, M. S. Jo, J. B. Park, M. Siddik, I. S. Kim, K. A. Seo, J. H. Shin, K. P. Biju, and H. Hwang, *Gwangju Institute of Science and Technology, Korea*
- P.34 - **A Novel PEALD Tunnel Dielectric for Three-Dimensional Non-Volatile Charge-Trapping Technology**, A. Cacciato¹, L. Breuil¹, H. Dekkers¹, M. Zahid¹, G. S. Kar¹, J. L. Everaert¹, G. Schoofs¹, X. Shi¹, G. Van den Bosch¹, M. Jurczak¹, I. Debusschere¹, J. Van Houdt¹, A. Cockburn², L. Date², L.-Q. Xia², M. Le², and W. Lee², ¹*imec, Belgium*, ²*Applied Materials*

P.35 - Engineering SiGe Buried Channel for Charge-Trapping Flash Memory Devices, K.-S. Chang-Liao, L.-J. Liu, Z.-H. Ye, W.-C. Keng, and T.-K. Wang, *National Tsing Hua University, Taiwan*

P.36 - Compositional Study of BaSrTiO Thin Films for Memory Application, K. Tomida¹, K. Opsomer^{1,2}, C. Vrancken¹, B. Kaczer¹, M. A. Pawlak¹, M. I. Popovici¹, J. Swerts¹, S. V. Elshocht¹, C. Detavernier², M. S. Kim¹, I. Debusschere¹, L. Altimime¹, and J. A. Kittl¹, ¹*imec, Belgium*, ²*Ghent University, Belgium*

P.37 - Non-Volatile Memory Effect in Carbon Nanotube Field-Effect Transistors: Charge Trapping in Al_xO_y High-k Dielectrics Made from Sacrificial Metal Catalyst, L. Rispal, and U. Schwalke, *Technische Universität Darmstadt, Germany*

2:50 PM Break

Session 4 - Memory

Thursday, December 2, 2010

Session Chair: J. Van Houdt

3:20 PM Opening remarks

3:25 PM 4.1 *Invited - BiCS Flash Memory Technology*, A. Nitayama, *Toshiba, Japan*

4:00 PM 4.2 - **Effect of Area Scaling on Switching Uniformity of WO_x RRAM**, S. Kim, K. P. Biju, M. Jo, S. Jung, J. Park, J. Lee, W. Lee, J. Shin, S. Park, and H. Hwang, *Gwangju Institute of Science and Technology, Korea*

4:20 PM 4.3 - **Universal Switching and Noise Characteristics of Nanofilaments in Metal-Oxide RRAMs**, D. Ielmini, F. Nardi, and C. Cagli, *Politecnico di Milano, Italy*

4:40 PM 4.4 - **Atomistic Design of Interface Layer for MONOS-Type Memories with High Program/Erase Cycle Endurance**, K. Yamaguchi¹, A. Otake¹, K. Kamiya², Y. Shigeta², and K. Shiraishi¹, ¹*University of Tsukuba, Japan*, ²*University of Hyogo, Japan*

Poster Preview Session 4 - Memory, Reliability, Interfaces

Thursday, December 2, 2010

Session Chair: D. Ielmini

5:00 PM P.38 - **Bipolar Resistive Switching Characteristics of HfO₂ Based MIM Devices**, Ch. Walczyk¹, D. Walczyk¹, T. Schroeder¹, M. Lukosius¹, M. Fräschke¹, E. Miranda², B. Tillack¹, and Ch. Wenger¹, ¹*IHP, Germany*, ²*Universitat Autònoma de Barcelona, Spain*

P.39 - **A Study of the HRS and LRS Temperature Behavior of Pt/HfO₂/Pt Based Oxide Resistive RAM**, P. Lorenzi, P. Singh, J. Buckley, V. Jousseau, A. Fantini, J. F. Nodin, A. Persico, S. Tirano, H. Grampeix, G. Betti Beneventi, L. Perniola, and B. De Salvo, *CEA-LETI-MINATEC, France*

P.40 - Band Alignment of Vanadium Oxide as an Interlayer in a Hafnium Oxide and Silicon Gate Stack Structure, C. Zhu, F. Tang, X. Liu, and R. J. Nemanich, *Arizona State University*

P.41 - Si Tunneling Field Effect Transistor with Highly Strained-Ge Source on Si(110) Substrate, G. Han, P. Guo, Y. Yang, C. Zhan, Q. Zhou, and Y.-C. Yeo, *National University of Singapore, Singapore*

P.42 - Implications of Channel Hot Carrier Degradation in Si_{0.45}Ge_{0.55} pMOSFETs, J. Franco^{1,2}, B. Kaczer¹, J. Mitard¹, G. Eneman^{1,2,3}, Ph. J. Roussel¹, F. Crupi⁴, T. Grasser⁵, L. Witters¹, T. Y. Hoffmann¹, and G. Groeseneken^{1,2}, ¹*imec, Belgium*, ²*KU Leuven, Belgium*, ³*FWO Vlaanderen, Belgium*, ⁴*Università della Calabria, Italy*, ⁵*TU Wien, Austria*

P.43 - Inherent Si Dangling Bond Defects at the Thermal (110)Si/SiO₂ Interface, K. Keunen, A. Stesmans, and V. V. Afanas'ev, *KU Leuven, Belgium*

P.44 - Depth Localization of Trapped Holes in SiON after Positive and Negative Gate Stress, M. Toledano-Luque¹, B. Kaczer², Ph. J. Roussel², R. Degraeve², J. Franco^{2,3}, T. Kauerauf², T. Grasser⁴, and G. Groeseneken^{2,3}, ¹*Universidad Complutense de Madrid, Spain*, ²*imec, Belgium*, ³*KU Leuven, Belgium*, ⁴*TU Wien, Austria*

P.45 - Interfacial Trap Density-of-States in Amorphous-InGaZnO-based Thin-Film Transistors Measured by Photo-Excited Charge-Collection Spectroscopy, Y.-G. Chang^{1,2}, D.-H. Kim², G. Ko¹, K. Lee¹, and S. Im¹, ¹*Yonsei University, Korea*, ²*LG Display, Korea*

P.46 - Source-Channel Interface Engineering for Tunneling Field Effect Transistor (TFET) with SiGe Source: Insertion of Strained Si:C Layer for Enhancement of Tunneling Current, P. Guo, G. Han, Y. Yang, X. Gong, C. Zhan, and Y.-C. Yeo, *National University of Singapore, Singapore*

P.47 - Energy Band Structure of Thermally Grown SiO₂/4H-SiC Interfaces and Its Modulation Induced by Post-Oxidation Treatments, T. Kirino¹, Y. Kagei¹, A. Yoshigoe², Y. Teraoka², S. Mitani³, Y. Nakano³, T. Nakamura³, T. Hosoi¹, T. Shimura¹, and H. Watanabe¹, ¹*Osaka University, Japan*, ²*Japan Atomic Energy Agency, Japan*, ³*Rohm Co., Japan*

P.48 - Bias-Temperature Instabilities in 4H-SiC MOS Capacitors, E. X. Zhang¹, C. X. Zhang¹, D. M. Fleetwood¹, R. D. Schrimpf¹, S. Dhar², and S.-H. Ryu², ¹*Vanderbilt University*, ²*Cree*

P.49 - Characterization of Tungsten-Filled Through-Silicon Via, D. H. Triyoso, T. B. Dao, and V. Adams, *Freescale Semiconductor*

5:25 PM Adjournal

7:00 PM – 10:00 PM Poster Reception

Session 5 - III-Vs

Friday, December 3, 2010

Session Chair: A. Kummel

- 8:00 AM Morning announcements
- 8:05 AM 5.1 *Invited - In-situ Studies of High-k Oxide Growth on III-V Semiconductors*, C. L. Hinkle, *UT Dallas*
- 8:40 AM 5.2 - **Interface As Oxides as Indicator of Carrier Scattering in Al₂O₃/InGaAs MISFETs on (111)A and (100) surfaces**, N. Miyata¹, Y. Urabe¹, H. Ishii¹, T. Itatani¹, T. Maeda¹, T. Yasuda¹, H. Yamada², N. Fukuhara², M. Hata², M. Yokoyama³, N. Taoka³, M. Takenaka³, and S. Takagi³, ¹*National Institute of Advanced Industrial Science and Technology (AIST), Japan*, ²*Sumitomo Chemical Co., Japan*, ³*The University of Tokyo, Japan*
- 9:00 AM 5.3 - **Interface Composition of Atomic Layer Deposited HfO₂ and Al₂O₃ Thin Films on InAs Studied by X-ray Photoemission Spectroscopy**, R. Timm, M. Hjort, A. Fian, C. Thelander, E. Lind, J. N. Andersen, L.-E. Wernersson, and A. Mikkelsen, *Lund University, Sweden*
- 9:20 AM 5.4 - **Investigation of GaSb Interface Evolution by *in situ* X-ray Photoelectron Spectroscopy**, A. P. Kirk, D. M. Zhernokletov, S. McDonnell, J. Kim, and R. M. Wallace, *UT Dallas*
- 9:40 AM 5.5 - **Origin of Schottky Barrier Height Shifts by Inserting Thin Insulator Layers**, Y. Guo¹, S. J. Clark², L. Lin¹, and J. Robertson¹, ¹*University of Cambridge, UK*, ²*Durham University, UK*
- 10:00 AM Break

Session 6 - Ge

Friday, December 3, 2010

Session Chair: A. Stesmans

- 10:30 AM Opening remarks
- 10:35 AM 6.1 *Invited - Understanding of GeO₂ Material Properties for Advanced Ge MIS Stacks*, K. Kita, *The University of Tokyo, Japan*
- 11:10 AM 6.2 - **Improvement of EOT Scalability in Metal-Gate/High-k/SrGeX/Ge p-MISFETs with La-related Higher-k Gate Dielectrics**, Y. Kamata, Y. Kamimuta, and T. Tezuka, *MIRAI-Toshiba, Japan*
- 11:30 AM 6.3 - **Thin EOT and Low D_{it} Al₂O₃/GeO_x/Ge Gate Stacks Fabricated By Novel Post-Oxidation Method**, R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, *The University of Tokyo, Japan*

- 11:50 AM 6.4 - **Oxidation Sensitive LO-phonon Mode of GeO₂ in Initial Oxidation Regime of Ge**, M. Yoshida¹, C. H. Lee¹, K. Kita^{1,2}, K. Nagashio^{1,2}, T. Nishimura^{1,2}, and A. Toriumi^{1,2}, ¹*The University of Tokyo, Japan*, ²*JST-CREST, Japan*
- 12:10 PM 6.5 - **Impact of Plasma Nitridation on Electrical Properties and Thermal Stability of Ultrathin Thermal GeO₂ on Ge(100)**, K. Kutsuki, A. Kasuya, I. Hideshima, T. Hosoi, T. Shimura, and H. Watanabe, *Osaka University, Japan*
- 12:30 PM Adjourn for lunch ; Technical Committee / Invited Speaker Luncheon
- 3:00 PM – 5:30 PM Optional Rump Sessions – Topics TBD
- 7:00 PM – 10:00 PM Conference Banquet and Limerick Contest

Session 7 - Oxides

Saturday, December 4, 2010

Session Chair: J. Robertson

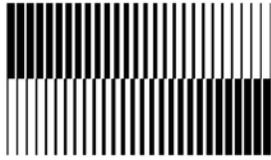
- 8:00 AM Morning Announcements
- 8:05 AM 7.1 *Invited* - **Design and Fabrication of Quantum-Enhanced Capacitors for CMOS-Applications**, J. Mannhart, *University of Augsburg, Germany*
- 8:40 AM 7.2 - **Metal-Insulator Transition at Conducting Atomic-Layer-Deposited LaAlO₃/SrTiO₃ Interface**, L. Dong¹, Y. Q. Liu², M. Xu¹, R. G. Gordon², and P. D. Ye¹, ¹*Purdue University*, ²*Harvard University*
- 9:00 AM 7.3 - **Intermixing in LaAlO₃/SrTiO₃ Interface Investigated by Medium Energy Ion Scattering**, H. D. Lee¹, T. Feng¹, E. Garfunkel¹, T. Gustafsson¹, and S. Chambers², ¹*Rutgers University*, ²*Pacific Northwest National Laboratory*
- 9:20 AM 7.4 - **Charge Transfer in Oxide Heterostructures**, A. A. Demkov and J. Lee, *UT Austin*
- 9:40 AM 7.5 - **Investigation of Leakage Mechanisms in ALD Sr-rich SrTiO₃ Films**, B. Kaczer¹, W. C. Wang², V. V. Afanas'ev², M. A. Pawlak¹, M. S. Kim¹, M. I. Popovici¹, K. Tomida¹, I. Debusschere¹, S. Van Elshocht¹, L. Altimime¹, and J. A. Kittl¹, ¹*imec, Belgium*, ²*KU Leuven, Belgium*
- 10:00 AM Break

Session 8 - High-k Oxides

Saturday, December 4, 2010

Session Chair: T. Nabatame

- 10:30 AM Opening remarks
- 10:35 AM 8.1 - **A New Model for Neutral Excited and Negative Ion States of O-atom Vacancies in Non- and Nano-crystalline High-k Dielectrics**, G. Lucovsky, L. Miotti, and K. Paz Bastos, *NC State University*
- 10:55 AM 8.2 - **Stability of Rare-Earth Scandates on Si(100)**, M. Copel, N. Bojarczuk, L. F. Edge, J. Bruley, and S. Guha, *IBM*
- 11:15 AM 8.3 - **General Stress-Defect Relationship at (100)Semiconductor/Oxide Interfaces**, M. Houssa¹, M. Scarrozza², G. Pourtois², M. Caymax², V. V. Afanas'ev¹, and A. Stesmans¹, ¹*KU Leuven, Belgium*, ²*imec, Belgium*
- 11:35 AM 8.4 - **Y-La-Si-O in Direct Contact with Silicon in Gate-First MOS Devices with 8 Å Equivalent Oxide Thickness**, C. Dubourdieu^{1,2}, M. M. Frank¹, E. Cartier¹, J. Bruley¹, S. M. Rossnagel¹, and V. Narayanan¹, ¹*IBM*, ²*Centre National de la Recherche Scientifique, France*
- 11:55 AM 8.5 - **Reevaluating Trap Densities at SiO₂/Si Interfaces on High-Index Surfaces**, T. Yasuda¹, S. Ogata², T. Mori¹, T. Horikawa¹, S. Ohno², and M. Tanaka², ¹*National Institute of Advanced Industrial Science and Technology (AIST), Japan*, ²*Yokohama National University, Japan*
- 12:15 PM 8.6 - **Medium Energy Ion Scattering Investigation of (0001)4H-SiC/Oxide Interface**, X. Zhu¹, H. D. Lee¹, T. Feng¹, A. C. Ahyi², D. Mastrogiovanni¹, A. Wan¹, E. Garfunkel¹, J. R. Williams², T. Gustafsson¹, and L. C. Feldman^{1,3}, ¹*Rutgers University*, ²*Auburn University*, ³*Vanderbilt University*
- 12:35 PM Closing Remarks



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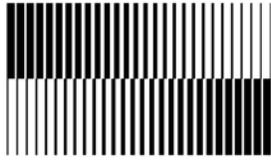
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