CONFERENCE PROGRAM

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This meeting is sponsored by the IEEE Electron Devices Society
SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, “MOS Physics and Technology,” published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author or either an oral or poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

**Winner of the 2010 SISC Ed Nicollian Award for Best Student Paper:**

Fei Xue, *University of Texas at Austin*

“InAs and In$_{0.7}$Ga$_{0.3}$As buried channel MOSFETs with ALD gate dielectrics”

with H. Zhao, Y. Chen, Y. Wang, F. Zhou, and J. Lee
Wednesday Evening Tutorial

Wednesday, November 30, 2011, 8:00 PM

First introduced at SISC 2008, the Wednesday evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

Prof. Mark Lundstrom

School of Electrical and Computer Engineering
Network for Computational Nanotechnology
Purdue University, West Lafayette, IN 47907

Understanding the Nanoscale MOSFET

MOSFET scaling continues to take transistors to smaller and smaller dimensions while advances in nanoscience provide fascinating new possibilities for electronic technologies. The MOSFET is now a true nanoelectronic device – one of enormous importance for computing, data storage, and communications. The research challenges are now about scaling below 10 nm channel lengths where traditional, textbook MOSFET theory begins to break down. Using simple models that have been backed-up by rigorous quantum mechanical simulations, this tutorial will show that the essential physics of very small MOSFETs can be simply understood. We begin with a discussion of the ballistic MOSFET and then discuss how carrier scattering affects the performance. We will explain why silicon MOSFETs operate surprisingly close to the ballistic limit – in spite of a large amount of scattering - and show that III-V HEMTs operate essentially at the ballistic limit. The reason why traditional concepts such as mobility and saturation velocity continue to have relevance will be discussed, and new concepts, like “ballistic mobility” and “injection velocity” will be introduced. Although the approach used in this tutorial appears to be much different from traditional MOSFET theory, we will show that it is easily related to the traditional approach. Finally, the limitations of the approach will be identified and the new challenges for scaling below 10 nm channel lengths will be identified. Understanding the MOSFET as a nanoelectronic device is not only useful for advancing MOSFET nanotechnology, it also provides a familiar starting point for understanding nanoelectronic devices more generally.
Conference Agenda Overview

Wednesday, November 30, 2011

Registration ........................................................................................................ 6:00 PM – 8:00 PM
Hospitality Room ............................................................................................. 8:00 PM – Midnight
Evening Tutorial ............................................................................................... 8:00 PM – 9:30 PM

Thursday, December 1, 2011

Registration ........................................................................................................ 8:00 AM – 5:00 PM
Session 1 – High-k Dielectrics ......................................................................... 8:00 AM – 9:30 AM
Poster Preview Session 1 – Dielectrics / Devices ........................................ 9:30 AM – 9:55 AM
Session 2 – Beyond Si / Oxide Electronics ..................................................... 10:25 AM – 11:40 AM
Poster Preview Session 2 – Oxide Electronics / Memory ............................... 11:40 AM – Noon
Session 3 – Devices .......................................................................................... 1:30 PM – 2:30 PM
Poster Preview Session 3 – III-V / Graphene ................................................ 2:30 PM – 2:50 PM
Session 4 – Memory .......................................................................................... 3:20 PM – 5:00 PM
Poster Preview Session 4 – Germanium / III-V ............................................ 5:00 PM – 5:20 PM
Poster Reception ............................................................................................... 7:00 PM – 10:00 PM
Hospitality Room ............................................................................................. 9:30 PM – Midnight

Friday, December 2, 2011

Registration ........................................................................................................ 8:00 AM – Noon
Session 5 - Germanium ................................................................................. 8:00 AM – 10:00 AM
Session 6 - III-V .............................................................................................. 10:30 AM – 12:30 PM
Technical Committee / Invited Speaker Luncheon ....................................... 12:30 PM – 2:00 PM
Rump Session .................................................................................................. 3:00 PM – 5:30 PM
Conference Banquet and Limerick Contest .................................................. 7:00 PM – 10:00 PM
Hospitality Room ............................................................................................. 10:00 PM – Midnight

Saturday, December 3, 2011

Session 7 – Germanium and III-V ................................................................. 8:00 AM – 10:00 AM
Session 8 – Defects and Reliability ................................................................. 10:30 AM – 11:35 AM
Session 9 – High-k Dielectrics ...................................................................... 11:35 AM – 12:55 PM
Conference Program

Session 1 - High-k Dielectrics
Thursday, December 1, 2011
Session Chair: J. Robertson

8:00 AM Welcome and opening remarks


8:50 AM 1.2 - Origin of Effective Work Function Roll-off Behavior for Replacement Gate Process Studied by Low-temperature Interfacial Layer Scavenging Technique, T. Ando, E. Cartier, J. Bruley, K. Choi, and V. Narayanan

1IBM T.J. Watson Research Center, USA; 2GLOBALFOUNDRIES, USA

9:10 AM 1.3 - Drastic degradation in dielectric properties of TiN/HfSiO/SiO2 gate stacks due to Hf uptake property of TiN electrodes, T. Hosoi, H. Arimura, Y. Odake, N. Kitano, T. Shimura, and H. Watanabe, Osaka University, Japan

Poster Preview Session 1 – Dielectrics / Devices
Thursday, December 1, 2011
Session Chair: R.M. Wallace

9:30 AM Poster Introduction

9:35 AM P.1 - Work function control and equivalent oxide thickness scaling below 9Å in a LaAlO-silicate interfacial layer / HfO2 stack compatible with gate last processing, J. Rozen, T. Ando, S.L. Brown, J. Bruley, E. Cartier, A.J. Kellock, and V. Narayanan, IBM T. J. Watson Research Center, USA; IBM Almaden Research Center, USA
P.2 - Modulation of High-K/Metal Gate Effective Work Function and its Roll-Off by Lanthanum addition, S. Baudot, C. Leroux, F. Chave, P. Caubet, G. Reimbold, G. Ghibaudo, STMicroelectronics, France; CEA-LETI, France; IMEP-LAHC, France

P.3 - First principles study of hydrogen in high κ oxides by hybrid density functional, K. Xiong, J. Robertson, and K. Cho, University of Texas at Dallas, USA; Cambridge University, UK

P.4 - Ab Initio Calculations for SiO₂ Thin Films: (i) Processing Generated Vacated O-Atom Defects and (ii) Strain Induced O-atom Vacancies With O-atoms Removed, K. Wu, G. Lucovsky, B. Papas, J.L. Whitten, North Carolina State University, USA

P.5 - Impact of Extreme Scaling on Cap Layer Induced Dipoles in High-k Metal Gate Stacks, H. Jagannathan, K. Watanabe, H. Sunamura, K. Ariyoshi, S. Allegret-Maret, V.K. Paruchuri, IBM Research @ Albany NanoTech, USA; Renesas Electronics @ Albany NanoTech, USA; Toshiba @ Albany NanoTech, USA; STMicroelectronics @ Albany NanoTech, USA

P.6 - Transitivity of band offsets between semiconductor heterojunctions and oxide insulators, V. V. Afanas’ev, H.-Y. Chou, M. Houssa, A. Stesmans, A. Lamperti, L. Lamagna, A. Molle, B. Vincent, and G. Brammertz, University of Leuven, Belgium; Laboratorio MDM, Italy; imec, Belgium

P.7 - Theoretical Approach of Effects of Wet Oxidation to Carbon Vacancy for 4H-SiC, Y. Ebihara, K. Chokawa, K. Kato, K. Kamiya, and K. Shiraishi, University of Tsukuba, Japan

P.8 - Physical Clarification of flatband voltage Shift Based on Band Alignment of High-k/Metal Gate Stack, X.L. Wang, W.W. Wang, K. Han, J. Zhang, X.L. Ma, J.J. Xiang, D.P. Chen, and T.C. Ye, Institute of Microelectronics - Chinese Academy of Sciences, China; North China University of Technology, China

P.9 - Experimental study of in situ Si oxidation for ALD high-k/metal gate stacks, E. Dentoni Litta, P.-E. Hellström, C. Henkel, M. Östling, KTH, Royal Institute of Technology, Sweden

P.10 - Low Field Mobility Model for MOSFET Stress and Surface/Channel Orientation Effects, O. Penzin, L. Smith, F. O. Heinz, Synopsys Inc – Hillsboro, USA; Synopsys Inc. - Mountain View, USA; Synopsys Schweiz GmbH, Switzerland

P.11 - Identification of vector gate current components in strained 28nm high-k pFETs, E.A. Gutiérrez-D., E. Póndigo de los A., V.H. Vega G., and F. Guarín, INAOE, Mexico; IBM Semiconductor Research and Development Center, USA

P.12 - Determination of Interface Traps in Strained-Si nMOSFETs, C. Mukherjee and C.K. Maiti, Indian Institute of Technology - Kharagpur, India

9:55 AM Break
Session 2 – Beyond Si / Oxide Electronics

Thursday, December 1, 2011

Session Chair: P. D. Ye

10:25 AM  Opening remarks

10:30 AM  2.1 Invited – Energy Efficient Computing Technologies Towards the End of Silicon Scaling, S. Guha, IBM T.J. Watson Research Center, USA

11:05 AM  2.2 Invited – Oxide-based heterostructures, D. Schlom, Cornell University, USA

Poster Preview Session 2 – Oxide Electronics / Memory

Thursday, December 1, 2011

Session Chair: C. S. Hwang

11:40 AM  P.13 - Epitaxial integration of a ferromagnet with Si (100), A. Posadas¹, M. Berg¹, H. Seo¹, A. de Lozanne¹, A.A. Demkov¹, D.J. Smith², ¹The University of Texas at Austin, USA; ²Arizona State University, USA

P.14 - Electrical Characterization of the Metal-Vanadium Dioxide Interface and Vanadium Dioxide Work Function, K. Martens¹,², I.P. Radu¹,², S. Mertens¹, X. Shi¹, M. Schaekers¹, H. Tielens¹, C.Huyghebaert¹, S. Degenêt¹,², M. Jurczak¹, V. Afanas’ev², M. Heyns¹,², J.A. Kittl¹, imec, Belgium; ²University of Leuven, Belgium

P.15 - Band Alignment of Vanadium Oxide as an Interlayer in a Hafnium Oxide-Silicon Gate Stack Structure, C. Zhu, F. Tang, X. Liu, R.J. Nemanich, Arizona State University, USA

P.16 - Alloy Bonding and Strain Induced Multivalency in TiO₂-Ti₂O₃ Magneli Phase and TiO₂-HfO₂ Alloys: Singlet Negative Ion States, Metallic Conductivity and Switching, J.-W. Kim and G. Lucovsky, North Carolina State University, USA

P.17 - Voltage-triggered resistance switching in SmNiO₃ films and SmNiO₃ – VO₂ heterostructures: Room temperature correlated oxide electronics, S.D. Ha, G.H. Aydogdu, B. Viswanath, S. Ramanathan, Harvard University, USA

P.18 - Effect of Annealing Temperature on the Forming-less Resistance Switching of NbOₓ Films, K. Lee, J. Kim, H. Na, S. Lee, H. Sohnz, Yonsei University, Korea

P.19 - Enhanced Performance for Charge-trapping Flash Memory Devices with Novel Si/Ge Super-lattice Channel, L.-J. Liu, K.-S. Chang-Liao, Y.-C. Jian, T.-K. Wang, National Tsing Hua University, Taiwan
P.20 - New Direct Measurement Technique of Programming Current for Flash Memory Cell Energy Consumption Optimization, V. Della Marca, J.L. Ogier, J. Postel-Pellerin, F. Lalande, G. Molas, 1STMicroelectronics, France; 2IM2NP, Université Aix-Marseille, France; 3CEA-LETI, France

P.21 - Effect of Top electrode material and Compliance Current on Resistive Switching properties of HfOx Film Memory Devices, D. Lee, D.-S. Byeon, J. Kim, H. Sohn, D.-H. Ko, Yonsei University, Korea

12:00 AM Adjourn for lunch

Session 3 - Devices
Thursday, December 1, 2011
Session Chair: M. Frank

1:30 PM Opening remarks

1:35 PM 3.1 Invited – Some Observations Associated with Scaling Towards Technologically Relevant Critical Geometries, I. Thayne, S. Bentley, M. Holland, I. Povey, E. O’Connor, M. Pemble, P. Hurley, J. Ahn, P. McIntyre, 1University of Glasgow, Scotland; 2Tyndall National Institute, Ireland; 3Stanford University

2:10 PM 3.2 - Thermally stable sub-nm EOT gate stack on Si-passivated In0.53Ga0.47As suitable for gate-first MOSFETs, M. El Kazzi, L. Czornomaz, C. Rossel, C. Gerl, M. Sousa, D. Caimi, H. Siegwart, J. Fompeyrine, and C. Marchiori, IBM Zurich, Switzerland

Poster Preview Session 3 – III-V / Graphene
Thursday, December 1, 2011
Session Chair: I. Thayne

2:30 PM P.22 - Surface cleaning effect on III-V oxide for InGaAs(100), (111)A, and (111)B surfaces and their Al2O3 MOS interfaces by using (NH4)2S solution, M. Yokoyama, R. Suzuki, N. Taoka, W. Jevasuwan, T. Maeda, T. Yasuda, O. Ichikawa, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, S. Takagi, The University of Tokyo, Japan; National Institute of Advanced Industrial Science and Technology (AIST), Japan; Sumitomo Chemical Co. Ltd., Japan
P.23 - Investigation of channel transport mechanisms in High-k based InGaAs MOSHEMTs, M.A. Negara1-3, D. Veksler1, J. Huang1, G. Ghibaudo3, P.K. Hurley2, G. Bersuker1, N. Goel1, P. Kirsch1, 1SEMATECH, USA; 2Tyndall National Institute, University College Cork, Ireland; 3IMEP, ENSERG, France

P.24 - Passivation of InGaAs (2x4) Surface using Trimethylaluminum, W. Melitz1, T. Kent1, A Kummel1, R. Droopad2, 1University of California at San Diego, USA; 2Texas State University, USA

P.25 - Improvement of HfO2/InGaAs Interfaces by ALD Temperature Control, R. Suzuki1, N. Taoka1, S. Lee1, S. H. Kim1, T. Hoshii1, M. Yokoyama1, T. Yasuda2, W. Jevasuwan2, T. Maeda2, O. Ichikawa3, N. Fukuhara3, M. Hata3, M. Takenaka1, S. Takagi1, 1The University of Tokyo, Japan; 2National Institute of Advanced Industrial Science and Technology (AIST), Japan; 3Sumitomo Chemical Co. Ltd., Japan

P.26 - Fermi level unpinning in metal/oxide and oxide/III-V interfaces: metal gates on MBE-grown Al2O3/Ga2O3(Gd2O3)/In0.2Ga0.8As/GaAs heterostructures, Y.C. Chang1, W.C. Hsu1, T.H. Chiang1, C.A. Lin1, Y.D. Wu1, J. Kwo1,2, M. Hong2, 1National Tsing Hua University, Taiwan; National Taiwan University, Taiwan

P.27 - Effects of Scaling and Barrier Layer Materials on High-k InGaAs MOSFETs, F. Xue, A. Jiang, H. Zhao, Y.-T. Chen, Y. Wang, F. Zhou, J. Lee, The University of Texas at Austin, USA

P.28 - Synchrotron radiation photoemission study of interface formation between MgO and the atomically clean n-InGaAs surface, L. Chauhan and G. Hughes, Dublin City University, Ireland

P.29 - Realization of Sub-100mV/dec SS for 3D Buried-channel InGaAs MOSFETs by Optimizing (NH4)2S Passivation (20%, 10%, or 5%), J.J. Gu and P.D. Ye, Purdue University, USA

P.30 - Passivation of InGaAs Surface by Ammonium Sulfide Vapor Treatment, A. Alian1,2, G. Brammertz1, C. Merckling1, A. Firrincieli1,2, W. Wang1, M. Caymax1, M. Meuris1, K. De Meyer1,2, M. Heyns1,2, imec, Belgium; 2University of Leuven, Belgium


2:50 PM Break
Session 4 - Memory
Thursday, December 1, 2011
Session Chair: Y. C. Yeo

3:20 PM  Opening remarks

3:25 PM  4.1 Invited – Cross-bar resistive memory using TiO2 thin film, G. H. Kim1, J. H. Lee1, J. H. Han1, S. J. Song1, J. Y. Seok1, J. H. Yoon1, K. J. Yoon1, M. H. Lee1, T. J. Park2, and Ch. S. Hwang1, 1Seoul National University, Korea; 2Hanyang University, Korea

4:00 PM  4.2 - Low Power RRAM with Improved HRS/LRS Uniformity through Efficient Filament Control Using CVS Forming, A. Kalantarian1,2, G. Bersuker1, D.C. Gilmer1, B. Butcher1,3, A. Padovani4, L. Vandelli4, L. Larcher4, R. Geer3, Y. Nishi2, P. Kirsch1, 1SEMATECH, USA; 2Stanford University, USA; 3University at Albany, USA; 4Università di Modena, Italy

4:20 PM  4.3 - On the electrical variability of resistive-switching memory devices based on NiO oxide, S. Tirano1,2, M. Bocquet1, Ch. Muller1, D. Deleruyelle1, L. Perniola2, V. Jousseame2, B. De Salvo2, G. Reimbold2, 1Aix-Marseille Université, France; 2CEA-LETI, France

4:40 PM  4.4 - Scalability investigation of 3D SONOS NAND Flash by experiment and simulation, G. Van den bosch, A. Arreghini, G. S. Kar, A. Maconi1, J. Van Houdt, imec, Belgium; 1DEI Politecnico di Milano, Italy

Poster Preview Session 4 – Germanium / III-V
Thursday, December 1, 2011
Session Chair: X. Garros

5:00 PM  P.34 - Effects of passivation layers and deposition temperature on electrical properties of atomic layer deposited HfO2 on Ge substrate, H.-S. Jung1,2, I.-H. Yu1, H.K. Kim1, S.Y. Lee1, N.-I. Lee2, T.J. Park3, C.S. Hwang1, 1Seoul National University, Korea; 2Samsung Electronics Co. Ltd., Korea; 3Hanyang University, Korea

P.35 - Defects, Band Offsets and Chemical Potentials in the Ge-O system, H. Li, L. Lin and J. Robertson, Cambridge University, UK

P.36 - Systematic investigation of Ge surface passivation with LaGeOx, I.Z. Mitrovic1, S. Hall1, N. Sedghi1, I. McLeod1, P. Spencer1, D. Hesp1, V.R. Dhanak1, P. Bailey2, T.C.Q. Noakes2, P.R. Chalker1, A. Dimoulas2, D. Tsoutsou3, 1University of Liverpool, UK; 2STFC Daresbury Laboratory, UK; 3NCSR Demokritos, Greece
P.37 - High-mobility Ge-on-insulator p-channel MOSFETs fabricated by lateral liquid-phase epitaxy, Y. Suzuki, S. Ogiwara, T. Hosoi, T. Shimura, H. Watanabe, Osaka University, Japan

P.38 - High resolution photoemission comparison study of interface formation between MgO and the atomically clean and selenium passivated Ge(100) surfaces, R.K. Chellappan and G. Hughes, Dublin City University, Ireland

P.39 - Study of Wet Etching Chemistry on Ge Surface in DIW, C.H. Lee¹, T. Tabata¹, T. Nishimura¹, K. Nagashio¹, K. Kita¹, and A. Toriumi¹, The University of Tokyo, Japan; ²JST-CREST, Japan

P.40 - Thin TiO₂/Al₂O₃ bilayer gate dielectrics in Ge MOS devices, M. Gunji, L. Zhang, S. Swaminathan, P.C. McIntyre, Stanford University, USA

P.41 - Ultra-shallow junction in germanium by phosphorus diffusion from polycrystalline-Ge, K. Li, H.S. Gamble, B.M. Armstrong, Queen’s University of Belfast, Ireland

P.42 - Interfacial Electronic Structure of ALD Al₂O₃ on the Clean GaAs(001)-4x6 Surface: A High-Resolution Synchrotron Radiation Photoemission Study, T.W. Pi¹, M.L. Huang²,³, Y.H. Chang³, P. Chang³, J.Y. Shen³, B.R. Chen³, K.H. Lee¹, G.K. Wertheim¹, M. Hong², and J. Kwo²,³, National Synchrotron Radiation Research Center, Taiwan; ²National Taiwan University, Taiwan; ³National Tsing Hua University, Taiwan; ⁴Woodland Consulting, USA

P.43 - Interface Studies of Atomic Layer Deposited Al₂O₃ on GaN, R.D. Long¹, B. McSkimming², M. Esposto³, S. Rajan³, J. Speck², P.C. McIntyre¹, Stanford University, USA; ²University of California Santa Barbara, USA; ³The Ohio State University, USA

P.44 - Effect of Hydrogen on Interface Properties of Al₂O₃/In₀.₅₃Ga₀₄₇As, Z. Liu¹, X. Sun¹, J. Yang¹, S. Cui¹, C.Y. Chen², K.S. Chang-Liao², T.P. Ma¹, Yale University, USA; ²National Tsing Hua University, Taiwan

P.45 - Trimethylaluminum saturation of InGaAs (100) prior to atomic layer deposition of Al₂O₃, J. Ahn and P.C. McIntyre, Stanford University, USA


5:20 PM Adjourn

7:00 PM – 10:00 PM Poster Reception
Session 5 – Germanium
Friday, December 2, 2011
Session Chair: A. Kummel

8:00 AM  Morning announcements

8:05 AM  5.1 Invited – MOS Interface Properties of Ge Gate Stacks based on Ge oxides and the Impact on MOS Device Performance, S. Takagi, R. Zhang, N. Taoka and M. Takenaka, The University of Tokyo, Japan

8:40 AM  5.2 - Epitaxial Growth of LaYO3 as Gate Dielectric for Ge CMOS by ALD, M. Xu1, Y.Q. Liu2, C. Wang1, J.Y. Zhang1, R.G. Gordon2 and P.D. Ye1,1Purdue University, USA; 2Harvard University, USA

9:00 AM  5.3 - Hydrogen reaction kinetics of the Ge Pb1 defect at the (100)Si1-xGex/SiO2 interface, A. Stesmans, N. H. Thoan, A. P. D. Nguyen, K. Keunen, and V. V. Afanas’ev, University of Leuven, Belgium

9:20 AM  5.4 - A Comparison of the Passivation and Nucleation of Ge(100) via H2O and HOOH Dosing, T. Kaufman-Osborn, J.S. Lee, K. Kiantaj, A.C. Kummel, University of California - San Diego, USA

9:40 AM  5.5 - MIGS-metal layer formation model at metal/Ge Schottky barrier diode interface, T. Nishimura and A. Toriumi, The University of Tokyo and JST-CREST, Japan

10:00 AM  Break

Session 6 - III-V
Friday, December 2, 2011
Session Chair: T. Yasuda

10:30 AM  Opening remarks

10:35 AM  6.1 Invited – Pushing the material limits in high k dielectrics on high carrier mobility semiconductors. Is in-situ process the best choice? M. L. Huang1, W. C. Lee1, T. D. Lin2, Y. H. Chang1, C. A. Lin1, Y. C. Chang2, T. W. Pi3, J. Kwo1,2, and M. Hong2,1National Tsing Hua Univ., Taiwan; 2National Taiwan Univ., Taiwan; 3National Synchrotron Radiation Research Center, Taiwan

11:10 AM  6.2 - Influence of Interface Traps inside Conduction Band on C-V Characteristics of InGaAs MOS Capacitors, N.Taoka1, M.Yokoyama1, S.H.Kim1, R. Suzuki1, R. Iida1, S. Lee1, T. Hoshii1, W. Jevasuwan2, T. Maeda2, T. Yasuda2, O. Ichikawa3, N. Fukuhara3, M. Hata3, M.Takenaka1, and S.Takagi1, The University of Tokyo, Japan; 2National Institute of Advanced Industrial Science and Technology, Japan; 3Sumitomo Chemical Co. Ltd, Japan

11:30 AM  6.3 - X-ray Photoemission beyond the Limit: Interface Characterization of 20 nm thick InAs-based MOS Stacks and InAs/high-k Nanowires, R. Timm1, O. Persson1, M. Hjort1, C. Thelander1, E. Lind1, K. A. Dick1, J. Rubio-Zuazo2, G. R.
Session 7 – Germanium and III-V

Saturday, December 3, 2011

Session Chair: A. Stesmans

8:00 AM Morning Announcements

8:05 AM 7.1 Invited – III-V 3D Transistors, P. D. Ye, J. Gu, and Y. Wu, Purdue University, USA

8:40 AM 7.2 Principles for Passivation and Bonding at III-V – oxide Interfaces, L. Lin and J. Robertson, Cambridge University, UK

9:00 AM 7.3 Impact of forming gas anneal on performance of surface channel Pd/Al2O3/In0.53Ga0.47As metal-oxide-semiconductor field-effect transistor, V. Djara, K. Cherkaoui, M. Schmidt, E. O’Connor, I. Povey, D. O’Connell, P. K. Hurley, Tyndall National Institute, University College Cork, Ireland

9:20 AM 7.4 Oxygen vacancy formation, diffusion and GeO desorption in GeO2/Ge stack, S. K. Wang1,2, K. Kita1,2, K. Nagashio1,2, T. Nishimura1,2, A. Toriumi1,2, 1The University of Tokyo, Japan; 2JST-CREST, Japan

9:40 AM 7.5 Atomic Layer Deposition of Al2O3 on GeSn and Impact of Wet Chemical Surface Pre-Treatment, S. Gupta, R. Chen, J. Harris, K.C. Saraswat, Stanford University, USA

10:00 AM Break
Session 8 – Defects and Reliability
Saturday, December 3, 2011
Session Chair: T. Nabatame

10:30 AM  Opening remarks

10:35 AM  8.1 - Impact of Body Bias on Nanoscaled MOSFETs with Individual Trapped
Gate Oxide Charges, J. Franco1, B. Kaczer, M. Toledano-Luque, P. J. Roussel,
L.-A. Ragnarsson, G. Eneman1, T. Grasser2, G. Groeseneken1, imec, Belgium; 1 also
at University of Leuven, Belgium; 2 T.U. Wien, Austria

11:55 AM  8.2 - Methodology for Defect Identification in High-k Stacks, D. Veksler, G.
Bersuker, H. Madan1, M. Minakais, K. Matthews, C. D. Young, C. Hobbs, P. D.
Kirsch, SEMATECH, USA; 1 also at Penn State University, USA

11:15 AM  8.3 - AC Transconductance Dispersion (ACGD): a novel method to profile slow
traps, X. Sun1, S. Cui1, A. Alian2, G. Brammertz2, C. Merckling2, D. Lin2, T. P.
Ma1, 1Yale University, USA; 2IMEC, Belgium

Session 9 – High-k Dielectrics
Saturday, December 3, 2011
Session Chair: M. Niwa

11:35 AM  9.1 - Low-resistivity W/TaMN/TiN full metal gate for aggressive MOSFET
Kanakasabapathy, A. Inada2, V.K. Paruchuri, V. Narayanan, IBM, USA; 2 Renesas at
Albany NanoTech, USA

11:55 AM  9.2 - Advanced characterization of lanthanum diffusion in HfSiON gate stack
by backside SIMS and MEIS combined with frontside high energy XPS, R.
Boujamaa123, F. Pierre2, E. Martinez2, M. Py2, J.P. Barnes2, O. Renault2, B.
Detlefs4, J. Zegenhagen4, M. Gros-Jean1, F. Bertin2, C. Dubourdieu3,
1STMicroelectronics, France; 2CEA-LETI, France; 3 LMGP, Grenoble, France;
4European Synchrotron Radiation Facility, France

12:15 PM  9.3 - Comparison of modulation behaviors of flat band voltage and work
function in TiN/HfO2/La gate stack on Si and Ge, H.K. Kim1, H.-S. Jung1, S.Y.
Lee1, I.-H. Yu1, T.J. Park2, C.S. Hwang1, 1Seoul National University, Korea;
2Hanyang University, Korea

12:35 PM  9.4 - Ozone Functionalization of Graphene for Atomic Layer Deposition (ALD)
of Dielectrics: in-situ Studies, S. Jandhyala, B. Lee, G. Mordi, K. Cho, J. Kim,
University of Texas at Dallas, USA

12:55 PM  Closing Remarks