42nd IEEE Semiconductor Interface Specialists Conference

SISC 2011

December 1-3, 2011 (Tutorial: November 30)
Key Bridge Marriott Hotel, Arlington, VA
www.ieeesisc.org

CONFERENCE PROGRAM

General Chair: John Robertson

Program Chair: Michel Houssa

Arrangements Chair: Chadwin Young

Ex-Officio: Martin Frank

The abstracts reproduced here are for the use of SISC attendees only. Authors are free to publish any of their work presented in this abstract book. To encourage future participants to submit new and unpublished work, conference policy is that these abstracts *may not be referenced*. The presentations themselves, which may be significantly different from the associated abstracts, may be cited "as discussed at the 2011 IEEE SISC, Arlington, VA."

42nd IEEE Semiconductor Interface Specialists Conference

SISC 2011

December 1-3, 2011 (Tutorial: November 30)
Key Bridge Marriott Hotel, Arlington, VA
www.ieeesisc.org

Executive Committee

General Chair	Program Chair	Arrangements Chair	Ex-Officio
J. Robertson	**M. Houssa**	**C. Young**	**M. M. Frank**
U. of Cambridge	U. of Leuven	Sematech	IBM
Cambridge, UK	***Leuven, BELGIUM***	***Albany, NY***	***Yorktown Heights, NY***

Registration: W. Walker, Widerkehr & Associates, Gaithersburg, MD

Technical Program Committee

E. Cartier, IBM
Yorktown Heights, NY

R. Choi, Inha University
Nam-gu Incheon, KOREA

S. Datta, Penn State University
University Park, PA

A. Demkov, University of Texas at Austin
Austin, TX

X. Garros, CEA-LETI
Grenoble, FRANCE

A. Kummel, UCSD
San Diego, CA

P. Mahji, SEMATECH
Albany, NY

T. Nabatame, NIMS
Tsukuba, JAPAN

T. Nigam, GLOBALFOUNDRIES
Milpitas, CA

M. Niwa, University of Tsukuba
Tsukuba, JAPAN

J. Schubert, FZ-Juelich
Jülich, GERMANY

E. Shero, ASM America
Phoenix, AZ

A. Stesmans, University of Leuven
Leuven, BELGIUM

J. Van Houdt, imec
Leuven, BELGIUM

R. Wallace, University of Texas at Dallas
Dallas, TX

T. Yasuda, AIST
Tsukuba, JAPAN

Y. C. Yeo, National University of Singapore
SINGAPORE

This meeting is sponsored by the IEEE Electron Devices Society

SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology," published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author or either an oral or poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

Winner of the 2010 SISC Ed Nicollian Award for Best Student Paper:

Fei Xue, *University of Texas at Austin*

"InAs and $In_{0.7}Ga_{0.3}As$ buried channel MOSFETs with ALD gate dielectrics"

with H. Zhao, Y. Chen, Y. Wang, F. Zhou, and J. Lee

SISC 2011

42nd IEEE
Semiconductor Interface
Specialists Conference

December 1-3, 2011 (Tutorial: November 30)
Key Bridge Marriott Hotel, Arlington, VA
www.ieeesisc.org

Wednesday Evening Tutorial

Wednesday, November 30, 2011, 8:00 PM

First introduced at SISC 2008, the Wednesday evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

Prof. Mark Lundstrom

School of Electrical and Computer Engineering
Network for Computational Nanotechnology
Purdue University, West Lafayette, IN 47907

Understanding the Nanoscale MOSFET

MOSFET scaling continues to take transistors to smaller and smaller dimensions while advances in nanoscience provide fascinating new possibilities for electronic technologies. The MOSFET is now a true nanoelectronic device – one of enormous importance for computing, data storage, and communications. The research challenges are now about scaling below 10 nm channel lengths where traditional, textbook MOSFET theory begins to break down. Using simple models that have been backed-up by rigorous quantum mechanical simulations, this tutorial will show that the essential physics of very small MOSFETs can be simply understood. We begin with a discussion of the ballistic MOSFET and then discuss how carrier scattering affects the performance. We will explain why silicon MOSFETs operate surprisingly close to the ballistic limit – in spite of a large amount of scattering - and show that III-V HEMTs operate essentially at the ballistic limit. The reason why traditional concepts such as mobility and saturation velocity continue to have relevance will be discussed, and new concepts, like "ballistic mobility" and "injection velocity" will be introduced. Although the approach used in this tutorial appears to be much different from traditional MOSFET theory, we will show that it is easily related to the traditional approach. Finally, the limitations of the approach will be identified and the new challenges for scaling below 10 nm channel lengths will be identified. Understanding the MOSFET as a nanoelectronic device is not only useful for advancing MOSFET nanotechnology, it also provides a familiar starting point for understanding nanoelectronic devices more generally.

Conference Agenda Overview

Wednesday, November 30, 2011

Registration ..... 6:00 PM – 8:00 PM
Hospitality Room ..... 8:00 PM – Midnight
Evening Tutorial ..... 8:00 PM – 9:30 PM

Thursday, December 1, 2011

Registration ..... 8:00 AM – 5:00 PM
Session 1 – High-k Dielectrics ..... 8:00 AM – 9:30 AM
Poster Preview Session 1 – Dielectrics / Devices ..... 9:30 AM – 9:55 AM
Session 2 – Beyond Si / Oxide Electronics ..... 10:25 AM – 11:40 AM
Poster Preview Session 2 – Oxide Electronics / Memory ..... 11:40 AM – Noon
Session 3 – Devices ..... 1:30 PM – 2:30 PM
Poster Preview Session 3 – III-V / Graphene ..... 2:30 PM – 2:50 PM
Session 4 – Memory ..... 3:20 PM – 5:00 PM
Poster Preview Session 4 – Germanium / III-V ..... 5:00 PM – 5:20 PM
Poster Reception ..... 7:00 PM – 10:00 PM
Hospitality Room ..... 9:30 PM – Midnight

Friday, December 2, 2011

Registration ..... 8:00 AM – Noon
Session 5 - Germanium ..... 8:00 AM – 10:00 AM
Session 6 - III-V ..... 10:30 AM – 12:30 PM
Technical Committee / Invited Speaker Luncheon ..... 12:30 PM – 2:00 PM
Rump Session ..... 3:00 PM – 5:30 PM
Conference Banquet and Limerick Contest ..... 7:00 PM – 10:00 PM
Hospitality Room ..... 10:00 PM – Midnight

Saturday, December 3, 2011

Session 7 – Germanium and III-V ..... 8:00 AM – 10:00 AM
Session 8 – Defects and Reliability ..... 10:30 AM – 11:35 AM
Session 9 – High-k Dielectrics ..... 11:35 AM – 12:55 PM

Conference Program

Session 1 - High-k Dielectrics

Thursday, December 1, 2011

Session Chair: J. Robertson

8:00 AM Welcome and opening remarks

8:15 AM 1.1 *Invited* – **Ultrathin EOT scaling of high-k/metal gate stacks,** L.-Å. Ragnarsson, M. Cho, T. Chiarella, J. Mitard, T. Schram, E. Röhr, L. Witters, M. Togo, N. Horiguchi, and A. Thean, *imec, Belgium*

8:50 AM 1.2 - **Origin of Effective Work Function Roll-off Behavior for Replacement Gate Process Studied by Low-temperature Interfacial Layer Scavenging Technique,** T. Ando[1], E. Cartier[1], J. Bruley[1], K. Choi[2], and V. Narayanan[1] [1]*IBM T.J. Watson Research Center, USA;* [2]*GLOBALFOUNDRIES, USA*

9:10 AM 1.3 - **Drastic degradation in dielectric properties of TiN/HfSiO/SiO_2 gate stacks due to Hf uptake property of TiN electrodes,** T. Hosoi, H. Arimura, Y. Odake, N. Kitano, T. Shimura, and H. Watanabe, *Osaka University, Japan*

Poster Preview Session 1 – Dielectrics / Devices

Thursday, December 1, 2011

Session Chair: R.M. Wallace

9:30 AM Poster Introduction

9:35 AM P.1 - **Work function control and equivalent oxide thickness scaling below 9Å in a LaAlO-silicate interfacial layer / HfO_2 stack compatible with gate last processing**, J. Rozen, T. Ando, S.L. Brown, J. Bruley, E. Cartier, A.J. Kellock[*], and V.Narayanan, *IBM T. J. Watson Research Center, USA;* [*]*IBM Almaden Research Center, USA*

P.2 - **Modulation of High-K/Metal Gate Effective Work Function and its Roll-Off by Lanthanum addition**, S. Baudot[1,2,3], C. Leroux[2], F. Chave[1], P. Caubet[1], G. Reimbold[2], G. Ghibaudo[3], *[1]STMicroelectronics, France; [2]CEA-LETI, France;[3] IMEP-LAHC, France*

P.3 - **First principles study of hydrogen in high κ oxides by hybrid density functional**, K. Xiong[1], J. Robertson[2], and K. Cho[1], *[1]University of Texas at Dallas, USA; [2]Cambridge University, UK*

P.4 - **Ab Initio Calculations for SiO_2 Thin Films: (i) Processing Generated Vacated O-Atom Defects and (ii) Strain Inducted O-atom Vacancies With O-atoms Removed**, K. Wu, G. Lucovsky, B. Papas, J.L. Whitten, *North Carolina State University, USA*

P.5 - **Impact of Extreme Scaling on Cap Layer Induced Dipoles in High-k Metal Gate Stacks**, H. Jagannathan[1], K. Watanabe[2], H. Sunamura[2], K. Ariyoshi[3], S. Allegret-Maret[4], V.K. Paruchuri[1],*[1]IBM Research @ Albany NanoTech, USA; [2]Renesas Electronics @ Albany NanoTech, USA; [3]Toshiba @ Albany NanoTech, USA; [4]STMicroelectronics @ Albany NanoTech, USA*

P.6 - **Transitivity of band offsets between semiconductor heterojunctions and oxide insulators**, V. V. Afanas'ev[1], H.-Y. Chou[1], M. Houssa[1], A. Stesmans[1], A. Lamperti[2], L. Lamagna[2], A. Molle[2], B. Vincent[3], and G. Brammertz[3], *[1]University of Leuven, Belgium; [2]Laboratorio MDM, Italy; [3]imec, Belgium*

P.7 - **Theoretical Approach of Effects of Wet Oxidation to Carbon Vacancy for 4H-SiC**, Y. Ebihara, K. Chokawa, K. Kato, K. Kamiya, and K. Shiraishi, *University of Tsukuba, Japan*

P.8 - **Physical Clarification of flatband voltage Shift Based on Band Alignment of High-k/Metal Gate Stack**, X.L. Wang, W.W. Wang, K. Han, J. Zhang[*], X.L. Ma, J.J. Xiang, D.P. Chen, and T.C. Ye, *Institute of Microelectronics - Chinese Academy of Sciences, China; [*]North China University of Technology, China*

P.9 - **Experimental study of in situ Si oxidation for ALD high-k/metal gate stacks**, E. Dentoni Litta, P.-E. Hellström, C. Henkel, M. Östling, *KTH, Royal Institute of Technology, Sweden*

P.10 - **Low Field Mobility Model for MOSFET Stress and Surface/Channel Orientation Effects**, O. Penzin[1], L. Smith[2], F. O. Heinz[3], *[1]Synopsys Inc – Hillsboro, USA; [2]Synopsys Inc. - Mountain View, USA; [3]Synopsys Schweiz GmbH, Switzerland*

P.11 - **Identification of vector gate current components in strained 28nm high-k pFETs**, E.A. Gutiérrez-D.[1], E. Póndigo de los A.[1], V.H. Vega G.[1], and F. Guarin[2], *[1]INAOE, Mexico; [2] IBM Semiconductor Research and Development Center, USA*

P.12 - **Determination of Interface Traps in Strained-Si nMOSFETs**, C. Mukherjee and C.K. Maiti, *Indian Institute of Technology - Kharagpur, India*

9:55 AM Break

Session 2 – Beyond Si / Oxide Electronics

Thursday, December 1, 2011

Session Chair: P. D. Ye

10:25 AM Opening remarks

10:30 AM 2.1 *Invited* – **Energy Efficient Computing Technologies Towards the End of Silicon Scaling,** S. Guha, *IBM T.J. Watson Research Center, USA*

11:05 AM 2.2 *Invited* – **Oxide-based heterostructures,** D. Schlom, *Cornell University, USA*

Poster Preview Session 2 – Oxide Electronics / Memory

Thursday, December 1, 2011

Session Chair: C. S. Hwang

11:40 AM P.13 - **Epitaxial integration of a ferromagnet with Si (100)**, A. Posadas[1], M. Berg[1], H. Seo[1], A. de Lozanne[1], A.A. Demkov[1], D.J. Smith[2], *[1]The University of Texas at Austin, USA; [2]Arizona State University, USA*

P.14 - **Electrical Characterization of the Metal-Vanadium Dioxide Interface and Vanadium Dioxide Work Function**, K. Martens[1,2], I.P. Radu[1,2], S. Mertens[1], X. Shi[1], M. Schaekers[1], H. Tielens[1], C.Huyghebaert[1], S. Degendt[1,2], M. Jurczak[1], V. Afanas'ev[2], M. Heyns[1,2], J.A. Kittl[1], *[1]imec, Belgium; [2]University of Leuven, Belgium*

P.15 - **Band Alignment of Vanadium Oxide as an Interlayer in a Hafnium Oxide-Silicon Gate Stack Structure**, C. Zhu, F. Tang, X. Liu, R.J. Nemanich, *Arizona State University, USA*

P.16 - **Alloy Bonding and Strain Induced Multivalency in TiO_2-Ti_2O_3 Magneli Phase and TiO_2-HfO_2 Alloys: Singlet Negative Ion States, Metallic Conductivity and Switching**, J.-W. Kim and G. Lucovsky, *North Carolina State University, USA*

P.17 - **Voltage-triggered resistance switching in $SmNiO_3$ films and $SmNiO_3$ – VO_2 heterostructures: Room temperature correlated oxide electronics**, S.D. Ha, G.H. Aydogdu, B. Viswanath, S. Ramanathan, *Harvard University, USA*

P.18 - **Effect of Annealing Temperature on the Forming-less Resistance Switching of NbO_x Films**, K. Lee, J. Kim, H. Na, S. Lee, H. Sohnz, *Yonsei University, Korea*

P.19 - **Enhanced Performance for Charge-trapping Flash Memory Devices with Novel Si/Ge Super-lattice Channel**, L.-J. Liu, K.-S. Chang-Liao, Y.-C. Jian, T.-K. Wang, *National Tsing Hua University, Taiwan*

P.20 - **New Direct Measurement Technique of Programming Current for Flash Memory Cell Energy Consumption Optimization**, V. Della Marca[1,2,3], J.L. Ogier[1], J. Postel-Pellerin[2], F. Lalande[2], G. Molas[3], *[1]STMicroelectronics, France; [2]IM2NP, Université Aix-Marseille, France; [3]CEA-LETI, France*

P.21 - **Effect of Top electrode material and Compliance Current on Resistive Switching properties of HfO_x Film Memory Devices**, D. Lee, D.-S. Byeon, J. Kim, H. Sohn, D.-H. Ko, *Yonsei University, Korea*

12:00 AM Adjourn for lunch

Session 3 - Devices

Thursday, December 1, 2011

Session Chair: M. Frank

1:30 PM Opening remarks

1:35 PM 3.1 *Invited* – **Some Observations Associated with Scaling Towards Technologically Relevant Critical Geometries,** I. Thayne[1], S. Bentley[1], M. Holland[1], I. Povey[2], E. O'Connor[2], M. Pemble[2], P. Hurley[2], J. Ahn[3], P. McIntyre[3], *[1]University of Glasgow, Scotland; [2]Tyndall National Institute, Ireland; [3]Stanford University*

2:10 PM 3.2 - **Thermally stable sub-nm EOT gate stack on Si-passivated In0.53Ga0.47As suitable for gate-first MOSFETs**, M. El Kazzi, L. Czornomaz, C. Rossel, C. Gerl, M. Sousa, D. Caimi, H. Siegwart, J. Fompeyrine, and C.Marchiori, *IBM Zurich, Switzerland*

Poster Preview Session 3 – III-V / Graphene

Thursday, December 1, 2011

Session Chair: I. Thayne

2:30 PM P.22 - **Surface cleaning effect on III-V oxide for InGaAs(100), (111)A, and (111)B surfaces and their Al_2O_3 MOS interfaces by using $(NH_4)_2S$ solution**, M. Yokoyama[1] , R. Suzuki[1] , N. Taoka[1] , W. Jevasuwan[2] , T. Maeda[2] , T. Yasuda[2] , O. Ichikawa[3] , H. Yamada[3] , N. Fukuhara[3] , M. Hata[3] , M. Sugiyama[1] , Y. Nakano[1] , M. Takenaka[1], S. Takagi[1], *[1]The University of Tokyo, Japan; [2]National Institute of Advanced Industrial Science and Technology (AIST), Japan; [3]Sumitomo Chemical Co. Ltd., Japan*

P.23 - **Investigation of channel transport mechanisms in High-k based InGaAs MOSHEMTs**, M.A. Negara[1-3], D. Veksler[1], J. Huang[1], G. Ghibaudo[3], P.K. Hurley[2], G. Bersuker[1], N. Goel[1], P. Kirsch[1], *[1]SEMATECH, USA; [2]Tyndall National Institute, University College Cork, Ireland; [3]IMEP, ENSERG, France*

P.24 - **Passivation of InGaAs (2x4) Surface using Trimethylaluminum**, W. Melitz[1] , T. Kent[1], A Kummel[1], R. Droopad[2], *[1]University of California at San Diego, USA; [2]Texas State University, USA*

P.25 - **Improvement of HfO_2/InGaAs Interfaces by ALD Temperature Control**, R. Suzuki[1], N. Taoka[1], S. Lee[1], S. H. Kim[1], T.Hoshii[1], M. Yokoyama[1], T. Yasuda[2], W. Jevasuwan[2], T. Maeda[2], O. Ichikawa[3], N. Fukuhara[3], M. Hata[3], M. Takenaka[1], S. Takagi[1], *[1]The University of Tokyo, Japan; [2]National Institute of Advanced Industrial Science and Technology (AIST), Japan; [3]Sumitomo Chemical Co. Ltd., Japan*

P.26 - **Fermi level unpinning in metal/oxide and oxide/III-V interfaces: metal gates on MBE-grown Al_2O_3/$Ga_2O_3(Gd_2O_3)$/$In_{0.2}Ga_{0.8}As$/GaAs heterostructures**, Y.C. Chang[1], W.C. Hsu[1], T.H. Chiang[1], C.A. Lin[1], Y.D. Wu[1], J. Kwo[1,2], M. Hong[2], *[1]National Tsing Hua University, Taiwan; National Taiwan University, Taiwan*

P.27 - **Effects of Scaling and Barrier Layer Materials on High-k InGaAs MOSFETs**, F. Xue, A. Jiang, H. Zhao, Y.-T. Chen, Y. Wang, F. Zhou, J. Lee, *The University of Texas at Austin, USA*

P.28 - **Synchrotron radiation photoemission study of interface formation between MgO and the atomically clean n-InGaAs surface**, L. Chauhan and G. Hughes, *Dublin City University, Ireland*

P.29 - **Realization of Sub-100mV/dec SS for 3D Buried-channel InGaAs MOSFETs by Optimizing (NH_4)2S Passivation (20%, 10%, or 5%)**, J.J. Gu and P.D. Ye, *Purdue University, USA*

P.30 - **Passivation of InGaAs Surface by Ammonium Sulfide Vapor Treatment**, A. Alian[1,2], G. Brammertz[1], C. Merckling[1], A. Firrincieli[1,2], W. Wang[1], M. Caymax[1], M. Meuris[1], K. De Meyer[1,2], M. Heyns[1,2], *[1]imec, Belgium; [2]University of Leuven, Belgium*

P.31 - **Thermal stability of the InP/high-k dielectric interface**, R.V. Galatage, H. Dong, D.M. Zhernokletov, B. Brennan, C.L. Hinkle, R.M. Wallace, E.M. Vogel, *The University of Texas at Dallas, USA*

P.32 – **Study on the Origin of Hysteretic Characteristics of Graphene Field Effect Transistor**, Y.G. Lee, C.G. Kang, Y.H. Kim, C.H. Cho, U.J. Jung, S.K. Lee, B.H. Lee, *Gwangju Institute of Science and Technology, Korea*

P.33 - **Enhancement of electron conduction and reduction of hysteresis for graphene FET by low temperature ALD Al_2O_3 Passivation**, C.G. Kang, Y.G. Lee, S.K. Lee, E. Park, C.H. Cho, S.K. Lim, H.J. Hwang, B.H. Lee, *Gwangju Institute of Science and Technology, Korea*

2:50 PM Break

Session 4 - Memory

Thursday, December 1, 2011

Session Chair: Y. C. Yeo

3:20 PM Opening remarks

3:25 PM 4.1 *Invited* – **Cross-bar resistive memory using TiO_2 thin film,** G. H. Kim[1], J. H. Lee[1], J. H. Han[1], S. J. Song[1], J. Y. Seok[1], J. H. Yoon[1], K. J. Yoon[1], M. H. Lee[1], T. J. Park[2], and Ch. S. Hwang[1]**,** *[1]Seoul National University, Korea; [2]Hanyang University, Korea*

4:00 PM 4.2 - **Low Power RRAM with Improved HRS/LRS Uniformity through Efficient Filament Control Using CVS Forming,** A. Kalantarian[1,2], G. Bersuker[1], D.C. Gilmer[1], B. Butcher[1,3], A. Padovani[4], L. Vandelli[4], L. Larcher[4], R. Geer[3], Y. Nishi[2], P. Kirsch[1], *[1]SEMATECH, USA; [2]Stanford University, USA; [3]University at Albany, USA; Università di Modena, Italy*

4:20 PM 4.3 - **On the electrical variability of resistive-switching memory devices based on NiO oxide,** S.Tirano[1,2], M.Bocquet[1], Ch.Muller[1], D.Deleruyelle[1], L.Perniola[2], V. Jousseaume[2], B. De Salvo[2], G.Reimbold[2], *[1]Aix-Marseille Université, France; [2]CEA-LETI, France*

4:40 PM 4.4 - **Scalability investigation of 3D SONOS NAND Flash by experiment and simulation,** G. Van den bosch, A. Arreghini, G. S. Kar, A. Maconi[1], J. Van Houdt, *imec, Belgium; [1]DEI Politecnico di Milano, Italy*

Poster Preview Session 4 – Germanium / III-V

Thursday, December 1, 2011

Session Chair: X. Garros

5:00 PM P.34 - **Effects of passivation layers and deposition temperature on electrical properties of atomic layer deposited HfO_2 on Ge substrate**, H.-S. Jung[1,2], I.-H. Yu[1], H.K. Kim[1], S.Y. Lee[1], N.-I. Lee[2], T.J. Park[3], C.S. Hwang[1], *[1]Seoul National University, Korea; [2]Samsung Electronics Co. Ltd., Korea; [3]Hanyang University, Korea*

P.35 - **Defects, Band Offsets and Chemical Potentials in the Ge-O system**, H. Li, L. Lin and J. Robertson, *Cambridge University, UK*

P.36 - **Systematic investigation of Ge surface passivation with $LaGeO_x$,** I.Z. Mitrovic[1], S. Hall[1], N. Sedghi[1], I. McLeod[1], P. Spencer[1], D. Hesp[1], V.R. Dhanak[1], P. Bailey[2], T.C.Q. Noakes[2], P.R. Chalker[1], A. Dimoulas[3], D. Tsoutsou[3], *[1]University of Liverpool, UK; [2]STFC Daresbury Laboratory, UK; [3]NCSR Demokritos, Greece*

P.37 - **High-mobility Ge-on-insulator p-channel MOSFETs fabricated by lateral liquid-phase epitaxy**, Y. Suzuki, S. Ogiwara, T. Hosoi, T. Shimura, H. Watanabe, *Osaka University, Japan*

P.38 - **High resolution photoemission comparison study of interface formation between MgO and the atomically clean and selenium passivated Ge(100) surfaces**, R.K. Chellappan and G. Hughes, *Dublin City University, Ireland*

P.39 - **Study of Wet Etching Chemistry on Ge Surface in DIW**, C.H. Lee[1,2], T. Tabata[1,2], T. Nishimura[1,2], K. Nagashio[1,2], K. Kita[1,2], and A. Toriumi[1,2], *[1]The University of Tokyo, Japan; [2]JST-CREST, Japan*

P.40 - **Thin TiO_2/Al_2O_3 bilayer gate dielectrics in Ge MOS devices**, M. Gunji, L. Zhang, S. Swaminathan, P.C. McIntyre, *Stanford University, USA*

P.41 - **Ultra-shallow junction in germanium by phosphorus diffusion from polycrystalline-Ge**, K. Li, H.S. Gamble, B.M. Armstrong, *Queen's University of Belfast, Ireland*

P.42 - **Interfacial Electronic Structure of ALD Al_2O_3 on the Clean GaAs(001)-4x6 Surface: A High-Resolution Synchrotron Radiation Photoemission Study**, T.W. Pi[1], M.L. Huang[2,3], Y.H. Chang[3], P. Chang[3], J.Y. Shen[3], B.R. Chen[3], K.H. Lee[1], G.K. Wertheim[4], M. Hong[2], and J. Kwo[2,3], *[1]National Synchrotron Radiation Research Center, Taiwan; [2]National Taiwan University,Taiwan; [3]National Tsing Hua University, Taiwan; [4]Woodland Consulting, USA*

P.43 - **Interface Studies of Atomic Layer Deposited Al_2O_3 on GaN**, R.D. Long[1], B. McSkimming[2], M. Esposto[3], S. Rajan[3], J. Speck[2], P.C. McIntyre[1], *[1]Stanford University, USA; [2]University of California Santa Barbara, USA; [3]The Ohio State University, USA*

P.44 - **Effect of Hydrogen on Interface Properties of $Al_2O_3/In_{0.53}Ga_{0.47}As$**, Z. Liu[1], X. Sun[1], J. Yang[1], S. Cui[1], C.Y. Chen[2], K.S. Chang-Liao[2], T.P. Ma[1], *[1]Yale University, USA; [2]National Tsing Hua University, Taiwan*

P.45 - **Trimethylaluminum saturation of InGaAs (100) prior to atomic layer deposition of Al_2O_3** , J. Ahn and P.C. McIntyre, *Stanford University, USA*

P.46 - **Role of Wide Bandgap III-V Materials on Emitter Surface Passivation of Single-Junction GaAs Solar Cells**, D. Shahrjerdi, C. Ebert[*], T. Gokmen, B. Hekmatshoar, C.-W. Cheng, S.W. Bedell, D.K. Sadana, *IBM T.J. Watson Research Center, USA; [*]Veeco Corporation, USA*

5:20 PM Adjourn

7:00 PM – 10:00 PM Poster Reception

Session 5 – Germanium

Friday, December 2, 2011

Session Chair: A. Kummel

8:00 AM Morning announcements

8:05 AM 5.1 *Invited* – **MOS Interface Properties of Ge Gate Stacks based on Ge oxides and the Impact on MOS Device Performance,** S. Takagi, R. Zhang, N. Taoka and M. Takenaka, *The University of Tokyo, Japan*

8:40 AM 5.2 - **Epitaxial Growth of $LaYO_3$ as Gate Dielectric for Ge CMOS by ALD**, M. Xu[1], Y.Q. Liu[2], C. Wang[1], J.Y. Zhang[1], R.G. Gordon[2] and P.D. Ye[1], *[1]Purdue University, USA; [2]Harvard University, USA*

9:00 AM 5.3 - **Hydrogen reaction kinetics of the Ge Pb_1 defect at the (100)$Si_{1-x}Ge_x/SiO_2$ interface,** A. Stesmans, N. H. Thoan, A. P. D. Nguyen, K. Keunen, and V. V. Afanas'ev, *University of Leuven, Belgium*

9:20 AM 5.4 - **A Comparison of the Passivation and Nucleation of Ge(100) via H_2O and HOOH Dosing,** T. Kaufman-Osborn, J.S. Lee, K. Kiantaj, A.C. Kummel, *University of California - San Diego, USA*

9:40 AM 5.5 - **MIGS-metal layer formation model at metal/Ge Schottky barrier diode interface,** T. Nishimura and A. Toriumi, *The University of Tokyo and JST-CREST, Japan*

10:00 AM Break

Session 6 - III-V

Friday, December 2, 2011

Session Chair: T. Yasuda

10:30 AM Opening remarks

10:35 AM 6.1 *Invited* – **Pushing the material limits in high k dielectrics on high carrier mobility semiconductors. Is in-situ process the best choice?** M. L. Huang[1], W. C. Lee[1], T. D. Lin[2], Y. H. Chang[1], C. A. Lin[1], Y. C. Chang[2], T. W. Pi[3], J. Kwo[1,2], and M. Hong[2], *[1]National Tsing Hua Univ., Taiwan; [2]National Taiwan Univ., Taiwan; [3]National Synchrotron Radiation Research Center, Taiwan*

11:10 AM 6.2 - **Influence of Interface Traps inside Conduction Band on C-V Characteristics of InGaAs MOS Capacitors,** N.Taoka[1] , M.Yokoyama[1] , S.H.Kim[1] , R. Suzuki[1] , R. Iida[1] , S. Lee[1] , T. Hoshii[1] , W. Jevasuwan[2] , T. Maeda[2] , T. Yasuda[2] , O. Ichikawa[3] , N. Fukuhara[3] , M. Hata[3] , M.Takenaka[1] , and S.Takag[1], *[1]The University of Tokyo, Japan; [2]National Institute of Advanced Industrial Science and Technology, Japan; [3]Sumitomo Chemical Co. Ltd, Japan*

11:30 AM 6.3 - **X-ray Photoemission beyond the Limit: Interface Characterization of 20 nm thick InAs-based MOS Stacks and InAs/high-k Nanowires,** R. Timm[1], O. Persson[1], M. Hjort[1], C. Thelander[1], E. Lind[1], K. A. Dick[1], J. Rubio-Zuazo[2], G. R.

Castro[2], L. Samuelson[1], L.-E. Wernersson[1], and A. Mikkelsen[1], *[1]Lund University, Sweden; [2]SpLine Spanish CRG Beamline at the ESRF, France*

11:50 AM 6.4 - **Characterization of Interface Traps in Metal–High-k–InAs/GaSb TFETs,** S.D. Chae, G. Zhou, I. Kwihangana, R. Li, Y. Lu, Q. Liu, T. Vasen, Q. Zhang, W.-S. Hwang, P. Fay, T. Kosel, M. Wistey, H. Xing, A. Seabaugh, *University of Notre Dame, USA*

12:10 PM 6.5 - **Improved Electron Mobility and On/Off Ratio of InGaAs MISFETs by New Surface Treatments Utilizing Selenite Adsorption,** Y. Urabe[1], N. Miyata[1], W. Jevasuwan[1], T.Maeda[1], and T.Yasuda[1], O. Ichikawa[2], N. Fukuhara[2], M. Hata[2], M. Yokoyama[3], N. Taoka[3], M. Takenaka[3], S. Takagi[3], *[1]National Institute of Advanced Industrial Science and Technology, Japan; [2]Sumitomo Chemical, Japan; [3]The University of Tokyo, Japan*

12:30 PM Adjourn for lunch ; Technical Committee / Invited Speaker Luncheon

3:00 PM – 5:30 PM Optional Rump Sessions – Topics TBD

7:00 PM – 10:00 PM Conference Banquet and Limerick Contest

Session 7 – Germanium and III-V

Saturday, December 3, 2011

Session Chair: A. Stesmans

8:00 AM Morning Announcements

8:05 AM 7.1 *Invited* – **III-V 3D Transistors,** P. D. Ye, J. Gu, and Y. Wu, *Purdue University, USA*

8:40 AM 7.2 - **Principles for Passivation and Bonding at III-V – oxide Interfaces,** L. Lin and J. Robertson, *Cambridge University, UK*

9:00 AM 7.3 - **Impact of forming gas anneal on performance of surface channel $Pd/Al_2O_3/In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistor,** V. Djara, K. Cherkaoui, M. Schmidt, E. O'Connor, I. Povey, D. O'Connell, P. K. Hurley, *Tyndall National Institute, University College Cork, Ireland*

9:20 AM 7.4 – **Oxygen vacancy formation, diffusion and GeO desorption in GeO_2/Ge stack**, S. K. Wang[1,2], K. Kita[1,2], K. Nagashio[1,2], T. Nishimura[1,2], A. Toriumi[1,2], *[1]The University of Tokyo, Japan; [2]JST-CREST, Japan*

9:40 AM 7.5 - **Atomic Layer Deposition of Al_2O_3 on GeSn and Impact of Wet Chemical Surface Pre-Treatment,** S. Gupta, R. Chen, J. Harris, K.C. Saraswat, *Stanford University, USA*

10:00 AM Break

Session 8 – Defects and Reliability

Saturday, December 3, 2011

Session Chair: T. Nabatame

10:30 AM Opening remarks

10:35 AM 8.1 - **Impact of Body Bias on Nanoscaled MOSFETs with Individual Trapped Gate Oxide Charges,** J. Franco[1], B. Kaczer, M. Toledano-Luque, P. J. Roussel, L.-Å. Ragnarsson, G. Eneman[1], T. Grasser[2], G. Groeseneken[1], *imec, Belgium; [1]also at University of Leuven, Belgium; [2]T.U.Wien, Austria*

11:55 AM 8.2 - **Methodology for Defect Identification in High-k Stacks,** D. Veksler, G. Bersuker, H. Madan[1] , M. Minakais, K. Matthews, C. D. Young, C. Hobbs, P. D. Kirsch, *SEMATECH, USA; [1]also at Penn State University, USA*

11:15 AM 8.3 - **AC Transconductance Dispersion (ACGD): a novel method to profile slow traps,** X. Sun[1], S. Cui[1], A. Alian[2], G. Brammertz[2], C. Merckling[2], D. Lin[2], T. P. Ma[1], *[1]Yale University, USA; [2]IMEC, Belgium*

Session 9 – High-k Dielectrics

Saturday, December 3, 2011

Session Chair: M. Niwa

11:35 AM 9.1 - **Low-resistivity W/TaMN/TiN full metal gate for aggressive MOSFET scaling,** M.M. Frank, L. F. Edge, S.L. Brown, J. Bruley, M. J.P. Hopstaken, S. Kanakasabapathy, A. Inada[2], V.K. Paruchuri, V. Narayanan, *IBM, USA; [2]Renesas at Albany NanoTech, USA*

11:55 AM 9.2 - **Advanced characterization of lanthanum diffusion in HfSiON gate stack by backside SIMS and MEIS combined with frontside high energy XPS,** R. Boujamaa[1,2,3], F. Pierre[2], E. Martinez[2], M. Py[2], J.P. Barnes[2], O. Renault[2], B. Detlefs[4], J. Zegenhagen[4], M. Gros-Jean[1], F. Bertin[2], C . Dubourdieu[3], *[1]STMicroelectronics, France; [2]CEA-LETI, France; [3]LMGP, Grenoble, France; [4]European Synchrotron Radiation Facility, France*

12:15 PM 9.3 - **Comparison of modulation behaviors of flat band voltage and work function in TiN/HfO_2/La gate stack on Si and Ge,** H.K. Kim[1], H.-S. Jung[1], S.Y. Lee[1], I.-H. Yu[1], T.J. Park[2], C.S. Hwang[1], *[1]Seoul National University, Korea; [2]Hanyang University, Korea*

12:35 PM 9.4 - **Ozone Functionalization of Graphene for Atomic Layer Deposition (ALD) of Dielectrics: in-situ Studies**, S. Jandhyala, B. Lee, G. Mordi, K. Cho, J. Kim, *University of Texas at Dallas, USA*

12:55 PM Closing Remarks