44th IEEE Semiconductor Interface Specialists Conference

SISC 2013

December 5-7, 2013 (Tutorial: December 4)
Key Bridge Marriott Hotel, Arlington, VA
www.ieeesisc.org

CONFERENCE PROGRAM

General Chair: Chadwin Young

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SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology," published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author for either an oral or a poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

Winner of the 2012 SISC Ed Nicollian Award for Best Student Paper:

Jiangjiang Gu, *Purdue University*

"Performance and Variability Breakthrough for $LaAlO_3$/InGaAs Gate-all-around Nanowire MOSFETs with Ultra-thin Al_2O_3 Passivation"

with P. D. Ye

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Wednesday Evening Tutorial

Wednesday, December 4, 2013, 8:00 PM

First introduced at SISC 2008, the Wednesday evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

Prof. Michelle Simmons

The University of New South Wales, Australia

The development of a quantum computer in silicon

Down-scaling has been the leading paradigm of the semiconductor industry since the invention of the first transistor in 1947. However miniaturization will soon reach the ultimate limit, set by the discreteness of matter, leading to intensified research in alternative approaches for creating logic devices. One of the most exciting of these is quantum computation. We will present devices that address the ultimate limit of device miniaturization in silicon where we have patterned dopants in a crystalline environment with atomic precision to act as one dimensional leads, single electron transistors and control gates. In particular we demonstrate precision single atom transistors and spin-read-out in a silicon quantum computing architecture that is inherently scalable. We will discuss the benefits of donors as qubits and address some of the challenges to achieving truly atomically precise devices in all three spatial dimensions.

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Conference Agenda Overview

Wednesday, December 4, 2013

Registration ..... 6:00 PM – 8:00 PM
Evening Tutorial ..... 8:00 PM – 9:30 PM
Hospitality Room ..... 9:30 PM – Midnight

Thursday, December 5, 2013

Registration ..... 8:00 AM – 5:00 PM
Session 1 – Ge MOSFETs I ..... 8:00 AM – 9:30 AM
Session 2 – Ge MOSFETs II ..... 10:00 AM – 11:05 AM
Session 3 – Poster Session I Preview ..... 11:05 AM – 12:05 PM
Session 4 – Two-Dimensional Materials I ..... 1:30 PM – 2:45 PM
Session 5 – Two-Dimensional Materials II ..... 2:45 PM – 3:45 PM
Session 6 – RRAM ..... 4:15 PM – 5:15 PM
Session 7 – Poster Session I Preview (continued) ..... 5:15 PM – 6:00 PM
Poster Session I ..... 6:00 PM – 10:00 PM
Hospitality Room ..... 10:00 PM – Midnight

Friday, December 6, 2013

Registration ..... 8:00 AM – Noon
Session 8 – III-V I ..... 8:00 AM – 9:40 AM
Session 9 – III-V II ..... 10:10 AM – 11:50 AM
Technical Committee / Invited Speaker Luncheon ..... 11:50 AM – 1:30 PM
Session 10 – III-V/High-k ..... 1:30 PM – 2:45 PM
Session 11 – Poster Session II Preview ..... 2:45 PM – 3:45 PM
Session 12 – Poster Session II Preview (continued) ..... 4:15 PM – 5:00 PM
Poster Session II ..... 5:00 PM – 7:00 PM
Conference Banquet and Limerick Contest ..... 7:00 PM – 10:00 PM
Hospitality Room ..... 10:00 PM – Midnight

Saturday, December 7, 2013

Session 13 – High-k/III-V ..... 8:00 AM – 9:05 AM
Session 14 – Reliability ..... 9:05 AM – 10:10 AM
Session 15 – High-k ..... 10:40 AM – 12:15 PM

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Conference Program

Wednesday, December 4, 2013

Tutorial

Session Chair: A. Demkov

8:00 PM – 9:30 PM *Tutorial* - The development of a quantum computer in silicon, M. Simmons, U. of New South Wales, Australia

9:30 PM – Midnight Hospitality Room

Thursday, December 5, 2013

8:00 AM Welcome and opening remarks

Session 1 – Ge MOSFETs I

Session Chair: C. Young

8:10 AM Opening remarks

8:15 AM 1.1 *Invited* - **Schottky Barrier Height Engineering for Low Resistance Contacts to Ge and III-V Devices,** K. Saraswat, J.-Y. Lin, A. Nainani, A. Roy, G. Shine, and Z. Yuan, *Stanford U.*

8:50 AM 1.2 - **High-k/Ge Gate Stack with an EOT of 0.56 nm by Controlling Interface Reaction Using Ultrathin AlO_x Interlayer,** T. Hosoi[1], I. Hideshima[1], R. Tanaka[1], Y. Minoura[1], A. Yoshigoe[2], Y. Teraoka[2], T. Shimura[1], and H. Watanabe[1], *[1]Osaka U., Japan, [2]Japan Atomic Energy Agency, Japan*

9:10 AM 1.3 - **Impact of Ge composition on the interface trap density at $Al_2O_3/Si_{1-x}Ge_x$ MOS interface with plasma post-nitridation,** J.-H. Han[1], R. Zhang[1], T. Osada[2], M. Hata[2], M. Takenaka[1], and S. Takagi[1], *[1]U. of Tokyo, Japan, [2]Sumitomo Chemical, Japan*

9:30 AM Break

Session 2 - Ge MOSFETs II

Session Chair: K. Saraswat

10:00 AM Opening Remarks

10:05 AM 2.1 - **Ultra-scaled Junctionless MOSFETs on GeOI Substrates,** H. Wu, X. F. Li, L. Dong, J. J. Gu, N. J. Conrad, J. Y. Zhang, and P. D. Ye, *Purdue U.*

10:25 AM 2.2 - **Very High Stoichiometric GeO_2 in Interfacial Layer of Ge MOS Devices by In-situ H_2O Plasma Process,** L.-J. Liu, K.-S. Chang-Liao, C.-H. Fu, T.-C. Chen, C.-C. Li, J.-W. Cheng, C.-C. Lu, T.-M. Lee, L.-T. Chen, S.-H. Yi, and T.-K. Wang, *National Tsing Hua U., Taiwan*

10:45 AM 2.3 - **Post-Gate Fluorine Incorporation by CF_4 Plasma on Very High κ Tetragonal ZrO_2/Ge Gate Stack with Ultrathin EOT of 0.4 nm,** C.-H. Huang, C.-M. Lin, H.-C. Chang, and C. W. Liu, *National Taiwan U., Taiwan*

Session 3 - Poster Session I Preview

Session Chair: R. Wallace

11:05 AM Opening remarks

3.1 - **Controlled H_2 annealing in aggressively scaled multi-fin SOI FinFETs: performance and electrostatics enhancement by fin surface smoothening,** A. Paul[1], C. C. Yeh[2], S. Mochizuki[2], A. F. Bello[1], H. Bu[2], and M. Khare[2], *[1]GLOBALFOUNDRIES, [2]IBM*

3.2 - **Resonant tunneling in CVD Graphene-Insulator-Graphene devices with atomic layer deposited high-k tunnel dielectrics,** T. Roy[1], Z. R. Hesabi[1], B. Chakrabarti[2,1], C. A. Joiner[1], and E. M. Vogel[1], *[1]Georgia Institute of Technology, [2]UT Dallas*

3.3 - **Theoretical Studies on NO Initial Oxidation Process of 4H-SiC Surface,** K.Endo[1], S.Maruyama[1], S.Kato[1], K.Chokawa[1], K.Kamiya[1], K.Shiraishi[1,2], *[1]U. of Tsukuba, Japan, [2]Nagoya U., Japan*

3.4 - **Hafnia-Hafnium Interface in RRAM Devices: Theoretical Investigation,** A. O'Hara[1], G. Bersuker[2], and A. A. Demkov[1], *[1]UT Austin, [2]SEMATECH*

3.5 - **Resistive Memory Effects on Nanoparticles Formed Using Biotemplate,** M. Uenuma, I. Yamashita, and Y. Uraoka, *Nara Institute of Science and Technology, Japan*

3.6 - **Silicon-Passivated Germanium-Tin: An Angle-Resolved X-Ray Photoelectron Spectroscopy Study of Surface Segregation Effects,** P. Guo[1], R. Cheng[1], W. Wang[1], Z. Zhang[2], J. Pan[2], E. S. Tok[1], and Y.-C. Yeo[1], *[1]National U. of Singapore, Singapore, [2]A*STAR, Singapore*

3.7 - **Study of SiO_x-Based Resistive Switching Memory by Nano-Sphere Lithography,** Y. F. Chang[1], L. Ji[1], P. Y. Chen[1], F. Zhou[1], F. Xue[1], B. Fowler[2], E. T. Yu[1], and J. C. Lee[1], *[1]UT Austin, [2]PrivaTran, LLC*

3.8 - **C-C Defect Generation at Interface of SiC and SiO_2 Induced by Oxidation,** K. Chokawa[1,2], K. Kamiya[2], and K. Shiraishi[1], *[1]Nagoya U., Japan, [2]U. of Tsukuba, Japan*

3.9 - **Utilization of Defect State Mixing in SDR and SDT at Zero- & Low-Magnetic Fields to Study Bias Temperature Instabilities in MOSFETs and Time Dependent Dielectric Breakdown in Thin Film Dielectrics,** C. J. Cochrane and P. M. Lenahan, *Penn State U.*

3.10 - **Chemical Bonding and Contact Resistivity of Metal Contacts on MoS_2,** S. McDonnell, C. Buie, A. Azcatl, R. M. Wallace, and C. L. Hinkle, *UT Dallas*

3.11 - **Integration of ferroelectric $BaTiO_3$ on Ge (001),** K. D. Fredrickson[1], P. Ponath[1], A. B. Posadas[1], M. R. McCartney[2], D. J. Smith[2], and A. A. Demkov[1], *[1]UT Austin, [2]Arizona State U.*

3.12 - **Graphene Field-Effect Transistor Based on Lateral Tunneling,** A. Orlikovsky[1], D. Svintsov[1], V. Vyurkov[1], V. Ryzhii[2], and T. Otsuji[2], *[1]Russian Academy of Sciences, Russia, [2]Tohoku U., Japan*

3.13 - **Effect of Tunnel Barrier Engineering on Improvement of Non-linearity in Resistive Switching Characteristics of Hetero-junction Device,** J. Kim and H. Sohn, *Yonsei U., Korea*

3.14 - **Limiting factors in SiC Inversion Layer Mobility,** G. Liu[1], Y. Xu[1], S. Shubeita[1], H. Lee[1], V. Amarasinghe[1], A. Ahyi[2], T. Isaacs-Smith[2], F. Wang[3], E. Conrad[3], J. Williams[2], S. Dhar[2], G. Celler[1], E. Garfunkel[1], T. Gustafsson[1], and L. C. Feldman[1], *[1]Rutgers U., [2]Auburn U., [3]Georgia Institute of Technology*

3.15 - **MoX_2 (X=S,Se,Te) as possible substrates for the growth of silicene: A theoretical study,** E. Scalise[1], B. van den Broek[1], G. Pourtois[2], V. V. Afanas'ev[1], A. Stesmans[1], and M. Houssa[1], *[1]U. of Leuven, Belgium, [2]imec, Belgium*

3.16 - **Mobility Enhancement and Slow Traps Reduction in Interfacial Layer-Free Al_2O_3/Ge pMOSFETs with Ozone Post Annealing,** J. Sun[1], R. Zhang[1], W. Wu[1], Y. Shi[1], and Y. Zhao[1,2], *[1]Nanjing U., China, [2]Zhejiang U., China*

3.17 - **Investigation of degradation mechanisms of Low Resistance State through disturb measurements in HfO_2-ReRAM integrated in a 65nm CMOS Technology,** T. Diokh[1,2], S. Jeannot[1], E. Le-Roux[1], S. Blonkowski[1], L. Perniola[2], J. F. Nodin[2], P. Candelier[1], and B. De Salvo[2], *[1]STMicroelectronics, France, [2]CEA-LETI, France*

3.18 - **Identifying Resonant States at InGaAs and Ge - Oxide Interfaces,** H. Li, Y. Guo, and J. Robertson, *Cambridge U., UK*

3.19 - **Ultra-low 1/f Noise in Top Gated Epitaxial Graphene Field Effect Transistors,** H. K. Chan[1], V. D. Wheeler[2], V. K. Nagareddy[1], L. O. Nyakiti[3], A. Nath[4], R. L. Myers-Ward[4], Z. R. Robinson[3], N. Y. Garces[2], M.V. Rao[4], J. P. Goss[1], N. G. Wright[1], C. R. Eddy Jr[2], D. K. Gaskill[2], and A. B. Horsfall[1], *[1]Newcastle U., UK, [2]U.S. Naval Research Laboratory, [3]American Society of Engineering Education, [4]George Mason U.*

3.20 - **Surface band bending and band alignment of PEALD dielectrics on n- and p-type GaN with different polarities,** J. Yang, B. S. Eller, and R. J. Nemanich, *Arizona State U.*

12:05 PM Adjourn for Lunch

Session 4 - Two-Dimensional Materials I

Session Chair: M. Houssa

1:30 PM Opening remarks

1:35 PM 4.1 *Invited* - **Growth and characterization of Silicene, Germanene and other 2D layered materials,** A. Dimoulas, D. Tsoutsou, E. Xenogiannopoulou, E. Golias, P. Tsipas, and S. Kassavetis, *NCSR DEMOKRITOS, Greece*

2:10 PM 4.2 *Invited* - **SymFET: A novel Graphene-Insulator-Graphene Tunneling Device,** D. Jena, *U. of Notre Dame*

Session 5 - Two-Dimensional Materials II

Session Chair: P. Ye

2:45 PM 5.1 - **Doping, Band offsets, Sulfur Vacancies and Electrical Contacts in MoS_2,** Y. Guo[1], D. Liu[2], and J. Robertson[1], *[1]Cambridge U., UK, [2]Tsinghua U., China*

3:05 PM 5.2 - **Monitoring of interfacial reactions using discharging current from graphene FETs,** U. Jung, J. E. Lee, Y. G. Lee, Y. J. Kim, and B. H. Lee, *Gwangju Institute of Science and Technology, Korea*

3:25 PM 5.3 - **Epitaxial Graphene Oxide Films: Order, Structure and Elasticity,** S. Zhou[1], S. Kim[1], C. Gong[2], C. Berger[1], W. de Heer[1], E. Riedo[1], Y. J. Chabal[2], C. Aruta[3], and A. Bongiorno[1], *[1]Georgia Institute of Technology, [2]UT Dallas, [3]U. of Rome, Italy*

3:45 PM Break

Session 6 - RRAM

Session Chair: M. Passlack

4:15 PM Opening remarks

4:20 PM 6.1 *Invited* - **Modeling SET and RESET transients in Hf-based RRAM devices using the Hourglass approach,** R. Degraeve[1], A. Fantini[2], N. Raghavan[1,2], Y. Y. Chen[1,2], L. Goux[1], S. Clima[1], S. Cosemans[1], B. Govoreanu[1], D. J. Wouters[1,2], Ph. Roussel[1], G. S. Kar[1], G. Groeseneken[1,2], and M. Jurczak[1], *[1]imec, Belgium, [2]U. of Leuven, Belgium*

4:55 PM 6.2 - **Ti Thickness-Dependent Improved Non-Linearity in TiO_2-Based 1T1R Memory Element,** W. Banerjee[1,2], B. Roesgen[1,2], F. Lentz[1,2], V. Rana[1,2], and R. Waser[1,2,3], *[1]Forschungszentrum Jülich, Germany, [2]JARA, Germany, [3]RWTH Aachen U., Germany*

Session 7 - Poster Session I Preview (continued)

Session Chair: A. Demkov

5:15 PM Opening remarks

7.1 - **Robust Interfacial Layer Y-doped GeO_2 for Scalable EOT Ge Gate Stacks,** C. H. Lee[1,2], C. Lu[1,2], T. Nishimura[1,2], K. Nagashio[1,2], and A. Toriumi[1,2], *[1]U. of Tokyo, Japan, [2]JST-CREST, Japan*

7.2 - **Improvement on MIS Properties of Single-Grain Germanium by Pulsed-Laser Annealing,** P. Sun, M. van der Zwan, A. Arslan, E. Charbon, and R. Ishihara, *Delft U. of Technology, The Netherlands*

7.3 - **Functionalizing SiGe(100) via HOOH(g) Dosing,** T. Kaufman-Osborn, A. Kerr, and A. C. Kummel, *UC San Diego*

7.4 - **Improvement of structure and electrical properties of Al_2O_3/Ge gate stacks by post-deposition O_2 oxidation,** X. Li, X. Liu, X. Li, Y. Cao, D. Wu, and A. Li, *Nanjing U., China*

7.5 - **Schottky Barrier Modulation Using Ultrathin MgO on Ge and Si,** C. Y. Su, R. Lieten, M. Menghini, and J. P. Locquet, *U. of Leuven, Belgium*

7.6 - **Asymmetric behavior in transition metals-silicon interfaces,** M.Ibrahim[1] , P.Stender[1], B. Parditka[2], Z.Balogh[1], A.Fuhrich[1], Z. Erdélyi[2], and G.Schmitz[1], *[1]U. of Münster, Germany, [2]U. of Debrecen, Hungary*

7.7 - **Polymer-Graphene Interference Signature of Trenched Graphene Field-Effect Transistor.,** J. E. Jin[1], I. Nam[1,2], J. Choi[1], H. Yun[3], M.-K. Joo[1], J. Na[1], B. C. Lee[1], A. Choi[1], S. W. Lee[3], U. Dettlaff-Weglikowska[1], and G. T. Kim[1], *[1]Korea U., Korea, [2]Samsung, Korea, [3]Konkuk U., Korea*

7.8 - **Band alignment of ZnO as a Channel Layer between SiO_2 and Al_2O_3,** M. Kaur, J. Yang, X. Wang, and R. J. Nemanich, *Arizona State U.*

7.9 - **Structural and Electrical Characterization of hexagonal $GdScO_3$,** A. Schaefer[1,2], A. Winden[1,2], H. Hardtdegen[1,2], M. Luysberg[1], T. Schroeder[3], and J. Schubert[1,2], *[1]Forschungszentrum Jülich, Germany, [2]JARA, Germany, [3]IHP, Germany*

7.10 - **Time-evolution of Roughening Process on Atomically Flat Ge (111) Surface by Diluted H_2O_2 Solution,** W. F. Zhang[1,2], T. Nishimura[1,2], K. Nagashio[1,2], and A. Toriumi[1,2], *[1]U. of Tokyo, Japan, [2]JST-CREST, Japan*

7.11 - **Quantum Computer in MOSFET Channel: Coulomb Blockade for Measurement,** V. Vyurkov, A. Orlikovsky, D. Svintsov, and M. Rudenko, *Russian Academy of Sciences, Russia*

7.12 - **Energy Barrier Height Engineering by Inserting Interfacial Layers for Improvement of III-V MIS Gate Stacks Reliability,** S. Yoshida[1], S. Taniguchi[1], H. Minari[1], D. Lin[2], T. Ivanov[2,3], and M. Nakazawa[1], *[1]Sony, Japan, [2]imec, Belgium, [3]U. of Leuven, Belgium*

7.13 - **A physical absorption dominant ALD growth of Al_2O_3 on graphene for graphene-based devices,** Y. Zhang, L. Wang, Z. Qiu and R. Liu, *Fudan U., China*

6:00 PM Adjourn

Poster Session I

Session Chairs: R. Wallace and A. Demkov

6:00 PM – 10:00 PM Poster Session I

10:00 PM – Midnight Hospitality Room

Friday, December 6, 2013

Session 8 - III-V I

Session Chair: J. Lisoni

8:00 AM Welcome and opening remarks

8:05 AM 8.1 *Invited* - **Overcoming critical instabilities at the interfaces of scaled $HfO_2/Al_2O_3/Si$ gate stacks on $In_{0.53}Ga_{0.47}As$-On-Insulator,** C. Marchiori[1], M. El Kazzi[1], L. Czornomaz[1], D. Pierucci[2], M. Silly[2], F. Sirotti[2], E. Uccelli[1], M. Sousa[1], and J. Fompeyrine[1], *[1]IBM, Switzerland, [2]Synchrotron SOLEIL, France*

8:40 AM 8.2 - **Determination of Border Trap Density, Interface Trap Density, and Surface Potential Fluctuation on GaAs MOS Capacitors from a Single Conductance Spectrum,** X. Li[1], L. Dong[1], J. Zhang[1], X. Wang[2], X. Lou[2], R. G. Gordon[2], and P. D. Ye[1], *[1]Purdue U., [2]Harvard U.*

9:00 AM 8.3 - **On the Temperature dependence of Frequency dispersion in C-V Measurements of III-V MOS Devices and its application in spatial profiling of Border Traps,** A. Vais[1,3], D. Lin[1], C. Dou[2], Y. Yuan[4], K. Martens[1], T. Ivanov[1] , N. Collaert[1], K. DeMeyer[1,3], A. Thean[1], and Y. Taur[4], *[1]imec, Belgium, [2]Tokyo Institute of Technology, Japan, [3]U. of Leuven, Belgium, [4]UC San Diego*

9:20 AM 8.4 - **Electronic structure of (In)GaAs surfaces and native-oxide free high k interfaces – Synchrotron radiation photoemission studies,** A. T. W. Pi[1], B. T. D. Lin[2], C. T. H. Chiang[3], D. Y. T. Liu[3], E. Y. C. Chang[2], F. C. H. Wei[1], G. G. K. Wertheim[4], H. J. Kwo[3], and I. M. Hong[2], *[1]National Synchrotron Radiation Research Center, Taiwan, [2]National Taiwan U., Taiwan, [3]National Tsing Hua U., Taiwan, [4]Woodland Consulting*

9:40 AM Break

Session 9 - III-V II

Session Chair: F. Martin

10:10 AM Opening remarks

10:15 AM 9.1 *Invited* - **Heavily doped epitaxially grown source in InGaAs MOSFET for high drain current density,** Y. Miyamoto[1], T. Kanazawa[1], Y. Yonai[1], A. Kato[1], K. Ohsawa[1], M. Oda[2], T. Irisawa[2], and T. Tezuka[2], *[1]Tokyo U. of Technology, Japan, [2]AIST, Japan*

11:50AM 9.2 - **Perfecting high κ/GaSb(100) interface using molecule beam epitaxy Y_2O_3,** R. L. Chu[1], W. J. Hsueh[2], T. H. Chiang[1], W. C. Lee[1], H. Y. Lin[1], T. D. Lin[3], C. H. Fu[3], G. J. Brown[4], T. W. Pi[5], J. I. Chyi[2], J. Kwo[1], and M. Hong[3], *[1]National Tsing Hua U., Taiwan, [2]National Central U., Taiwan, [3]National Taiwan U., Taiwan, [4]Air Force Research Laboratory (AFRL), [5]National Synchrotron Radiation Research Center, Taiwan*

11:10 AM 9.3 - **Reduction in Interface State Density in $GaSb/Al_2O_3$ Structures via Hydrogen Plasma Exposure,** L. B. Ruppalt, E. R. Cleveland, J. G. Champlain, B. R. Bennett, J. B. Boos, and S. M. Prokes, *U.S. Naval Research Laboratory*

11:30 AM 9.4 - **Electrical properties of metal/GaSb junctions using metal-GaSb alloys,** K. Nishi[1], M. Yokoyama[1], S. H. Kim[1], H. Yokoyama[2], M. Takenaka[1], and S. Takagi[1], *[1]U. of Tokyo, Japan, [2]NTT Corporation, Japan*

11:50 AM Adjourn for lunch

11:50 AM – 1:30 PM Committee / Invited Speaker Luncheon

Session 10 – III-V/High-k

Session Chair: J. Robertson

1:30 PM Opening Remarks

1:35 PM 10.1 *Invited* - **Reducing EOT and Interface Trap Densities of High-k/III-V Gate Stacks,** S. Stemmer[1], V. Chobpattana[1], R. Engel-Herbert[2], B. Mazumder[1], T. E. Mates[1], and W. J. Mitchell[1], *[1]UC Santa Barbara, [2]Penn State U.*

2:10 PM 10.2 *Invited* - **Materials Selection and Device Design for Low Power Tunnel Transistors,** S. Datta, *Penn State U.*

Session 11 - Poster Session II Preview

Session Chairs: M. Frank and A. Demkov

2:45 PM Opening remarks

11.1 - **Photo-CV Analysis for Positive Valence Band-Offset Dielectrics (Al_2O_3, SiO_2) on GaN and Dielectric Stress Tests correlating Performance to Measured Trap Values,** R. Yeluri, X. Liu, O. Koksaldi, M. Guidry, S. Lal, J. Kim, B. L. Swenson, J. Lu, A. Raman, S. Keller, and U. K. Mishra, *UC Santa Barbara*

11.2 - **A Novel Tunnel Dielectric Based Tunnel FET (TD-TFET) with 36mV/dec SS,** Z. Luo, H. Wang, N. An, Z. Zhu, and J. Liu, *Chinese Academy of Sciences, China*

11.3 - **Passivation of the InGaAs (001)-(2x4) Surface using both an oxidant and a reductant,** T. Kent, M. Edmonds, E. Chagarov, and A. C. Kummel, *UC San Diego*

11.4 - **Inherent interface defects at the thermal (211)Si/SiO_2 interface,** S. Iacovo and A. Stesmans, *U. of Leuven, Belgium*

11.5 - **Total Ionizing Dose (TID) Effects on Ultra-thin InGaAs Nanowire Gate-All-Around MOSFETs with ALD Al_2O_3 Gate Dielectrics,** S. Ren[1], X. Sun[1], M. Si[2], E. X. Zhang[3], J. Chen[4], D. M. Fleetwood[3], P. D. Ye[2], S. Cui[1], and T. P. Ma[1], *[1]Yale U., [2]Purdue U., [3]Vanderbilt U., [4]Peking U., China*

11.6 - **Gate-All-Around Poly-Si Nanowire Memory Devices with Bandgap-Engineered HfAlO Trapping Layer,** K.-H. Lee[1], T.-T. Wen[1], J.-R. Tsai[2], H.-C. Lin[1,3], and T.-Y. Huang[1], *[1]National Chiao Tung U., Taiwan, [2]Asia U., Taiwan, [3]National Nano Device Laboratories, Taiwan*

11.7 - **Towards vertical sidewalls in III-V FinFETs: dry etch processing and its associated damage on the electrical and physical properties of (100)-oriented InGaAs.,** O. Ignatova[1], U. Peralagu[1], X. Li[1], M. Steer[1], M. Mirza[1], J. Lin[2], I. Povey[2], P. Carolan[2], K. Cherkaoui[2], P. Hurley[2], and I. Thayne[1], *[1]U. of Glasgow, UK, [2]Tyndall National Institute, Ireland*

11.8 - **Atomic Scaling Imaging of In-Situ Cleaning and ALD Gate Oxide Nucleation on GaAs(110) and InGaAs(110),** M. Edmonds[1], T. Kent[1], R. Droopad[2], E. Chagarov[1], A. C. Kummel[1], *[1]UC San Diego, [2]Texas State U.*

11.9 - **Higher-k stack using a TiO_2 capping layer compatible with gate last processing to achieve 7Å EOT with reduced leakage, suppressed EWF roll-off, and improved reliability,** J. Rozen, T. Ando, E. Cartier, M. M. Frank, S. L. Brown, J. Bruley, A. J. Kellock, and V. Narayanan, *IBM*

11.10 - **Effect of Forming Gas Anneal on High-k/Ge Interface,** L. Zhang and P. C. McIntyre, *Stanford U.*

11.11 - **Impact of interfacial InAs layers on GaSb MOS interface properties,** M. Yokoyama[1], H. Yokoyama[2], M. Takenaka[1], and S. Takagi[1], *[1]U. of Tokyo, Japan, [2]NTT Corporation, Japan*

11.12 - **Coulomb Interaction on Multi-electron Wave Packet Dynamics in Nanoscale Channels,** T. Shiokawa[1], G. Fujita[1], Y. Takada[2], S. Konabe[1,5], M. Muraguchi[4,5], T. Yamamoto[2], T. Endoh[3,4,5], Y. Hatsugai[1,4] and K. Shiraishi[1,4], *[1]U. of Tsukuba, Japan, [2]Tokyo U. of Science, Japan, [3]Tohoku U., Japan, [4]Nagoya U., Japan, [5]JST-CREST, Japan*

11.13 - **Density Functional-Based Tight Binding for Atomic Level Simulation of Electron Devices Including the Semiconductor-Oxide Interfaces,** S. Markov, C. Y. Yam, and G. H. Chen, *U. of Hong Kong, China*

11.14 - **Bulk Oxide Defect Characterization of InGaAs Nanowire MOSFETs Using AC Transconductance Dispersion Method,** N. J. Conrad, J. Gu, and P. D. Ye, *Purdue U.*

11.15 - **Improved Properties of GaSb MOS Devices Passivated with Acidic $(NH_4)_2S$ Solution,** L. Zhao, Z. Tan, J. Wang, and J. Xu, *Tsinghua U., China*

11.16 - **Fluorine Interface Treatments within the Gate Stack for Defect Passivation in 28nm HKMG Technology,** M. Drescher[2], E. Erben[1], M. Trentzsch[1], C. Grass[1], M. Hempel[1], A. Naumann[2], J. Sundqvist[2], J. Schubert[3], J. Szillinski[3], A. Schäfer[3], and S. Mantl[3], *[1]GLOBALFOUNDRIES, Germany, [2]Fraunhofer IPMS-CNT, Germany, [3]Forschungszentrum Jülich, Germany*

11.17 - **ESR parameters of defects at GaAs/oxide interfaces: A first-principles study,** M. Houssa, V. V. Afanas'ev, and A. Stesmans, *U. of Leuven, Belgium*

11.18 - **High-Contrast Multi-bit Processing in Spatial Wavefunction Switched (SWS) FETs Incorporating Hybrid Quantum Well and Quantum Dot Channels,** F. Jain[1], P.-Y. Chan[1], M. Lingalugari[1], J. Kondo[1], E. Suarez[1], P. Gogna[1,2], J. Chandy[1], and E. Heller[3], *[1]U. of Connecticut, [2]Intel, [3]Synopsys*

3:45 PM Break

Session 12 - Poster Session II Preview (continued)

Session Chairs: M. Frank and A. Demkov

4:15 PM Opening remarks

12.1 - **Characterization and Engineering of High-k/InP Interfaces,** H. Dong[1], R. Galatage[1], W. Cabrera[1], K. C. Santosh[1], S. McDonnell[1], X. Qin[1], D. M. Zhernokletov[1], J. Kim[1], K. Cho[1], C. L. Hinkle[1], Y. J. Chabal[1], E. M. Vogel[2], and R. M. Wallace[1], *[1]UT Dallas, [2]Georgia Institute of Technology*

12.2 - **Effect of SiH_4 surface passivation on the band alignment of $HfO_2/Al_{0.25}Ga_{0.75}N$ interface,** M. H. S. Owen[1], M. A. Bhuiyan[1], Q. Zhou[1], Z. Zhang[2], J. S. Pan[2], and Y.-C. Yeo[1], *[1]National U. of Singapore, Singapore, [2]A*STAR, Singapore*

12.3 - **X-ray Induced Electron Trapping in AlGaN/GaN HEMTs,** J. Yang, X. Sun, S. Ren, S. Cui, and T. P. Ma, *Yale U.*

12.4 - **Direct Quantum Calculation of Contact Resistance,** P. A. Clifton, A. Goebel, and W. A. Harrison, *Acorn Technologies, Inc.*

12.5 - **Physical mechanism of the flatband voltage shift on Al_2O_3-incorporated high-k gate stacks,** M. Y. Yang[1], K. Kamiya[1], and K. Shiraishi[1,2], *[1]U. of Tsukuba, Japan, [2]Nagoya U., Japan*

12.6 - **Ultimately Scaled Sub-10nm V-Gate InGaAs MOSFETs,** M. Si, H. Wu, J. Y. Zhang, H. Liu, J. J. Gu, and P. D. Ye, *Purdue U.*

12.7 - **Band Offset Transitivity and Interfacial Electric Dipole at Oxide Heterojunctions,** X. L. Wang[1], W. W. Wang[1], J. J. Xiang[1], J. Zhang[2], H. Yang[1], J. Yan[1], C. Zhao[1], D. P. Chen[1], and T. C. Ye[1], *[1]Chinese Academy of Sciences, China, [2]North China U. of Technology, China*

12.8 - **Demonstration of InAlN/GaN Metal-Insulator-Semiconductor High-Electron-Mobility-Transistors with Atomic-Layer-Deposited $La_{1.8}Y_{0.2}O_3/Al_2O_3$ as Gate Insulator,** H. Zhou[1], N. J. Conrad[1], S. P. Guo[2], and P. D. Ye[1], *[1]Purdue U., [2]IQE RF, LLC*

12.9 - **A combinatorial approach to the rapid development of transparent conducting oxides,** R. E. Treharne, L. J. Phillips, K. Durose, A. D. Weerakkody, I. Z. Mitrovic, and S. Hall, *U. of Liverpool, UK*

12.10 - **Indium out-diffusion in InGaAs based gate stacks,** I.Krylov, A.Gavrilov, D.Ritter, and M.Eizenberg, *Technion, Israel*

12.11 - **Demonstration of Ni-GaSb metal S/D GaSb pMOSFETs with vacuum annealing on GaAs substrates,** T. Gotow[1,2], S. Fujikawa[1], H. I. Fujishiro[1], M. Ogura[2], T. Yasuda[2], and T. Maeda[1,2], *[1]Tokyo U. of Science, Japan, [2]AIST, Japan*

12.12 - **In-situ sulfur passivation of $In_{0.53}Ga_{0.47}As$ at elevated temperature by $(NH_4)_2S$ solution vapor and H_2S treatment in an ALD reactor,** F. Tang[1], Q. Xie[2], S.-H. Jung[1], M. Givens[1], J.W. Maes[2], and V. Machkaoutsan[2], *[1]ASM, [2]ASM, Belgium*

12.13 - **Detection and characterization of failure events in high-K dielectrics using transient IR thermography,** E. Miranda[1], M. Riccio[2], G. De Falco[2], J. Suñé[1], and A. Irace [2], *[1]Universitat Autònoma de Barcelona, Spain, [2]U. of Naples Federico II, Italy*

12.14 - **NBTI and PBTI Reliability Studies of Epitaxial La_2O_3 on GaAs(111)A,** J. Zhang[1], L. Dong[1], X. Wang[2], N. J. Conrad[1], R. G. Gordon[2], and P. D. Ye[1], *[1]Purdue U., [2]Harvard U.*

5:00 PM Adjourn

Poster Session II

Session Chair: M. Frank

5:00 PM – 7:00 PM Poster Session II

7:00 PM – 10:00 PM Conference Banquet and Limerick Contest

10:00 PM – Midnight Hospitality Room

Saturday, December 7, 2013

8:00 AM Morning announcements

Session 13 - High-k/III-V

Session Chair: A. Kummel

8:05 AM Opening remarks

8:10 AM 13.1 *Invited* - **Disorder Induced Gap States at the High-k/III-V Interface,** E. M. Vogel, *Georgia Institute of Technology*

8:45 AM 13.2 - **Enhanced direct bandgap photoluminescence from local Ge-on-insulator structures fabricated by lateral liquid-phase epitaxy: Material and strain engineering toward CMOS compatible group-IV photonics,** M. Matsue[1], Y. Yasutake[2], S. Fukatsu[2], T. Hosoi[1], T. Shimura[1], and H. Watanabe[1], *[1]Osaka U., Japan, [2]U. of Tokyo, Japan*

Session 14 - Reliability

Session Chair: V. V. Afanas'ev

9:05 AM Opening Remarks

9:10 AM 14.1 - **Performance and Reliability Improvement of Gate-Last HfO_2 MOSFETs Using High Pressure Hydrogen/Deuterium Annealing,** T. Ngai[1], K. Matthews[1], D. Veksler[1], S. Deora[1], D. C. Gilmer[1], G. Moore[2], B. Wu[2], J. Lew[2], T. Burroughs[3], M. Jahanbani[3], S. Vivekanand[3], C. Y. Kang[1], G. Bersuker[1], V. Kaushik[3], and P. D. Kirsch[1], *[1]SEMATECH, [2]Poongsan, Korea, [3]CNSE SUNY Albany*

9:30 AM 14.2 - **Negative bias temperature instabilities in SiGe-pMOSFETs with SiO_2/HfO_2 gate dielectrics,** G. X. Duan[1], C. X. Zhang[1], E. X. Zhang[1], D. M. Fleetwood[1], R. D. Schrimpf[1], R. A. Reed[1], D. Linten[2], and J. Mitard[2], *[1]Vanderbilt U., [2]imec, Belgium*

9:50 AM 14.3 - **NBTI-induced Variability Of Ultra-Scaled FDSOI MOSFETs: Experiment vs Simulation,** X. Garros[1], A. Subirats[1,2], C. Le Royer[1], G. Reimbold[1], and G. Ghibaudo[2], *[1]CEA-LETI, France, [2]IMEP-LAHC, France*

10:10 AM Break

Session 15 - High-k

Session Chair: P. Lenahan

10:40 AM Opening remarks

10:45 AM 15.1 - **$TiSi_x$/TiN full metal gates for dual-channel gate-first CMOS technology,** M. M. Frank, C. Cabral Jr, J. M. Dechene, C. Ortolland, Y. Zhu, E. D. Marshall, and M. P. Chudzik, *IBM*

11:05 AM 15.2 - **Dopant compensation in HfO_2 and other high K oxides,** H. Li, Y. Guo, and J. Robertson, *Cambridge U., UK*

11:25 AM 15.3 - **Exhaustive Photodepopulation Spectroscopy of Electron Traps in High-k Insulators,** V. V. Afanas'ev, W. C. Wang, F. Cerbu, M. Houssa, and A. Stesmans, *U. of Leuven, Belgium*

11:45 AM 15.4 - **Workfunction control in high-k/metal gate stacks employing TmSiO IL,** E. Dentoni Litta, P.-E. Hellström, and M. Östling, *KTH, Sweden*

12:05 PM Closing remarks

12:15 PM Adjourn

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