SISC 2016

47th IEEE Semiconductor Interface Specialists Conference

December 7-10, 2016
Catamaran Hotel, San Diego, CA
www.ieeesisc.org

CONFERENCE PROGRAM

General Chair: Valeri Afanas'ev

Program Chair: Chris Hinkle

Arrangements Chair: Matthias Passlack

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SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology," published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author for either an oral or a poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

Winner of the 2015 SISC Ed Nicollian Award for Best Student Paper:

Julien Borrel

STMicroelectronics / CEA-LETI / IEMN, France

"At 10nm node, what is the AC impact of dielectric insertions in contact initially meant to decrease the DC contact resistivity?"

with L. Hutin, O. Rozeau, M.-A. Jaud, S. Martinie, E. Dubois, and M. Vinet

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Wednesday Evening Tutorial

Wednesday, December 7, 2016, 8:00 PM

First introduced at SISC 2008, the Wednesday evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

T. Theis, Columbia U.

Materials, Devices, and Circuit Architectures for Future Electronics

The continuing evolution of silicon CMOS digital device technology is clearly approaching some important physical limits. Since roughly 2003, the increasing inability to reduce supply voltages combined with physical and economic constraints on power density and total power, has forced designers to limit clock frequencies even as devices have continued to shrink. Either the device physics or the system architecture must change in a fundamental way if computing is to escape this power-performance bottleneck. Recent years have therefore brought a large increase in research funding and interest in new electronic materials, new device concepts enabled by these materials, and new architectures for computing.

This tutorial will begin with a brief high-level survey of the physical possibilities for new approaches to digital computing – from "transistor-like" devices that would operate in more or less conventional circuits to the brave new world of quantum computing. Much of this vast research landscape remains unexplored. I will then survey in more detail two promising classes of digital switching devices that have been the focus of growing research efforts in the last ten years. Transistor-like "steep slope" devices promise to open a new low-voltage design space that is inaccessible to the conventional field effect transistor. Nanomagnetic devices combine the functions of memory and logic in a single device, raising the possibility of profound innovation in circuit and higher-level architecture. Because these device concepts seek to harness new physical principles for digital switching, they are driving interest in materials and heterostructures that are new to electronics. Since none of these emerging devices will be a "drop in" replacement for the FET, devices and circuits must be co-developed and co-optimized. Co-optimization of neuromorphic devices and architectures is one exciting and active research frontier. There will be more in coming years.

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Conference Agenda Overview

Wednesday, December 7, 2016

Registration ..... 6:00 PM – 8:00 PM
Evening Tutorial ..... 8:00 PM – 9:30 PM
Hospitality Room ..... 9:30 PM – Midnight

Thursday, December 8, 2016

Registration ..... 8:00 AM – 5:00 PM
Session 1 – 2D Materials I ..... 8:00 AM – 10:05 AM
Session 2 – Two-Dimensional Transport and Interfaces ..... 10:30 AM – 11:45 AM
Session 3 – Poster Preview Session 1 – 2D and GaN ..... 11:45 AM – 12:25 PM
Session 4 – Ferroelectrics I ..... 2:00 PM – 3:35 PM
Session 5 – III-Vs and Trapping ..... 4:00 PM – 5:35 PM
Session 6 – Poster Preview Session 2 – III-V Interfaces ..... 5:35 PM – 6:01 PM
Poster Session I ..... 7:00 PM – 10:00 PM
Hospitality Room ..... 10:00 PM – Midnight

Friday, December 9, 2016

Registration ..... 8:00 AM – Noon
Session 7 – Ge Interfaces ..... 8:00 AM – 10:00 AM
Session 8 – Ferroelectrics II ..... 10:25 AM – 12:00 PM
Session 9 – Poster Preview Session 3 – Ge and Oxides ..... 12:00 PM – 12:20 PM
Technical Committee / Invited Speaker Luncheon ..... 12:20 PM – 2:00 PM
Session 10 – Interfaces of Novel Materials and Applications ..... 2:00 PM – 3:40 PM
Session 11 – Poster Preview Session 4 – Si, High-k, Wide Bandgap Interfaces 3:40 PM – 4:30 PM
Poster Session II ..... 4:45 PM – 6:45 PM
Conference Banquet and Limerick Contest ..... 7:00 PM – 10:00 PM
Hospitality Room ..... 10:00 PM – Midnight

Saturday, December 10, 2016

Session 12 – 2D Materials II ..... 8:00 AM – 9:20 AM
Session 13 – III-V Interfaces ..... 9:50 AM – 11:25 AM
Session 14 – GaN and SiC ..... 11:25 AM – 12:25 PM

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Conference Program

Wednesday, December 7, 2016

Tutorial

Session Chair: C. L. Hinkle

8:00 PM – 9:30 PM *Tutorial* - **Materials, Devices, and Circuit Architectures for Future Electronics,** T. Theis, *Columbia U.*

9:30 PM – Midnight Hospitality Room

Thursday, December 8, 2016

8:00 AM Welcome and opening remarks

Session 1 – 2D Materials I

Session Chair: V. V. Afanas'ev

8:10 AM 1.1 *Invited* - **Addressing Process Integration Challenges for 2D Semiconductor Materials,** R. M. Wallace, *UT Dallas*

8:45 AM 1.2 - **Large Grain WSe_2 and WTe_2 Growth by MBE,** L. A. Walsh[1], R. Yue[1], Y. Nie[1], Q. Wang[1], A. T. Barton[1], N. Lu[1], C. M. Smyth[1], H. Zhu[1], J. Kim[1], Y. J. Chabal[1], L. Colombo[2], R. M. Wallace[1], M. J. Kim[1], K. Cho[1], and C. L. Hinkle[1], *[1]UT Dallas, [2]Texas Instruments*

9:05 AM 1.3 - **Scanning Tunneling Microscopy and Spectroscopy of Air Exposure Effects on Metal Dichalcogenides,** J. H. Park[1], S. Vishwanath[2], X. Liu[3], H. Zhou[2], S. M. Eichfeld[4], S. K. Fullerton-Shirey[5], J. A. Robinson[4], R. M. Feenstra[6], J. Furdyna[3], D. Jena[2], H. G. Xing[2], and A. C. Kummel[1], *[1]UCSD, [2]Cornell U., [3]U. Notre Dame, [4]Penn State U., [5]U. Pittsburgh, [6]CMU*

9:25 AM 1.4 - **Point defects in MoS_2: comparison between DFT simulations and ESR experiments,** M. Houssa[1], K. Iordanidou[1], G. Pourtois[2], V. V. Afanas'ev[1], and A. Stesmans[1], *[1]U. Leuven, Belgium, [2]imec, Belgium*

9:45 AM 1.5 - **2D/3D Interfaces: Where the Magic Happens,** J. A. Robinson and D. D. Deng, *Penn State U.*

10:05 AM Coffee break

Session 2 - Two-Dimensional Transport and Interfaces

Session Chair: W. Zhu

10:30 AM 2.1 *Invited* - **Interface Engineering for High Performance Insulator-Protected MIS Photosynthesis Cells,** P. C. McIntyre, *Stanford U.*

11:05 AM 2.2 - **WSe_2 P-type Transistors Fabricated by Self-Assembled Monolayer for Contact Metal Patterning and Ultrathin Gate Dielectrics,** W. Du[1,2,3], T. Kawanago[1,2,3], and S. Oda[1,2,3], *[1]QNERC, Japan, [2]Institute of Innovative Research, Japan, [3]Tokyo Institute of Technology, Japan*

11:25 AM 2.3 - **Towards Nitride–based Dielectric Environment for High Performance MoS_2 FETs,** S. Bhattacharjee, K. L. Ganapathi, H. Chandrasekar, T. Paul, S. Mohan, A. Ghosh, S. Raghavan, and N. Bhat, *IIS Bangalore, India*

Session 3 - Poster Preview Session 1 – 2D and GaN

Session Chair: R. M. Wallace

11:45 AM Opening remarks

11:47 AM 3.1 - **Impact of Ultra-High Vacuum Metal Deposition on Few-Layer MoS_2, Top-Gate Field-Effect-Transistors,** P. Bolshakov[1], P. Zhao[1], C. M. Smyth[1], A. Azcatl[1], P. K. Hurley[2], R. M. Wallace[1], and C. D. Young[1], *[1]UT Dallas, [2]Tyndall National Institute, Ireland*

11:49 AM 3.2 - **Band alignment at monolayer MoS_2 and high-k oxide interface by internal photoemission,** Q. Zhang[1,2], W. Li[2,3], A. G. Birdwell[4], O. A. Kirillov[2], G. Cheng[2], X. Liang[3], A. R. Hight Walker[2], D. J. Gundlach[2], and N. V. Nguyen[2], *[1]Theiss Research, [2]NIST, [3]Peking U., China, [4]US Army Research Laboratory*

11:51 AM 3.3 - **ESR study of p-type natural 2H-polytype MoS_2 crystals: The As acceptor activity,** A. Stesmans, S. Iacovo, and V. V. Afanas'ev, *U. Leuven, Belgium*

11:53 AM 3.4 - **High energy x-ray photoelectron spectroscopy of Fermi level alignment and Schottky barrier heights on metal - MoS_2 interfaces,** C. McGeough[1], T. Cafolla[1], P. K. Hurley[2], R. M. Wallace[3], and G. Hughes[1], *[1]Dublin City U., Ireland, [2]Tyndall National Institute, Ireland, [3]UT Dallas*

11:55 AM 3.5 - **Novel Two-dimensional GeSe-MoS_2 PN Heterojunctions,** W. C. Yap and W. J. Zhu, *UIUC*

11:57 AM 3.6 - **Sulfurization in Sulfur Vapor for Sputtered-MoS_2 Film,** K. Matsuura[1], T. Ohashi[1], I. Muneta[1] S. Ishihara[2], N. Sawamoto[2], K. Kakushima[1], K. Tsutsui[1], A. Ogura[2], and H. Wakabayashi[1], *[1]Tokyo Institute of Technology, Japan, [2]Meiji U. Japan*

11:59 AM 3.7 - **The characterization of CVD growth MoS_2 Back Gate FET with Pd Contact Electrode for Monolayer Ultra-Thin Body Transistor,** M.-H. Hsu[1], F.-A. Tsai[1], L.-X. Luo[1], H.-Y. Huang[1], C.-H. Yeh[1], M.-H. Lee[2], S.-T. Chang[3], M.-C. Chen[4], K.-S. Li[4], L.-J. Li[5], C.-W. Yao[6], and M.-H. Liao[1], *[1]National Taiwan U., Taiwan, [2]National Taiwan Normal U., Taiwan, [3]National Chung Hsing U., Taiwan, [4]National Nano Device Laboratories, Taiwan, [5]King Abduliah U. of Science and Technology, Saudi Arabia, [6]Lamar U.*

12:01 PM 3.8 - **Low temperature ALD of High-K oxides on 2D materials,** I. Kwak, J. H. Park, and A. C. Kummel, *UCSD*

12:03 PM 3.9 - **Band Engineering, Doping and Tunnel FETs with InSe,** Y. Guo[1], H. Lu[2], and J. Robertson[2], *[1]U. Swansea, UK, [2]U. Cambridge, UK*

12:05 PM 3.10 - **Characterization of Black Phosphorus Capacitors with Boron Nitride Gate Dielectrics,** J. Liu and W. Zhu, *UIUC*

12:07 PM 3.11 - **Enhanced Electrical Stability in Recessed Gate GaN HEMTs on Si using Low-Temperature Atomic Layer Deposited-ZrO_2,** Y.-C. Byun, J.-G. Lee, A. T. Lucero, C. D. Young, M. J. Kim, and J. Kim, *UT Dallas*

12:09 PM 3.12 - **AlGaN/GaN MISHFETs with $GdScO_3$ gate dielectric and low interface trap density,** A. Schmid[1], S. Seidel[1], R. Otto[1], T. C. U. Tromm[2], J. Schubert[2], and J. Heitmann[1], *[1]TU Bergakademie Freiberg, Germany, [2]Forschungszentrum Jülich, Germany*

12:11 PM 3.13 - **Large Surface Potential Fluctuation at ALD-Al_2O_3/GaN MOS Interfaces,** N. Taoka[1], T. Kubo[2], T. Yamada[1], T. Egawa[2], and M. Shimizu[1], *[1]AIST, Japan, [2]Nagoya Institute of Technology, Japan*

12:13 PM 3.14 - **Electron-spin-resonance studies of AlGaN/GaN MIS-HEMT structures with Al_2O_3 and HfO_2 fabricated by atomic layer deposition,** T. Kubo and T. Egawa, *Nagoya Institute of Technology, Japan*

12:15 PM 3.15 - **Investigation of atomic layer etching process for AlGaN/GaN HEMT,** K. Kanomaru, J. Kataoka, T. Kikuchi, and S. Ishikawa, *Toshiba, Japan*

12:17 PM 3.16 - **Ultrathin Al_2O_3 Plasma-enhanced Atomic Layer Deposition on H_2O-pretreated InAlN/GaN MIS-HEMTs,** S. Ozaki[1,2], K. Makiyama[1,2], T. Ohki[1,2], A. Yamada[1,2], J. Kotani[1,2],Y. Niida[2], M. Sato[2], Y. Kamada[2], Y. Minoura[1,2], M. Sato[1,2], N. Okamoto[1,2], and N. Nakamura[1,2], *[1]Fujitsu, Japan, [2]Fujitsu Laboratories, Japan*

12:19 PM 3.17 - **Characteristics of Fe/pGaN Contact upon Annealing Process,** Y. Ikeuchi[1], T. Hoshii[1], H. Wakabayashi[1], K. Tsutsui[1], H. Iwai[1], K. Kakushima[1], and S. Ishikawa[2], *[1]Tokyo Institute of Technology, Japan, [2]Toshiba, Japan*

12:21 PM 3.18 - **Total ionizing dose effects on GaN-based HEMTs and MOSHEMTs: Effects of channel thickness and epitaxial MgCaO as gate dielectric,** M. Bhuiyan[1], H. Zhou[2], S.-J. Chang[3], X. Lou[4], X. Gong[4], K. Ni[5], R. Jiang[5], H. Gong[5], E. X. Zhang[5], C.-H. Won[6], R. G. Gordon[4], J.-W. Lim[3], J.-H. Lee[6], R. A. Reed[5], D. M. Fleetwood[5], P. D. Ye[2], and T. P. Ma[1], *[1]Yale U., [2]Purdue U., [3]ETRI, Korea, [4]Harvard U., [5]Vanderbilt U., [6]Kyungpook National U., Korea*

12:23 PM 3.19 - **Effects of Buffer Leakage on Breakdown Characteristics of AlGaN/GaN HEMTs with a High-k Passivation Layer,** Y. Satoh, H. Hanawa, and K. Horio, *Shibaura Institute of Technology, Japan*

12:25 PM Adjourn for lunch

Session 4 – Ferroelectrics I

Session Chair: M. Fischetti

2:00 PM 4.1 *Invited* - **Material Innovation Ferroelectric Hafnium Oxide: Towards Cheaper Memories, Steeper Slopes and New Value Adders for HKMG,** J. Müller[1], H. Mulaosmanovic[2], S. Müller[2,3], P. Polakowski[1], J. Ocker[2,3], M. Noack[2,3], S. Riedel[1], T. Ali[1], M. Peši?[2], U. Schröder[2], S. Slesazeck[2], T. Mikolajick[2,4], *[1]Fraunhofer, Germany, [2]NaMLab, Germany, [3]Ferroelectric Memory GmbH, Germany, [4]TU Dresden, Germany*

2:35 PM 4.2 - **Stabilizing ferroelectric HfO_2: Non-monoclinic phase formation and loss studied by temperature-dependent synchrotron X-ray diffraction,** M. M. Frank[1], A. Carr[1], J. L. Jordan-Sweet[1], C. Lavoie[1], D. Muir[2], B. Moreno[2], T. Ando[1], X. Sun[1], C.-W. Cheng[1], A. Pyzyna[1], and V. Narayanan[1], *[1]IBM Research, [2]Canadian Light Source, Canada*

2:55 PM 4.3 - **Influence of top electrode material on HfO_2 based OxRAM performances,** M. Azzaz[1,2], E. Vianello[2], B. Sklenard[2], E. Jalaguier[2], S. Blonkowski[1], A. Roule[2], S. Bernasconi[2], C. Charpin[2], C. Cagli[2], S. Jeannot[1], S. Denorme[1], P. Candelier[1], C. Fenouillet-Beranger[2], and L. Perniola[2], *[1]STMicroelectronics, France, [2]CEA LETI, France*

3:15 PM 4.4 - **Drawback of Large Coercive Fields in HfO_2-based Ferroelectric Thin Films from the Standpoint of Dielectric Breakdown,** S. Migita[1], H. Ota[1], H. Yamada[1], A. Sawa[1], and A. Toriumi[2], *[1]AIST, Japan, [2]U. Tokyo, Japan*

3:35 PM Coffee break

Session 5 – III-Vs and Trapping

Session Chair: L.-E. Wernersson

4:00 PM 5.1 *Invited* - **Perspective on III-V Tunnel-FETs: bridging the gap between ideal device design and experimental realizations through calibration,** A. S. Verhulst[1], Q. Smets[1], J. Bizindavyi[1,2], D. Verreck[1,2], S. El Kazzi[1], A. Alian[1], J. Franco[1], Y. Mols[1], A. Vandooren[1], R. Rooyackers[1], D. Lin[1], A. Mocuta[1], B. Sorée[1,2,3], G. Groeseneken[1,2], N. Collaert[1], and M. M. Heyns[1,2], *[1]imec, Belgium, [2]U. Leuven, Belgium, [3]U. Antwerp, Belgium*

4:35 PM 5.2 - **Characterization of Electrical and Physical Properties of $W/La_2O_3/InGaAs$ MOS Interfaces,** C.-Y. Chang[1,2], C. Yokoyama[1,2], M. Takenaka[1,2], and S. Takagi[1,2], *[1]U. Tokyo, Japan, [2]JST-CREST, Japan*

4:55 PM 5.3 - **Random Telegraph Noise on InGaAs Tunneling Field Effect Transistor,** M. Si[1], C.-J. Su[2], and P. D. Ye[1], *[1]Purdue U., [2]National Nano Device Laboratories, Taiwan*

5:15 PM 5.4 - **Rethinking Charge trapping and detrapping dynamic without the sheet-charge approximation,** K. P. Cheung, J. P. Campbell, and D. Veksler, *NIST*

Session 6 - Poster Preview Session 2 – III-V Interfaces

Session Chair: M. Houssa

5:35 PM 6.1 - **Trap characterization and capacitance-voltage hysteresis of Al_2O_3/InGaAs gate stacks,** K. Tang[1], F. Palumbo[2], R. Droopad[3], and P. C. McIntyre[1], *[1]Stanford U., [2]National Scientific and Technical Research Council, Argentina, [3]Texas State U.*

5:37 PM 6.2 - **Atomic structure of Al_2O_3/InAs(100) interface with a pre-oxidized (3×1)-O surface,** M. Tuominen[1], J. Mäkelä[1], J. Dahl[1], M. Yasir[1], J. Lång[1], M. Kuzmin[1], S. Granroth[1], M. Laitinen[2], R. Félix[3], M. P. J. Punkkinen[1], P. Laukkanen[1], and K. Kokko[1], *[1]U. Turku, Finland, [2]U. Jyvaskyla, Finland, [3]Helmholtz-Zentrum Berlin, Germany*

5:39 PM 6.3 - **Improvement of GaAsSb MOS interface properties by using ultrathin InGaAs interfacial layers,** T. Gotow[1,3], M. Mitsuhara[2,3], T. Hoshi[2,3], H. Sugiyama[2,3], M. Takenaka[1,3], and S. Takagi[1,3], *[1]U. Tokyo, Japan, [2]NTT Device Technology Laboratories, Japan, [3]JST-CREST, Japan*

5:41 PM 6.4 - **Temperature dependent border trap response produced by a defective interfacial oxide layer in Al_2O_3/InGaAs gate stacks,** K. Tang[1], A. C. Meng[1], R. Droopad[2], and P. C. McIntyre[1], *[1]Stanford U., [2]Texas State U.*

5:43 PM 6.5 - **Rebooting the interfacial knowledge of high-k dielectrics on $In_{0.53}Ga_{0.47}As$(001)-4x2,** Y. H. Lin[1], Y. T. Cheng[2], W. S. Chen[2], K. Y. Lin[1], H. W. Wan[1], C. P. Cheng[3], T. W. Pi[2], J. Kwo[4], and M. Hong[1], *[1]National Taiwan U., Taiwan, [2]National Synchrotron Radiation Research Center, Taiwan, [3]National Chiayi U., Taiwan, [4]National Tsing Hua U., Taiwan*

5:45 PM 6.6 - **Modification of the Al_2O_3/GaAs junction with novel crystalline un-reconstructed (1x1)-InO interface structure,** J. Mäkelä[1], M. Tuominen[1], J. Dahl[1], M. Yasir[1], J. Lång[1], M. Kuzmin[1], S. Granroth[1], M. Lastusaari[1], R. Félix[2], M. P. J. Punkkinen[1], P. Laukkanen[1], and K. Kokko[1], *[1]U. Turku, Finland, [2]U. Jyvaskyla, Finland, [3]Helmholtz-Zentrum Berlin, Germany*

5:47 PM 6.7 - **The impact of an HBr/Ar atomic layer etch (ALE) process for InGaAs vertical nanowire diameter reduction on the interface between InGaAs and in-situ ALD deposited HfO_2,** X. Li, Y.-C. Fu, D. A. J. Millar, U. Peralagu, M. Steer, and I. G. Thayne, *U. Glasgow, UK*

5:49 PM 6.8 - **Relevance of GaAs(001) surface electronic structure for high frequency dispersion on n-type accumulation capacitance,** W. S. Chen[1], Y. H. Lin[2], Y. T. Cheng[3], K. Y. Lin[2], T. W. Chang[2], H. W. Wan[2], C. P. Cheng[3], T. W. Pi[1], J. Kwo[4], and M. Hong[2], *[1]National Synchrotron Radiation Research Center, Taiwan, [2]National Taiwan U., Taiwan, [3]National Chiayi U., Taiwan, [4]National Tsing Hua U., Taiwan*

5:51 PM 6.9 - **Elemental diffusion study of InAs/Al_2O_3 interface by photoemission spectroscopy,** X-L. Wang[1], Y. Sun[1], Y. Liu[1], W. Wang[1] , H. Wang[1], Y. Zhu[1], W-W. Wang[1], W-H. Wang[1], X. Xie[2] , J-O. Wang[3], H. Liu[1], and H. Dong[1], *[1]Nankai U., China, [2]HEBUT, China, [3]IHEP, China*

5:53 PM 6.10 - **Systematic Study on Plasma Enhanced Atomic Layer Deposited Al_2O_3 on n GaN,** E. Bahat Treidel[1], F. Naumann[2], H. Gargouri[2], O. Hilt[1], B. Martinez[1], and J. Würfl[1], *[1]FBH, Germany, [2]SENTECH Instruments, Germany*

5:55 PM 6.11 - **Electrical Conductivity and Interface Configurations Across Wafer Bonded III-V Interfaces,** M. Liao, M. Yee, and M. S. Goorsky, *UCLA*

5:57 PM 6.12 - **InP thin film transfer onto GaAs using titanium bonding for high efficiency photovoltaic applications,** C. Cadieux[1], C. Taillandier[1], M. Rabarot[1], J. M. Fabbri[1], and E. Guiot[2], *[1]U. Grenoble Alpes, France, [2]SOITEC, France*

5:59 PM 6.13 - **Effect of in-situ H_2 Plasma Clean on TiN/HfO_2/Al_2O_3/$In_{0.53}Ga_{0.47}As$ gate stacks formed using plasma-enhanced atomic layer deposition,** É. O'Connor, V. Djara, V. Deshpande, M. Sousa, R. Grundbacher, D. Caimi, J. Fompeyrine, and L. Czornomaz, *IBM Research, Switzerland*

6:01 PM Adjourn

Poster Session I

Session Chairs: C. L. Hinkle and M. Passlack

7:00 PM – 10:00 PM Poster Session I

10:00 PM – Midnight Hospitality room

Friday, December 9, 2016

Session 7 – Ge Interfaces

Session Chair: A. Kummel

8:00 AM Morning announcement and opening remarks

8:05 AM 7.1 *Invited* - **Critical issues and Challenges of High k Gate Stacks for Ge/GOI MOSFETs,** S. Takagi, M. Ke, Y. Xiao, R. Zhang, and M. Takenaka, *U. Tokyo, Japan*

8:40 AM 7.2 - **Ge Oxidation is not by Deal-Grove Mechanism,** H. Li and J. Robertson, *Cambridge U., UK*

9:00 AM 7.3 - **High Performance Ge pMOSFETs with Minimized Ge^{+1} and Ge^{+2} in GeOx Interfacial Layer,** J. Huang, S. H. Yi, C. W. Hsu, T. Y. Wu, and K. S. Chang-Liao, *National Tsing Hua U., Taiwan*

9:20 AM 7.4 - **The role of surface chemistry for the nucleation of Al_2O_3 on Ge(100) in atomic layer deposition,** Y. Zheng[1], S. Hong[1], G. Psofogiannakis[1], G. B. Rayner Jr[2], S. Datta[3], A. C. T. van Duin[1], and R. Engel-Herbert[1], *[1]Penn State U., [2]Kurt J. Lesker Co., [3]U. Notre Dame*

9:40 AM 7.5 - **Yttrium passivation of defects in GeO_2 and GeO_2/Ge interfaces,** H. Li and J. Robertson, *Cambridge U., UK*

10:00 AM Coffee break

Session 8 – Ferroelectrics II

Session Chair: J. Muller

10:25 AM 8.1 *Invited* - **Negative Capacitance and Its Implications for Low Voltage Transistors,** S. Salahuddin, *UC Berkeley*

11:00 AM 8.2 - **Investigating pulse responses of HfO_2 ferroelectric film,** X. Sun, T. Ando, P. M. Solomon, A. Pyzyna, M. M. Frank, J.-P. Han, C.-C. Yeh, and V. Narayanan, *IBM Research*

11:20 AM 8.3 - **Impact of Top and Bottom Conductive Layers on Electrical and Material Properties of Ferroelectric Aluminum Doped HfO_2,** K. Florent[1,2], M. Popovici[1], S. Lavizzari[1], L. Di Piazza[1], G. Groeseneken[1,2], and J. Van Houdt[1,2], *[1]imec, Belgium, [2]U. Leuven, Belgium*

11:40 AM 8.4 - **A Study of Depolarization Field and Related Retention in HfO_2-based Ferroelectric Field Effect Transistors,** N. Gong and T. P. Ma, *Yale U.*

Session 9 - Poster Preview Session 3 – Ge and Oxides

Session Chair: P. McIntyre

12:00 PM Opening remarks

12:02 PM 9.1 - **Evaluation of heat transport properties for Al_2O_3 gate insulator on Ge substrates,** N. Uchida, W.-H. Chang, H. Hattori, and T. Maeda, *AIST, Japan*

12:04 PM 9.2 - **Epi Ge(001)-2×1 surface aimed for high-κ deposition: An electronic-structure study,** Y. T. Cheng[1], W. S. Chen[2], Y. H. Lin[3], H. W. Wan[3], K. Y. Lin[3], S. Wang[1], C. P. Cheng[1], T. W. Pi[2], J. Kwo[4], and M. Hong[3], *[1]National Chiayi U., Taiwan, [2]National Synchrotron Radiation Research Center, Taiwan, [3]National Taiwan U., Taiwan, [4]National Tsing Hua U., Taiwan*

12:06 PM 9.3 - **Selective Etching of Silicon in Preference to Germanium,** C. F. Ahles[1], J. Y. Choi[1], R. Yang[2], and A. C. Kummel[1], *[1]UCSD, [2]LAM Research*

12:08 PM 9.4 - **Terahertz non-contact 3D sub-surface imaging of SiGe interfaces and stacking faults,** A. Rahman and A. K. Rahman, *Applied Research & Photonics*

12:10 PM 9.5 - **Passivation and photo/electro luminescence of Ge/GeSn/Ge quantum wells,** C.-Y. Lin[1], F.-L. Lu[1], C. W. Liu[1,2], Y.-C. Huang[3], H. Chung[3], and C.-P. Chang[3], *[1]National Taiwan U., Taiwan, [2]National Nano Device Laboratories, Taiwan, [3]Applied Materials*

12:12 PM 9.6 - **Scaled tri-layer gate oxide for GeSn nanoelectronics,** C. Schulte-Braucks[1,3], R. Pandey[2], M. Barth[2], N. von den Driesch[1], P. Sharma[3], B. Rayner[4], S. Mantl[1], D. Buca[1], and S. Datta[2], *[1]Forschungszentrum Jülich, Germany, [2]Penn State U., [3]U. Notre Dame, [4]Kurt J. Lesker Co.*

12:14 PM 9.7 - **Wider Memory Window in Ta_2O_5 RRAM by Doping,** N. Sedghi[1], H. Li[2], I. Brunell[1], R. Potter [1], S. Hall[1], P. R. Chalker[1], Y. Guo[2], and J. Robertson[2], *[1]U. Liverpool, UK, [2]Cambridge U., UK*

12:16 PM 9.8 - **Ferroelectric HfO_2 MIS Capacitor and MISFET on Oxide Semiconductors,** L. Xu[1], S. Shibayama[1], T. Nishimura[1], T. Yajima[1], S. Migita[2], and A. Toriumi[1], *[1]U. Tokyo, Japan, [2]AIST, Japan*

12:18 PM 9.9 - **Significant Enhancement of Operation Speeds in Flash Devices with Advanced Gate Structures by Si_3N_4/HfO_2 Stack Charge-trapping Layers for 3D Memory Applications,** P. G. Wu, K. S. Chang-Liao, H. K. Fang, C. H. Cheng, and Y. C. Yu, *National Tsing Hua U., Taiwan*

12:20 PM Adjourn for lunch

12:20 PM – 2:00 PM Committee / Invited speaker luncheon

Session 10 – Interfaces of Novel Materials and Applications

Session Chairs: C. L. Hinkle

2:00 PM Opening remarks

2:05 PM 10.1 *Invited* - **2D/3D Tunnel FETs: Toward Green Transistors and Sensors,** K. Banerjee, *UCSB*

2:40 PM 10.2 - **High Performance Depletion/Enhancement-Mode β-Ga_2O_3 on Insulator (GOOI) Field-Effect Transistors with Record Drain Currents of 600/450 mA/mm,** H. Zhou, M. Si, S. Alghamdi, G. Qiu, L. Yang, and P. D. Ye, *Purdue U.*

3:00 PM 10.3 - **Molecular Beam Epitaxy grown NbO2 thin films for selector devices,** T. Hadamek[1], A. B. Posadas[1], J. Park[2], E. Cha[2], H. Hwang[2], and A. A. Demkov[1], *[1]UT Austin, [2]Pohang U. Science and Technology, Korea*

3:20 PM 10.4 - **Making High-performance Low-power Transistors out of Imperfect Materials using Two-dimensional Topological Insulators,** W. G. Vandenberghe and M. V. Fischetti, *UT Dallas*

Session 11 - Poster Preview Session 4 – Si, High-k, Wide Bandgap Interfaces

Session Chair: P. D. Ye

3:40 PM 11.1 - **New Observation of Anomalous RTN Featuring Two Metastable Trap-States in Nanoscale MOSFET with HfO_2 Gate Dielectric,** S. Guo[1], R. Wang[1], Y. Wang[1], and R. Huang[1], *Peking U., China*

3:42 PM 11.2 - **Performance of Hybrid p-channel Trench Poly-Si Junctionless Field-Effect Gate-All-Around Transistors,** V. Thirunavukkarasu[1,2], C. H. Cheng[2], Y. R. Lin[2], E. D. Kurniawan[1,2], and Y. C. Wu[2], *[1]Academia Sinica, Taiwan, [2]National Tsing Hua U., Taiwan*

3:44 PM 11.3 - **Tensile strain recovery and dopant re-activation using laser annealing,** F.-L. Lu[1],and I.-H. Wong[1], S.-H. Huang[1], and C. W. Liu[1,2], *[1]National Taiwan U., Taiwan, [2]National Nano Device Laboratories, Taiwan*

3:46 PM 11.4 - **Oxygen-bond switching at GeO_2/Si interface in UHV annealing,** W. Song and A. Toriumi, *U. Tokyo, Japan*

3:48 PM 11.5 - **Determination of Schottky barrier height prior to metal formation,** C. P. Cheng[1], W. S. Chen[1,2], K. Y. Lin[3], G. J. Wei[1], Y. T. Cheng[1], Y. H. Lin[3], H. W. Wan[3], T. W. Pi[2], R. T. Tung[4], J. Kwo[5], and M. Hong[3], *[1]National Chiayi U., Taiwan, [2]National Synchrotron Radiation Research Center, Taiwan, [3]National Taiwan U., Taiwan, [4]CUNY, [5]National Tsing Hua U., Taiwan*

3:50 PM 11.6 - **Determination of Barrier Heights between Amorphous Metals and SiO_2, Al_2O_3, and HfO_2 using Internal Photoemission Spectroscopy,** M. A. Jenkins[1], T. Klarr[1], D. Austin[1], J. McGlone[1], L. Wei[2], N. Nguyen[2], J. F. Wager[1], J. F. Conley Jr[1], *[1]Oregon State U., [2]NIST*

3:52 PM 11.7 - **Low Temperature Thermal ALD BN from N_2H_4 + BCl_3 on $Si_{0.7}Ge_{0.3}$(001),** S. Wolf[1], M. Edmonds[1], K. Sardashti[1], M. Clemons[1], E. Yieh[2], H. Ren[2], S. Nemani[2], D. Alvarez[3], and A. C. Kummel[1], *[1]UCSD, [2]Applied Materials, [3]Rasirc, Inc.*

3:54 PM 11.8 - **Reconsideration of metal work function on semiconductors from metal-induced gap states viewpoint,** T. Nishimura, S. Matsumoto, T. Yajima, and A. Toriumi, *U. Tokyo, Japan*

3:56 PM 11.9 - **Investigation of microelectronics interfaces using neutron reflectometry,** A. Ponard[1], J. Segura-Ruiz[2], G. Imbert[1], P. Gutfreund[2], and R. Cubitt[2], *[1]STMicroelectronics, France, [2]Institut Laue Langevin, France*

3:58 PM 11.10 - **Simulation-Aided Characterization of Oxide Interface Traps for FinFETs,** J.-L. Lai[1], M.-H. Chiang[1], W.-C. Hsu[1], G.-L. Luo[2], and K. Wu[2], *[1]National Cheng Kung U., Taiwan, [2]National Nano Device Laboratories, Taiwan*

4:00 PM 11.11 - **Role of Fixed Charge on Schottky Barrier Height of Metal Insulator Semiconductor Tunnel Structures,** R. J. Marstell and N. C. Strandwitz, *Lehigh U.*

4:02 PM 11.12 - **Spontaneous growth of Single Crystalline Layers Induced by the Asymmetry of Organic Metallic Molecules,** J. H. Park[1], L. Ravavar[2], I. Kwak[1], S. K. Fullerton-Shirey[3], P. Choudhury[2], A. C. Kummel[1], *[1]UCSD, [2]New Mexico Tech., [3]U. Pittsburgh*

4:04 PM 11.13 - **Comparative study of the Al_2O_3/β-(-201)Ga_2O_3 and Al_2O_3/β-(010)Ga_2O_3 interfaces through photo-assisted C-V measurements,** S. Alghamdi, H. Zhou, M. Si, and P. D. Ye, *Purdue U.*

4:06 PM 11.14 - **A New Approach to Heterointerface Characterization: Multiple Field/Frequency Spin Dependent Charge Pumping and Bipolar Amplification Effect Spin Dependent Recombination,** M. A. Anders[1], P. M. Lenahan[1], and A. J. Lelis[2], *[1]Penn State U., [2]U.S. Army Research Laboratory*

4:08 PM 11.15 - **A Distributed Model for Near-Interface Traps in 4H-SiC MOS Capacitors,** X. F. Zhang[1], D. Okamoto[1], T. Hatakeyama[2], M. Sometani[2], S. Harada[2], R. Kosugi[2], N. Iwamuro[1], and H. Yano[1], *[1]U. Tsukuba, Japan, [2]AIST, Japan*

4:10 PM 11.16 - **Influence of Interface ALD-SiO_2 Layer for Lanthanum Silicate Gate Dielectrics for 4H-SiC MOS Capacitors,** Y. M. Lei[1], T. Kaneko[1], H. Wakabayashi[1], K. Tsutsui[1], H. Iwai[1], K. Kakushima[1], M. Furuhashi[2], S. Tomohisa[2], and S. Yamakawa[2], *[1]Tokyo Institute of Technology, Japan, [2]Mitsubishi Electric, Japan*

4:12 PM 11.17 - **Characterization of Traps at Nitrided SiO_2/ SiC Interfaces near the Conduction Band Edge by using Hall Effect Measurements,** T. Hatakeyama[1], Y. Kiuchi[1], M. Sometani[1], D. Okamoto[2], S. Harada[1], H. Yano[2], Y. Yonezawa[1], and H. Okumura[1], *[1]AIST, Japan, [2]U. Tsukuba, Japan*

4:14 PM 11.18 - **Al_2O_3 Dielectric Layers on Hydrogen-Terminated Diamond: Controlling Surface Conductivity,** Y. Yang, F. A. Koeck, M. Dutta, H. Surdi, S. Chowdhury, and R. J. Nemanich, *Arizona State U.*

4:16 PM 11.19 - **Are dangling bonds important defects at the SiC/SiO_2 interface?,** M. A. Anders[1], P. M. Lenahan[1], and A. J. Lelis[2], *[1]Penn State U., [2]U.S. Army Research Laboratory*

4:18 PM 11.20 - **Atomistic modeling of surfaces and interfaces beyond the slab approach,** A. Blom, P. A. Khomyakov, T. Markussen, and D. Stradi, *QuantumWise, Denmark*

4:20 PM 11.21 - **Systematic Thermal Dynamic Modeling Applied in Gate Stacks,** H. L. Chang, C. T. Chang, and C. T. Kuo, *Samsung Electronics, Korea*

4:22 PM 11.22 - **An Improved model for Tunneling Probability in HKMG MOS transistors with correction in WKB Approximation,** A. Ojha and N. R. Mohapatra, *IIT Gandhinagar, India*

4:24 PM 11.23 - **Radiation induced charge trapping in epitaxial La_2O_3 gate dielectric grown on GaAs,** M. Bhuiyan[1], X. Lou[2], X. Gong[2], H. Zhou[3], K. Ni[4], R. Jiang[4], H. Gong[4], E. X. Zhang[4], R. G. Gordon[2], R. A. Reed[4], D. M. Fleetwood[4], P. D. Ye[3], and T. P. Ma[1], *[1]Yale U., [2]Harvard U., [3]Purdue U., [4]Vanderbilt U.*

4:26 PM 11.24 - **Impacts of Ti incorporation on the electrical properties and reliability of GaAs metal-oxide-semiconductor capacitors with high-k NdTiON as gate dielectric,** L. N. Liu[1], H. W. Choi[1], J. P. Xu[2], and P. T. Lai[1], *[1]U. Hong Kong, Hong Kong, [2]Huazhong U. Science and Technology, China*

Poster Session II

Session Chairs: C. L. Hinkle and M. Passlack

4:45 PM – 6:45 PM Poster Session II

7:00 PM – 10:00 PM Conference banquet and Limerick contest

10:00 PM – Midnight Hospitality room

Saturday, December 10, 2016

Session 12 – 2D Materials II

Session Chair: W. G. Vandenberghe

8:00 AM 12.1 - **Contacts on WSe_2: Interface Chemistry and Band Alignment,** C. M. Smyth[1], R. Addou[1], S. McDonnell[2], J. Kim[1], C. L. Hinkle[1], and R. M. Wallace[1], *[1]UT Dallas, [2]U. Virginia*

8:20 AM 12.2 - **Tuning transport at the graphene/TMD interface,** D. D. Deng[1], S. Subramanian[1], K. Zhang[1], G. R. Bhimanapati[1], T. S. Mayer[2], and J. A. Robinson[1], *[1]Penn State U., [2]Virginia Tech*

8:40 AM 12.3 - **High Performance Functionalisation-free HfO_2 Top Gate for MoS_2 FETs with 6 nm EOT and SSmin~60 mV/decade,** S. Bhattacharjee, K. L. Ganapathi, S. Mohan, and N. Bhat, *IIS Bangalore, India*

9:00 AM 12.4 - **High field transport of high performance black phosphorus transistors,** X. Li, T. Li, and Y. Wu, *Huazhong U. Science and Technology, China*

9:20 AM Coffee Break

Session 13 – III-V Interfaces

Session Chair: J. Robertson

9:50 AM 13.1 *Invited* - **III-V Nanowire MosFETs and Tunnel FETs,** L.-E. Wernersson, *Lund U., Sweden*

10:25 AM 13.2 - **Effect of DEZn Surface Treatment on Sulfur-Passivated InGaAs with Atomic Layer Deposited High-k Film,** J.-G. Lee[1], Y.-C. Byun[1], Y. J. Oh[1], D. Narayan[1], A. T. Lucero[1], K. Cho[1], C. D. Young[1], H. Kim[2], and J. Kim[1], *[1]UT Dallas, [2]Sungkyunkwan U., Korea*

10:45 AM 13.3 - **Understanding Device Quality High-k/InAs/GaSb Gate Stack,** T. Vasen[1], S. W. Wang[1], R. Contreras-Guerrero[2], J. Rojas-Ramirez[2], G. Doornbos[1], T. K. Chen[3], G. Hsieh[3], P. Ramvall[1], G. Vellianitis[1], R. Oxland[1], M. C. Holland[1], R. Droopad[2], Y-.C. Yeo[3], and M. Passlack[1], *[1]TSMC, Belgium, [2]Texas State U., [3]TSMC, Taiwan*

11:05 AM 13.4 - **ALD Oxides In-situ on InGaAs - Perfecting Interfacial Electronic Structures in Pushing High-Performance Inversion-Channel MOSFETs,** H. W. Wan[1], K. Y. Lin[1], M. H. Chen[1], L. B. Young[1], Y. H. Lin[1], Y. C. Chang[1], T. D. Lin[1], Y. T. Cheng[2], W. S. Chen[2], S. H. Chen[3], T. W. Pi[2], J. Kwo[4], and M. Hong[1,3], *[1]National Taiwan U., Taiwan, [2]National Synchrotron Radiation Research Center, Taiwan, [3]National Nano Device Laboratories, Taiwan, [4]National Tsing Hua U., Taiwan*

Session 14 – GaN and SiC

Session Chair: R. Nemanich

11:25 AM 14.1 - **Gate Voltage Dependence of 1/f noise of GaN/AlGaN HEMTs,** P. Wang, R. Jiang, E. X. Zhang, H. Gong, S. Zhao, R. D. Schrimpf, and D. M. Fleetwood, *Vanderbilt U.*

11:45 AM 14.2 - **First-Principles Study of GaN Surface Electronic Structures with Ga, O or N Adatom,** Z. Zhang, B. Li, X. Tang, Q. Qian, M. Hua, B. Huang, and K. J. Chen, *Hong Kong U. Science and Technology, Hong Kong*

12:05 PM 14.3 - **Properties of SiC Schottky Junction with Laminated Molybdenum/Carbon Electrode,** T. Suzuki[1], H. Wakabayashi[1], K. Tsutsui[1], H. Iwai[1], H. Nohira[2], and K. Kakushima[1], *[1]Tokyo Institute of Technology, Japan, [2]Tokyo City U., Japan*

12:25 PM Closing remarks and adjourn