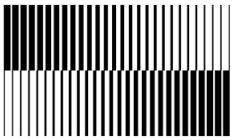

SISC 2023

54th IEEE Semiconductor Interface Specialists Conference

December 13–16, 2023
Bahia Resort Hotel, San Diego, CA
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SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E. H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology", published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author for either an oral or a poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

2022 SISC Ed Nicollian Award for Best Student Paper

Jiaqi Chen

University of Cambridge, UK

"Ambipolar Contacts at WSe_2/Metal via Moire Interface Transistors"

with Z. Zhang, Y. Guo, and J. Robertson

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SISC T. P. Ma Award for Best Student Poster

In 2021, the SISC added an award for the best student poster in honor of Professor T. P. Ma, Yale University. Professor Ma was an internationally recognized pioneer for his contributions to semiconductor science and technology — in particular, breakthroughs in advanced gate dielectrics, which paved the path for high-κ dielectrics and extended the scaling of CMOS technology. His research also generated fundamental and lasting impacts on many other applied physics fields, notably ferroelectrics and ionizing radiation sciences.

The *SISC T. P. Ma Award* will be presented to the lead student author for a poster presentation. The winner will be chosen by members of the technical program committee at the end of the SISC. The award will consist of a plaque, an honorarium, and a permanent mention on the conference web site.

2022 SISC T. P. Ma Award for Best Student Poster

Joy Roy

University of Texas at Dallas

"Bi Contact Interface and Band Alignment Study on W-based Transition Metal Dichalcogenides"

with S. Y. Kim, X. Wang, and R. M. Wallace

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Wednesday Evening Tutorial

Wednesday, December 13, 2023, 8:00 PM

First introduced at SISC 2008, the Wednesday Evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

Dr. Dale McHerron, *IBM*

From Interconnects to Chiplets: Materials and Interfaces for Advanced Packaging

Recent technology trends in areas such as CMOS scaling, artificial intelligence, computational workloads, including data centers and at the edge, are driving a resurgence in packaging technology innovations, particularly with Heterogeneous Integration and chiplet architectures. This tutorial will analyze these developments with particular focus on the materials, processes, and interfaces that are at the center of these new innovations. I will provide an overview of packaging technology fundamentals to put these technologies in context as well as highlight some of the challenges and opportunities that are emerging.

The tutorial will also explore these technology trends and why advanced packaging technologies are so critical to address the challenges and opportunities presenting themselves and ultimately provide improvements in performance and cost required for next generation computational systems and associated hardware architectures. I will put some focus on trends and advancements in artificial intelligence, as this technology is creating unique opportunities for advanced packaging and chiplet architectures to enable significant performance gains and energy efficiency improvements over the next decade.

Dale McHerron, PhD

Senior Manager and STSM, IBM Research

Dale is currently Senior Manager and Senior Technical Staff Member at IBM Research based in Albany, NY with responsibility for IBM's Heterogeneous Integration Research Program and principal investigator in the IBM AI Hardware Research Center. Over his 30+ year career at IBM, Dale has held various technical, managerial, and business development positions in both advanced packaging and CMOS logic R&D. In 2007, he transitioned to the IBM Albany Research lab where he has initiated and led research projects in logic scaling, heterogeneous integration, and has played a key role developing the IBM collaborative research ecosystem in Albany. Dale received his PhD in Chemical Engineering from Virginia Tech with a focus on polymeric materials. Dale has co-authored numerous research papers and holds multiple patents in the field of microelectronics.

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Conference Agenda Overview

Wednesday, December 13, 2023

Registration (Shell Foyer)	6:00 PM	–	8:00 PM
Evening Tutorial (Shell Room)	8:00 PM	–	9:30 PM
Hospitality (The Cabrillo Suite)	10:00 PM	–	12:00 AM

Thursday, December 14, 2023

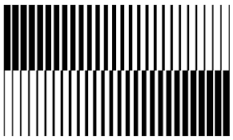
Registration (Mission Foyer)	8:00 AM	–	5:00 PM
Breakfast (Mission Foyer)	7:30 AM	–	8:30 AM
Session 1: Advanced Logic & Oxide FETs I (Mission Room AB)	8:30 AM	–	10:25 AM
Session 2: Reliability (Mission Room AB)	10:40 AM	–	12:10 PM
Session 3: Ferroelectrics I (Mission Room AB)	1:30 PM	–	2:55 PM
Session 4: Poster Preview I (Mission Room AB)	2:55 PM	–	3:25 PM
Session 5: Contacts & Metallization (Mission Room AB)	3:40 PM	–	5:10 PM
Session 6: Poster Preview II (Mission Room AB)	5:10 PM	–	5:40 PM
Reception & Poster Session (Bay Room CDE)	7:00 PM	–	10:00 PM
Hospitality (The Cabrillo Suite)	10:00 PM	–	12:00 AM

Friday, December 15, 2023

Registration (Mission Foyer)	8:00 AM	–	12:00 PM
Breakfast (Mission Foyer)	7:30 AM	–	8:30 AM
Session 7: NVM/Neuro I (Mission Room AB)	8:30 AM	–	10:00 AM
Session 8: Advanced Logic & Oxide FETs II (Mission Room AB)	10:15 AM	–	12:05 PM
Committee / Invited Speaker Luncheon (by invitation only, Shell Room)	12:10 PM	–	1:30 PM
Session 9: Advanced Logic & Oxide FETs III (Mission Room AB)	1:30 PM	–	3:00 PM
Session 10: 2D/TMD (Mission Room AB)	3:15 PM	–	4:35 PM
Session 11: NVM/Neuro II (Mission Room AB)	4:50 PM	–	6:00 PM
Conference Banquet & Limerick Contest (William D. Evans boat)	7:00 PM	–	10:00 PM
Hospitality (The Cabrillo Suite)	10:00 PM	–	12:00 AM

Saturday, December 16, 2023

Breakfast (Mission Foyer)	7:30 AM	–	8:30 AM
Session 12: Wide Band Gap Semiconductors (Mission Room AB)	8:30 AM	–	10:20 AM
Session 13: Ferroelectrics II (Mission Room AB)	10:35 AM	–	11:55 AM



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Wednesday, December 13, 2023

Tutorial

Session Chair: J. Rozen

8:00 PM – 9:30 PM *Tutorial* – **From Interconnects to Chiplets: Materials and Interfaces for Advanced Packaging,** D. McHerron, *IBM*

Thursday, December 14, 2023

Session 1: Advanced Logic & Oxide FETs I

Session Chair: P. D. Ye

8:30 AM Introduction

8:35 AM 1.1 *Invited* – **Enabling Gate-Pitch Scaling in the Angstrom Era,** A. Penumatcha, *Intel*

9:05 AM 1.2 – **High-k (47) $Hf_{0.2}Zr_{0.8}O_2$ Gate Stacks Integrated into 8 Stacked $Ge_{0.95}Si_{0.05}$ Nanowire and Nanosheet nFETs to Significantly Enhance I_{ON},** Y.-C. Liu, Y.-R. Chen, Y.-W. Chen, W.-J. Chen, C.-T. Tu, and C. W. Liu, *National Taiwan U., Taiwan*

9:25 AM 1.3 – **High-Performance Ge FinFET CMOS Devices by High-Pressure Supercritical Fluid Hydroxide Oxidation,** J. Y. Hsiung[1], D. B. Ruan[2], K. S. Chang-Liao[1], Y. J. Lee[3], Y. C. Chiu[4], C. W. Liu[1], G. T. Liu[1], B. L. Kuo[1], K. C. Yang[1], C. H. Li[1], and P. T. Liu[4], [1]*National Tsing Hua U., Taiwan,* [2]*Fuzhou U., China,* [3]*Taiwan Semiconductor Research Institute, Taiwan,* [4]*National Yang Ming Chiao Tung U., Taiwan*

9:45 AM 1.4 – **Density Functional Analysis of Flat-band Voltage Shifts at High K/Metal Gate Stacks,** R. Cao[1], Z. Zhang[2], Y. Guo[2], and J. Robertson[1,2], [1]*U. Cambridge, UK,* [2]*Wuhan U., China*

10:05 AM 1.5 – **IGZO Thickness Effect on Performance and Initial Instability in IGZO Thin Film Transistors,** R. A. Rodriguez-Davila[1], E. McNeil[1,2], M. Quevedo-Lopez[1], and C. D. Young[1], [1]*UT Dallas,* [2]*NSF*

10:25 AM–10:40 AM Coffee Break

Session 2: Reliability

Session Chair: D. Chen

10:40 AM — 2.1 *Invited* – **Radiation Effects and Reliability in 3D Integrated Circuits,** E. X. Zhang[1], S. Toguchi[2], R. D. Schrimpf[3], M. L. Alles[3], and D. M. Fleetwood[3], [1]*U. of Central Florida,* [2]*Microchip Technology Inc.,* [3]*Vanderbilt U.*

11:10 AM — 2.2 – **The impact of channel composition on the PBTI stability of oxide semiconductor transistors,** Z. Lin, Z. Wang, and M. Si, *Shanghai Jiao Tong U., China*

11:30 AM — 2.3 – **Improvement of PBS properties for c- and m-GaN/Al_2O_3/Pt capacitors using a dummy SiO_2 layer,** T. Nabatame, T. Sawada, Y. Irokawa, M. Miyamoto, H. Miura, Y. Koide, and K. Tsukagoshi, *National Institute for Materials Science, Japan*

11:50 AM — 2.4 – **Impact of Channel Thickness Scalability on Reliability Instability in AlGaN/GaN HEMTs,** W. Amir[1], S. Chakraborty[1], J.-W. Shin[1], K.-Y. Shin[1], J.-G. Kim[1], C.-Y. Cho[2], J.-M. Kim[2], J.-P. Shim[2], T. Hoshi[3], T. Tsutsumi[3], H. Matsuzaki[3], H.-M. Kwon[4], C.-S. Shin[2], K.-S. Seo[2], D.-H. Kim[5], and T.-W. Kim[1,6], [1]*U. of Ulsan, Korea,* [2]*KANC, Korea,* [3]*NTT Device Technology Laboratories, Japan,* [4]*Korea Polytechnics, Korea,* [5]*Kyungpook National U., Korea,* [6]*Texas Tech U.*

12:10 PM — Adjourn for lunch

Session 3: Ferroelectrics I

Session Chair: C. L. Hinkle

1:30 PM — 3.1 – **Why do ferroelectrics offer the lowest-power nonvolatile memory mechanism?,** J. Van Houdt[1,2], S. Clima[1], J. Bizindavyi[1], and P. Roussel[1], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

1:50 PM — 3.2 – **Cryogenic Investigation of Polarization Switching Ultra-Thin Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Capacitors,** B. Saini[1], C. Yoo[1,2], F. Huang[1], J. D. Baniecki[2], W. Tsai[1], and P. C. McIntyre[1,2], [1]*Stanford U.,* [2]*SLAC National Accelerator Laboratory*

2:10 PM — 3.3 – **Memory Window Boosting along with Endurance Improvement in MFMIS Ferroelectric FETs by Engineering Charge Injection in Antiferroelectric and Dielectric Layers,** D. Chen, T. Cui, Z. Yao, Z. Lin, J. Liu, M. Si, and X. Li, *Shanghai Jiao Tong U., China*

2:30 PM — 3.4 – **$Hf_{0.5}Zr_{0.5}O_2$-based Ferroelectric Field-Effect-Transistor with SnO_x Channel,** Z. Zheng, L. Jiao, C. Sun, X. Wang, Z. Zhou, and X. Gong, *National U. of Singapore, Singapore*

2:50 PM – 2:55 PM — Limerick Contest Introduction

Session 4: Poster Preview I

Session Chair: R. Timm

2:55 PM — 4.1 – **Conjugate Suppression of SiC Interface Double Defects,** L. Zheng, L.-Y. Shen, J. H. Feng, X. T. Zhou, and X.-H. Cheng, *Shanghai Institute of Microsystem and Information Technology, China*

2:56 PM 4.2 – **T-ray Wafer-scale Profile Mapping for Fab Yield Improvement and Domain Imaging of SiC Wafers,** A. Rahman, *Applied Research & Photonics*

2:57 PM 4.3 – **Interface Modification of Silicon/Colloidal Quantum Dot Heterojunction for Highly Responsive Wide Spectrum Detection,** Z.-Y. Liu[1,2], L. Zheng[1], L.-Y. Shen[1], X.-H. Cheng[1], and Y.-H. Yu[1], [1]*Shanghai Institute of Microsystem and Information Technology, China,* [2]*ShanghaiTech U., China.*

2:58 PM 4.4 – **Contactless Control of Interface Electric Field using Electron Beam Induced Charging,** Y. Shirasaki and M. Shoji, *Hitachi, Japan*

2:59 PM 4.5 – **Resistive Memory Based on operando created V-Ti-O Alloy in V_2O_3 thin films,** K. Veyret[1], L. Laborie[1], G. Lefevre[1], G. Navarro[1], R. Hida[1], X. Zucchi[1], C. Carabasse[1], G. Bourgeois[1], N. Castellani[1], P. Gonon[2], and E. Jalaguier[1], [1]*CEA-Leti, France,* [2]*U. Grenoble Alpes, France*

3:00 PM 4.6 – **Surface properties of p-GaN and interaction with nickel,** M. Miettinen[1], V. Nuutila[1], Z. Jahanshah Rad[1], M. Ebrahimzadeh[1], R. Punkkinen[1], J.-P. Lehtiö[1], S. Suihkonen[2], P. Laukkanen[1], H. Savin[2], and K. Kokko[1], [1]*U. of Turku, Finland,* [2]*Aalto U., Finland*

3:01 PM 4.7 – **Temperature Effect and Switching Gap Simulation on Oxide-Stacked Reprogrammable One-Time Programmable Memory,** J. Stouffer[1] and Y. C. Chen[2], [1]*Northern Arizona U.,* [2]*Arizona State U.*

3:02 PM 4.8 – **Al_2O_3 Deposition on SiO_2 in Preference to W by Water-free Chemical Vapor Depositions with Aniline Passivation,** J. Huang[1], J. Mu[1], Y. Cho[2], A. K. Yadav[2], K. Wong[2], S. Nemani[2], E. Yieh[2], and A. C. Kummel[1], [1]*UCSD,* [2]*Applied Materials*

3:03 PM 4.9 – **Towards wake-up free $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric capacitors thanks to Nanosecond Laser Annealing,** S. Martin, M. Opprecht, J. Coignus, C. Carabasse, C. Jahan, M. Louro, J. Laguerre, N. Castellani, V. Meli, J. Rottner, J. Barbot, J. Mercier, M. Bedjaoui, C. Boixaderas, S. Minoret, S. Kerdilès, and L. Grenouillet, *CEA-Leti, France*

3:04 PM 4.10 – **Machine-Learned Inter-atomic Potential for the Phase Change Material $Ge_3Sb_6Te_5$,** W. Yu[1], Z. Zhang[1], X. Wan[1], J. Su[1], Q. Gui[1], J. Robertson[1,2], and Y. Guo[2], [1]*Wuhan U., China,* [2]*U. Cambridge, UK*

3:05 PM 4.11 – **Improved Symmetrical Analog Switching of CuO_x/HfO_x Synaptic Transistors Using Al_2O_3 Buffer Layer and Two-Step Programming Scheme for Neuromorphic Systems,** S. Jeon, N. Kim, E. Hong, H. W. Kim, and J. Woo, *Kyungpook National U., Korea*

3:06 PM 4.12 – **Artificial Neuron Based on SiO_x Threshold Switch for Oscillatory Neural Networks,** E. Hong, H. W. Kim, S. Jeon, N. Kim, and J. Woo, *Kyungpook National U., Korea*

3:07 PM 4.13 – **Dipole first integration using Yttrium Oxide for Multi-Vt Logic Applications,** S. Homkar[1], V. Vandalon[1], V. K. Mootheri[1], R. Rastogi[2], F. Tang[2], M. Balseanu[2], E. Shero[2], G. A. Verni[1], and M. Givens[1], [1]*ASM Belgium, Belgium,* [2]*ASM America*

3:08 PM 4.14 – **Interplay of n-/p-type regions and ferroelectric switching in ferroelectric FETs,** S. Yang[1,2], L. Vieler[1], A. Sunil[1], Y. Raffel[1], F. Schöne[1], M. Everding[1], S. De[1], K. Seidel[1], M. Lederer[1], and G. Gerlach[2], [1]*Fraunhofer IPMS, Germany,* [2]*Technische Universität Dresden, Germany*

3:09 PM 4.15 – **0.6 mOhm cm^2 Ultra-low Ohmic Contact Resistance on Lightly-doped Silicon Carbide Substrate,** J. Yang[1] and Y. C. Liang[1,2], [1]*National U. of Singapore, Singapore,* [2]*NUSRI Suzhou, China*

3:10 PM 4.16 – **Vertically Stacked Cladded Si/Ge Quantum Dot GAA-FETs for Multi-bit Computing Potentially Integrating Logic, SRAMs, and NVRAMs,** F. Jain[1], R. H. Gudlavalleti[1], J. Chandy[1], and E. K. Heller[2], [1]*U. Connecticut,* [2]*Synopsys*

3:11 PM 4.17 – **Endurance Improvement of Silicon-based FeFET Employing Novel Surface Treatment Methods:Remote Plasma Nitridation and Forming Gas Annealing,** L. Jiao, X. Wang, Z. Zhou, Y. Kang, Z. Zheng, and X. Gong, *National U. of Singapore, Singapore*

3:12 PM 4.18 – **New Tunnel magnetoresistance (TMR) Magnetic Sensor Measurement System,** T. C. Yang and H. Fan, *U. of Electronic Science and Technology of China, China*

3:13 PM 4.19 – **Schottky Barrier of Moire Interfaces on HfS_2 2D Semiconductors,** R. Cao[1], Y. Guo[2], Z. Zhang[2], and J. Robertson[1], [1]*U. Cambridge, UK,* [2]*Wuhan U., China*

3:20 PM – 3:40 PM Coffee Break

Session 5: Contacts & Metallization

Session Chair: J. Robertson

3:40 PM 5.1 *Invited* – **Interconnects: New Materials for High Conductivity,** D. Gall, *Rensselaer Polytechnic Institute*

4:10 PM 5.2 – **Ohmic Contact Improvement on AlGaN/GaN Heterostructure using Graphene Layer,** Y. Chen, C. Chung, Y. Hsin, C. Huang, and C. Su, *National Central U., Taiwan*

4:30 PM 5.3 – **Computational Study of Contact Resistance as Function of Contact Length in Top-Contacted Two-Dimensional Materials,** E. Deylgat[1,2,3], S. R. Evans[1], B. Sorée[2,3,4], and W. G. Vandenberghe[1], [1]*UT Dallas,* [2]*U. Leuven, Belgium,* [3]*imec, Belgium,* [4]*U. Antwerp, Belgium*

4:50 PM 5.4 – **$PtCoO_2$ and CoSi: Directional and Topological Conductors for Scaled Interconnects,** Y. Li, G. Zhou, and C. L. Hinkle, *U. Notre Dame*

Session 6: Poster Preview II

Session Chair: A. C. Kummel

5:10 PM 6.1 – **Impact of Thermal Anneal on the Surface Properties of Synthetic Monolayer WS_2,** Z. Lin[1,2], S. Dekelver[1,2], D. Cott[1], B. Groven[1], P. Morin[1], D. Lin[1], and A. Delabie[1,2], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

5:11 PM 6.2 – **Control Crystallinity and Polarity of GaN on Oxide-free Si (111) Using ALD Process Parameters,** S. Yun[1], P. C. Lee[1], A. J. McLeod[1], H. Kashyap[1], J. Spiegelman[2], and A. C. Kummel[1], [1]*UCSD,* [2]*RASIRC*

5:12 PM 6.3 – **Reverse Templating Effects of Low-Resistivity Ru ALD on Sputtered Ru,** C. H. Kuo[1], V. Wang[1], R. Kanjolia[2], M. Moinpour[2], J. Woodruff[2], H. Simka[3], and A. C. Kummel[1], [1]*UCSD,* [2]*EMD Electronics,* [3]*Samsung*

5:13 PM 6.4 – **Reduction of voltage for low power ferroelectric devices, through graphene-based interfacial engineering,** S. Natani, Z. Zhang, W. Shipley, A. Tao, and P. Bandaru, *UCSD*

5:14 PM 6.5 – **Ferroelectric Device Optimization via Time-Resolved Synchrotron X-ray Scattering of Flash Annealed HZO Thin Films,** C. E. Ruano Arens[1], V. Tjong[2], D. Van Campen[2] P.C. McIntyre[1,2], and J. D. Baniecki[2], [1]*Stanford U.,* [2]*SLAC National Accelerator Laboratory*

5:15 PM 6.6 – **Si Doped ZrO_2 For Hysteresis Free High-k Dielectric,** H. Kashyap[1], P. C. Lee[1], K. Chae[2], A. K. Yadav[3], J. Spiegelman[4], A. I. Khan[5], and A. C. Kummel[1], [1]*UCSD,* [2]*UT Dallas,* [3]*Applied Materials,* [4]*RASIRC,* [5]*Georgia Tech*

5:16 PM 6.7 – **Oxygen vacancy rich TiO_2 for corrosion inhibition of electrical components and devices, via deposition of oxygen vacancy-rich TiO_{2-x} using atomic layer deposition (ALD),** K. Wang[1], S. Yun[1], A. Paxson[2], T. Valdez[2], A. C. Kummel[1], and P. Bandaru[1], [1]*UCSD,* [2]*Plug Power*

5:17 PM 6.8 – **Power and Thermal Stress Characterization of AlGaN/GaN HEMTs: A Comprehensive Study at Varying Elevated Temperatures,** S. Chakraborty[1], W. Amir[1], T. Hoshi[2], T. Tsutsumi[2], H. Sugiyama[2], H.-M. Kwon[3], C.-S. Shin[4], D.-H. Kim[5], and T.-W. Kim[1,6], [1]*U. of Ulsan, Korea,* [2]*NTT Device Technology Laboratories, Japan,* [3]*Korea Polytechnics, Korea,* [4]*KANC, Korea,* [5]*Kyungpook National U., Korea,* [6]*Texas Tech U.*

5:18 PM 6.9 – **Effects of Interlayer Formation by Oxidants and Substrates On Properties of ALD ZrO_2 Thin Film,** H. Shin, S. Park, S. Na, S. Chung, and H. Kim, *Yonsei U., Korea*

5:19 PM 6.10 – **Feasibility of accelerating the wake-up in HZO-based ferroelectric capacitors by optimizing cycling temperature and applied electric,** J. Bizindavyi[1], M. I. Popovici[1], S. Mukherjee[1,2], A. Belmonte[1], G. S. Kar[1], and J. Van Houdt[1,2], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

5:20 PM 6.11 – **Integration of ZnO Nanospheres using Apple Pectin as a Bio-Template for ppb-level NO_2 Detection,** J. C. Jian[1], Y. C. Chang[1], S. P. Chang[2], and S. J. Chang[1], [1]*National Cheng Kung U., Taiwan,* [2]*National Kaohsiung U. of Science and Technology, Taiwan*

5:21 PM 6.12 – **The molecular dynamics pictures of the role of surface bombardment on AlN crystallization,** Y. Jo[1], A. C. Kummel[2], and K. Cho[1], [1]*UT Dallas,* [2]*UCSD*

5:22 PM 6.13 – **First principles study of Schottky barriers at BAs/metal interfaces,** Z. Fu[1], Z. Zhang[1], J. Robertson[1,2], and Y. Guo[1], [1]*Wuhan U., China,* [2]*U. of Cambridge, UK*

5:23 PM 6.14 – **Remote O_2 Plasma Pretreatment Enhanced ALD HfO_2 Formation on MoS_2 FETs,** K.-S. Li[1], M.-K. Huang[2], Y.-H. Wang[2], Y.-C. Tseng[1], and C.-J. Su[1,3], [1]*National Yang Ming Chiao Tung U., Taiwan,* [2]*National Cheng Kung U., Taiwan,* [3]*Taiwan Semiconductor Research Institute, Taiwan*

5:24 PM 6.15 – **Growth of AlSb/Sb Structures for Phase Change Memories via Molecular Beam Epitaxy,** H. Gong[1], V. Tokranov[1], M. Yakimov[1], K. Brew[2], G. Cohen[2], and S. Oktyabrsky[1], [1]*U. at Albany-SUNY,* [2]*IBM*

5:25 PM 6.16 – **Effects of Scaling and Interface Roughness on Nanosheet Field-Effect Transistors: A 3-D Monte Carlo Simulation Study,** M. G. K. Alabdullah[1,2], D. Nagy[1], A. J. García-Loureiro[3], and K. Kalna[1], [1]*Swansea U., UK,* [2]*Northern Technical U., Iraq,* [3]*U. of Santiago de Compostela, Spain*

5:26 PM 6.17 – **Vapor-deposited ZIF-8 films as ultra-low-k dielectrics seamless high aspect ratio gap fill via capillary condensation,** D. Pal[1], J. Watson[1], H. Simka[2], and A. C. Kummel[1], [1]*UCSD,* [2]*Samsung*

5:27 PM 6.18 – **Image-Force Barrier Lowering of Schottky Barriers in Two-Dimensional Materials as a Function of Metal Contact Angle,** S. R. Evans[1], E. Deylgat[1,2,3], and W. G. Vandenberghe[1], [1]*UT Dallas,* [2]*U. Leuven, Belgium,* [3]*imec, Belgium*

5:28 PM 6.19 – **Conformal, ultrathin top gate oxide for monolayer MoS_2,** S. Natani[1], M. Passlack[2], I. Radu[3], A. C. Kummel[1], and P. Bandaru[1], [1]*UCSD,* [2]*TSMC ,* [3]*TSMC, Taiwan*

5:29 PM 6.20 – **Atomic Layer Deposition of Titanium Nitride in Horizontal Vias Using Hydrazine as Nitrogen Precursor,** J. Fammels[1,2], P. C. Lee[1], D. Pal[1], J. Pilz[2], D. Solonenko[2], J. Spiegelman[3], and A. C. Kummel[1], [1]*UCSD,* [2]*Silicon Austria Labs, Austria,* [3]*RASIRC*

5:30 PM 6.21 – **High Endurance 1T1R Synaptic Device with Excellent Linearity and Dynamic Range through Isotropic and Anisotropic Plasma Treatment,** P. A. Dananjaya[1], E. K. Koh[1,2], Y. S. You[2], and W. S. Lew[1], [1]*Nanyang Technological U., Singapore,* [2]*GlobalFoundries Singapore, Singapore*

5:31 PM 6.22 – **Characterizing Contact and Gate Interfaces with Varying Fabrication Ambient in β-Ga_2O_3 Based MOSCAPs,** A. A. Gruszecki[1], J. Roy[1], K. Cherkaoui[2], P. K. Hurley[2], R. M. Wallace[1], and C. D. Young[1], [1]*UT Dallas,* [2]*Tyndall National Institute, Ireland*

5:35 PM End

7:00 PM – 10:00 PM Reception/Poster Session

Friday, December 15, 2023

Session 7: NVM/Neuro I

Session Chair: J. Rozen

8:30 AM 7.1 *Invited* – **Protonic Electrochemical Synapses for Analog Deep Learning and Beyond,** B. Yildiz, *MIT*

9:00 AM 7.2 – **Design and Simulation of an Associative Memory Circuit with a Nanoscale Ionic Li_xTiO_2-based Synaptic Transistor,** N.-A. Nguyen[1], S. Oukassi[1], Y. Lamy[1], R. Salot[1], M. Rozenberg[2], K. Wang[2], P. Senzier[2], C. Pasquier[2], J. Giapintzakis[3], V.-H. Mai[4], and O. Schneegans[5], [1]*CEA-Leti, France,* [2]*Paris-Saclay U., France,* [3]*U. of Cyprus, Cyprus,* [4]*Le Quy Don Technical U., Vietnam,* [5]*CentraleSupélec, France*

9:20 AM 7.3 – **Large Memory Window of 2.7 V and High Endurance >10^{11} Cycles in Self-Aligned Top-Gated a-InGaZnO Ferroelectric FET by Incorporating ZnO-Rich,** Y.-M. Liu, E. Sarkar, Y.-R. Chen, J.-C. Chiu, Z. Zhao, Y.-C. Chen, Y.-C. Fan, R.-W. Ma, and C. W. Liu, *National Taiwan U., Taiwan*

9:40 AM 7.4 – **Role of Post-Annealing in Sputtered IGZO Transistor for 3D stackable Memory Applications,** N. Kim, H. W. Kim, E. Hong, S. Jeon, and J. Woo, *Kyungpook National U., Korea*

10:00 AM–10:15 AM Coffee Break

Session 8: Advanced Logic & Oxide FETs II

Session Chair: J. Franco

10:15 AM — 8.1 *Invited* – **Entering a New Era of Nanosheet FET-based Device Architectures with Increased FEOL-BEOL Synergies,** A. Veloso, G. Eneman, P. Matagne, B. Vermeersch, H. Arimura, B. O'Sullivan, C. Porret, and N. Horiguchi, *imec, Belgium*

10:45 AM — 8.2 – **Enhanced Electrical Characteristics of SiGe/Si Gate-All-Around Field-Effect-Transistor with Ge Condensation Using Supercritical Fluid Treatment,** P. H. Wei[1], D. B. Ruan[2], K. S. Chang-Liao[1], H. Y. Wang[1], G. L. Luo[3], Y. C. Chiu[4], T. K. Kuan[1], and P. T. Liu[4], [1]*National Tsing Hua U., Taiwan,* [2]*Fuzhou U., China,* [3]*Taiwan Semiconductor Research Institute, Taiwan,* [4]*National Yang Ming Chiao Tung U., Taiwan*

11:05 AM — 8.3 – **Atomic-Layer-Deposited ZnO FET and 2T0C DRAM at Cryogenic Temperatures,** Z. Wang, Z. Lin, L. Zheng, J. Zhao, and M. Si, *Shanghai Jiao Tong U., China*

11:25 AM — 8.4 – **Demonstration of a-InGaZnO Gate-all-around Nanosheet FETs,** J.-C. Chiu, E. Sarkar, Y.-M. Liu, Y.-C. Chen, Y.-C. Fan, R.-W. Ma, and C. W. Liu, *National Taiwan U., Taiwan*

11:45 AM — 8.5 – **Atomic-Layer-Deposited BEOL Bilayer ZnO/In_2O_3 Transistors,** J.-Y. Lin, D. Zheng, Z. Zhang, Z. Lin, and P. D. Ye, *Purdue U.*

12:05 PM — Adjourn for lunch

Session 9: Advanced Logic & Oxide FETs III

Session Chair: C. W. Liu

1:30 PM — 9.1 *Invited* – **Oxide Semiconductor Transistors for LSI Application,** M. Kobayashi, *U. Tokyo, Japan*

2:00 PM — 9.2 – **Atomic Layer Deposition of WO_3-doped In_2O_3 for High-Performance BEOL-Compatible Transistors,** C. Yoo[1,2], B. Saini[1], J. Hartanto[1], C. E. Ruano Arens[1], J. D. Baniecki[2], W. Tsai[1], B. B. Triplett[1], and P. C. McIntyre[1,2], [1]*Stanford U.,* [2]*SLAC National Accelerator Laboratory*

2:20 PM — 9.3 – **First Principles Studies on Thermal Oxidation and Effects of Hydrogen Annealing at the Si/SiO_2 (110) Interface toward less than 2nm Node CFET,** K. Shiraishi[1], H. Kageshima[2], and A. Oshiyama[1], [1]*Nagoya U., Japan,* [2]*Shimane U., Japan*

2:40 PM — 9.4 – **Performance Enhancement of BEOL-Compatible Atomic-Layer-Deposited HZO-In_2O_3 Transistors by Interfacial Layer Engineering,** Z. Lin and P. D. Ye, *Purdue U.*

3:00 PM – 3:15 PM — Coffee Break

Session 10: 2D/TMD

Session Chair: X. Gong

3:15 PM — 10.1 – **Interface chemistry and band alignment study of Sn metal contact on bulk and 1-L MoS_2,** J. Roy, S. Y. Kim, and R. M. Wallace, *UT Dallas*

3:35 PM — 10.2 – **Revealing Surface Ferroelectric Switching Mechanism in α-In_2Se_3-Based Ferroelectric Semiconductor Junctions Through Cryogenic Investigation,** P. Tan, C. Niu, Z. Zhang, and P. D. Ye, *Purdue U.*

3:55 PM — 10.3 – **Impact of MoS_2 grain size on Dit(E) distributions and MOSFET performance,** X. Wu[1], V. K. Mootheri[1,2], Y. Shi[1,2], D. Cott[1], B. Groven[1], H. M. Silva[1], P. Morin[1], J. F. de Marneffe[1], I. Asselberghs[1], L. Goux[1], C. J. L. de la Rosa[1], G. S. Kar[1], M. Heyns[1,2], and D. Lin[1], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

4:15 PM — 10.4 – **Ferromagnetism in Tungsten Diselenide and the Role of Selenium Vacancies,** R. Younas[1], G. Zhou[1], X. Liu[1], S. Tiwari[2], W. G. Vandenberghe[2], B. Assaf[1], and C. L. Hinkle[1], [1]*U. Notre Dame,* [2]*UT Dallas*

4:35 PM – 4:50 PM — Coffee Break

Session 11: NVM/Neuro II

Session Chair: J. Coignus

4:50 PM — 11.1 *Invited* – **Ovonic Threshold Switching (OTS) Device for Selector Applications,** J. Lee, S. Ban, and H. Hwang, *POSTECH, Korea*

5:20 PM — 11.2 – **Investigation of Ferroelectric Tunnel Junction Characteristics Using Optimized WN_x Interfacial Capping Layer Thickness on 5 nm $Hf_{0.25}Zr_{0.75}O_2$ Anti-ferroelectric Film,** S. Das[1], Z.-F. Lou[2], A. Senapati[1], A. Aich[1], Y.-T. Chang[3], Y.-P. Chen[1,4], S.-Y. Huang[1,4], S. Maikap[1,4], C. W. Liu[2], and M.-H. Lee[2], [1]*Chang Gung U., Taiwan,* [2]*National Taiwan U., Taiwan,* [3]*National Taiwan Normal U., Taiwan,* [4]*Keelung Chang Gung Memorial Hospital, Taiwan*

5:40 PM — 11.3 – **InAs-based Ferroelectric and RRAM Devices: Operando Interface Characterization during Electrical Switching,** A. Irish, A. Persson, R. Atle, M. S. Ram, M. Borg, L.-E. Wernersson, and R. Timm, *Lund U., Sweden*

6:00 PM — End

7:00 PM – 10:00 PM — Conference Banquet & Limerick Contest

Saturday, December 16, 2023

Session 12: Wide Band Gap Semiconductors

Session Chair: W. G. Vandenberghe

8:30 AM 12.1 *Invited* – **Interface Trapping and Scattering in 4H-SiC MOSFETs,** S. Dhar, *Auburn U.*

9:00 AM 12.2 – **Dielectric Integration and interface defect engineering for β-Ga_2O_3 MOS devices,** A. E. Islam[1], A. Miesle[2], A. Dheenan[3], E. Shin[2], W. Wang[4], K. D. Leedy[1], S. Ganguly[1], K. J. Liddy[1], D. Dryden[1], G. Subramanyam[2], A. Arehart[3], S. Rajan[3], K. D. Chabak[1], and A. J. Green[1], [1]*Air Force Research Laboratory,* [2]*U. of Dayton,* [3]*The Ohio State U.,* [4]*Wright State U.*

9:20 AM 12.3 – **High-Throughput Screening and Structure Prediction for Interfaces,** W. Yu[1], Z. Zhang[1], X. Wan[1], Q. Gui[1], J. Robertson[1,2], and Y. Guo[1], [1]*Wuhan U., China,* [2]*U. Cambridge, UK*

9:40 AM 12.4 – **Capacitance-Voltage characterization of the HfO_2/β-Ga_2O_3 MOS system: Impact of thermal annealing,** K. Cherkaoui[1], A. Delrat[1], A. A. Gruszecki[2], J. Roy[2], R. Hawkins[2], R. M. Wallace[2], P. K. Hurley[1], and C. D. Young[2], [1]*Tyndall National Institute, Ireland,* [2]*UT Dallas*

10:00 AM 12.5 – **Achieving a High Thermally Conductive One Micron AlN deposition By High Power Impulse Magnetron Sputtering Plus Kick,** P. C. Lee[1], D. Contreras Mora[1], A. J. McLeod[1], M. Choi[2], D. Vaca[2], S. Kumar[2], and A. C. Kummel[1], [1]*UCSD,* [2]*Georgia Tech*

10:20 AM–10:35 AM Coffee Break

Session 13: Ferroelectrics II

Session Chair: S. Migita

10:35 AM 13.1 – **Interfacial-layer Free Ferroelectric Field-effect Transistors based on Anti-ferroelectric $Hf_xZr_{1-x}O_2$ and Oxide Semiconductor,** D. Chen, T. Cui, Z. Lin, J. Liu, G. Liu, M. Si, and X. Li, *Shanghai Jiao Tong U., China*

10:55 AM 13.2 – **Improvement of Fatigue Properties of Ferroelectric Hf_xZr_1−xO_2 Thin Films Using Surface Oxidized TiN Bottom-Electrode,** T. Onaya[1,2], T. Nabatame[2], T. Nagata[2], Y. Yamashita[2], K. Tsukagoshi[2], Y. Morita[3], H. Ota[3], S. Migita[3], and K. Kita[1], [1]*U. Tokyo, Japan,* [2]*National Institute for Materials Science, Japan,* [3]*AIST, Japan*

11:15 AM 13.3 – **Charged domain boundaries of ferroelectric ZrO_2,** K. Chae[1,2], M. Noor[2], N. Afroze[3], A. I. Khan[3], A. C. Kummel[1], and K. Cho[2], [1]*UCSD,* [2]*UT Dallas,* [3]*Georgia Tech*

11:35 AM 13.4 – **Ferroelectric capacitive memory window: asymmetry engineering, pulse-based non-destructive read, and analytical understanding from thermodynamic potential framework,** S. Mukherjee[1,2], J. Bizindavyi[1], S. Clima[1], Y. Xiang[1], M. I. Popovici[1], P. Bagul[1,2], G. De[1,2], N. Bazzazian[1], F. Catthoor[1,2], S. Yu[3], V. V. Afanas'ev[1,2], and J. Van Houdt[1,2], [1]*imec, Belgium,* [2]*U. Leuven, Belgium,* [3]*Georgia Tech*

11:55 AM End

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