TSMC Property

Interface State Analysis on Nonsilicon Semiconductors and The Role of Heterostructures

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December 1, 2010

Nonsilicon Interfaces - Outline

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Introduction to Nonsilicon Channel Materials

Quiz: Do You Understand Nonsilicon Interface Data?

Interface State Analysis

- *Introduction*
- *Admittance-voltage (capture/emission):*
  - *Flow chart for trap evaluation*
  - *Example D_{it} quantification*
- *Photoluminescence intensity (recombination)*

D_{it} and Heterostructures in MOSFETs

- *Heterostructure barrier layer: Introduction*
- *Shifting D_{it} distribution in energy space*
- *D_{it} amplification or reduction – Barrier layer case studies*

Quiz Solution

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Quiz Solution

Introduction to Nonsilicon Channels

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Material	Lattice constant	Bandgap	Electron injection velocity @ 0.5 V
Silicon	0.5431 nm	1.12 eV	$0.5x10^7$ cm/s
GaAs	0.5653 nm	1.42 eV	$1.5x10^7$ cm/s
$In_{0.5}Ga_{0.5}As$	0.5869 nm	0.74 eV	$2.7x10^7$ cm/s
InAs	0.6058 nm	0.35 eV	$3.7x10^7$ cm/s
InSb	0.6479 nm	0.17 eV	$4.6x10^7$ cm/s

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Interface State Analysis: Introduction

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Many measurement techniques, among them

- Admittance-voltage: Capacitance-voltage (C-V) high/low frequency, low frequency, Terman method …
- Admittance-voltage: Conductance-voltage (G-V)
- Charge Pumping
- Photoluminescence intensity (PL-I) …

Physics

- Capture/emission of charge carrier at trapping center
- Recombination of charge carriers at trapping center

Major Parameters

- Bandstructure (bandgap, direct, indirect …)
- 0.35 eV ≤ bandgap ≤ 1.42 eV

Interface State Analysis: Introduction

TSMC Property

Many measurement techniques, among them

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- **Photoluminescence intensity (PL-I) …**

Physics

- **Capture/emission of charge carrier at trapping center**
- **Recombination of charge carriers at trapping center**

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Interface State Analysis: Introduction

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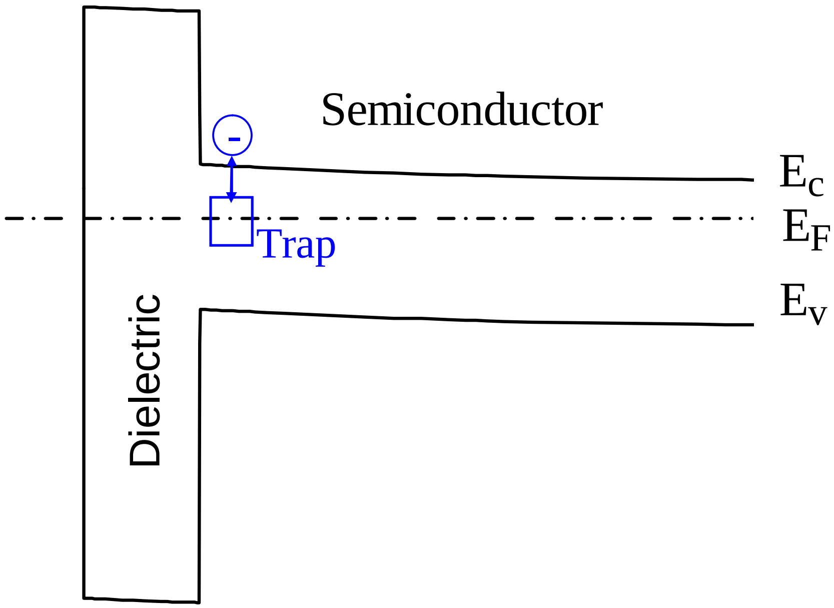
Carrier Capture/Emission τ



- τ is exponential function of E_T
- Interface state density $D_{it} = f(E_T)$

Interface State Analysis: Introduction

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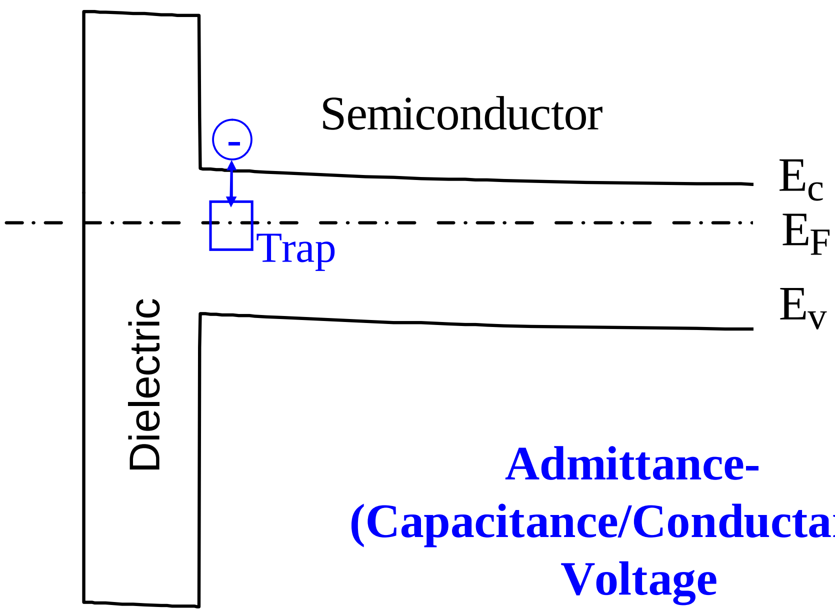
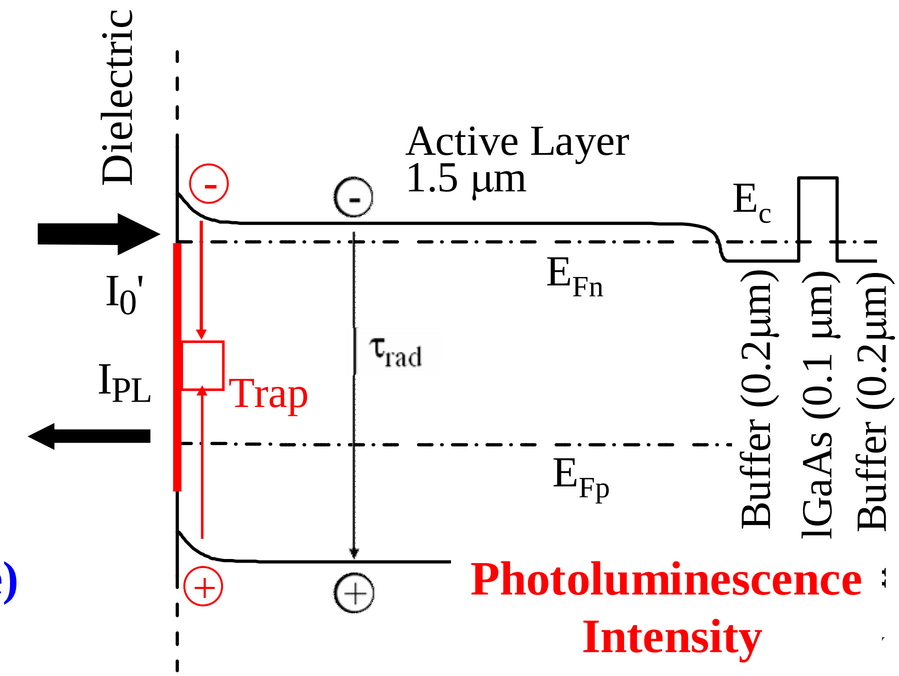
Carrier Capture/Emission τ

Carrier Recombination $\tau_{n/p}$



Admittance-(Capacitance/Conductance) Voltage



Photoluminescence Intensity

- τ is exponential function of E_T
- Interface state density $D_{it} = f(E_T)$

- $\tau_{n/p} \neq f$ (trap energy E_T)
- D_{it} integrated over bandgap

Admittance-Voltage Techniques: Examples

High/low frequency C-V

- Traps must follow DC sweep (quasi-equilibrium)
- Traps must follow low frequency (quasi-static) signal
- Traps must not follow high frequency signal

Low frequency C-V

- Traps must follow DC sweep (quasi-equilibrium)
- Traps must follow low frequency (quasi-static) signal
- Advanced model required to extract D_{it}

Terman Method (C-V)

- Traps must follow DC sweep (quasi-equilibrium)
- Traps must not follow ac signal

G-V Method

- Traps must follow DC signal (quasi-eqilibrium)
- Traps must partially follow ac signal

Admittance-Voltage Techniques: Examples

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Example C-V Analysis: High/low Frequency

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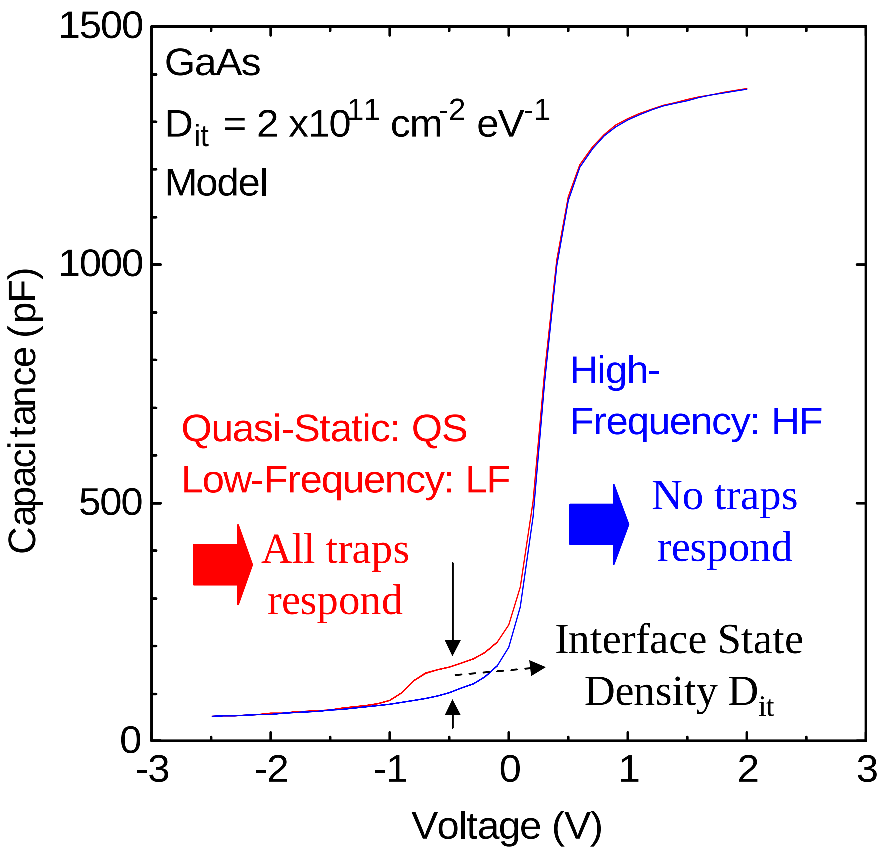

41st IEEE Semiconductor Interface Specialists Conference

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Example C-V Analysis: High/low Frequency

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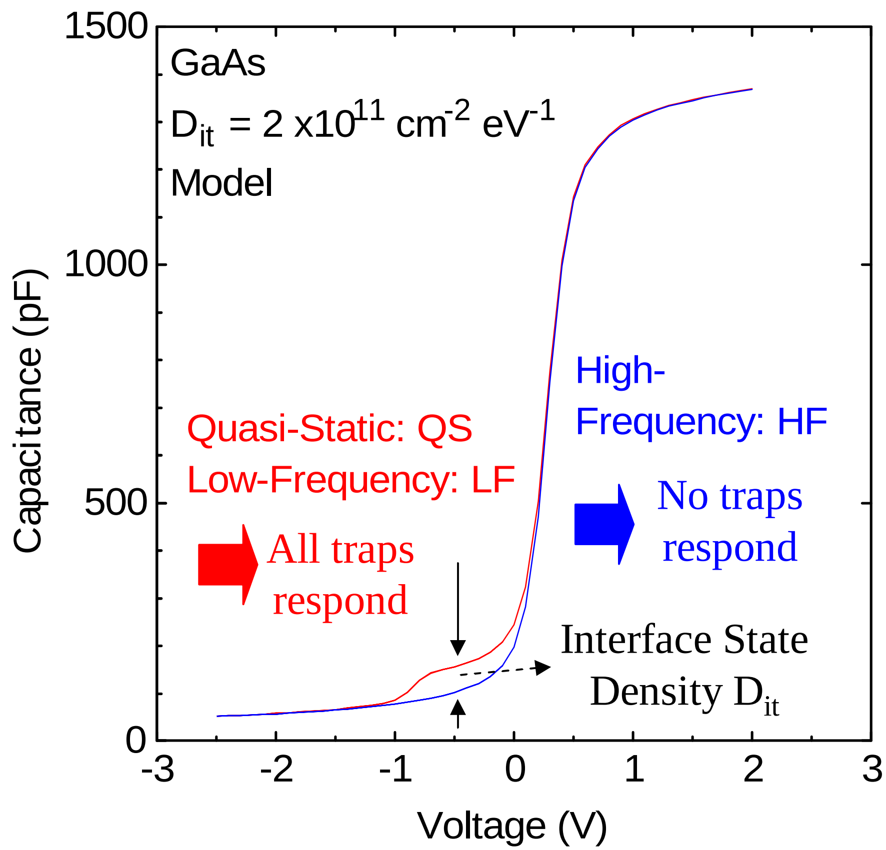
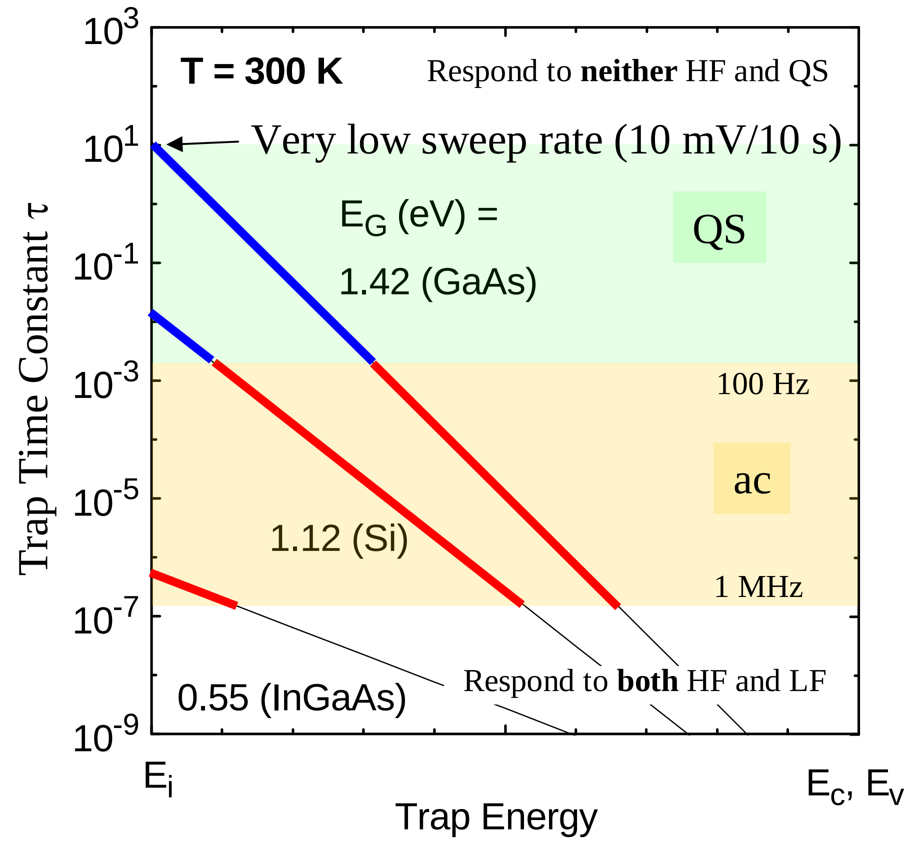
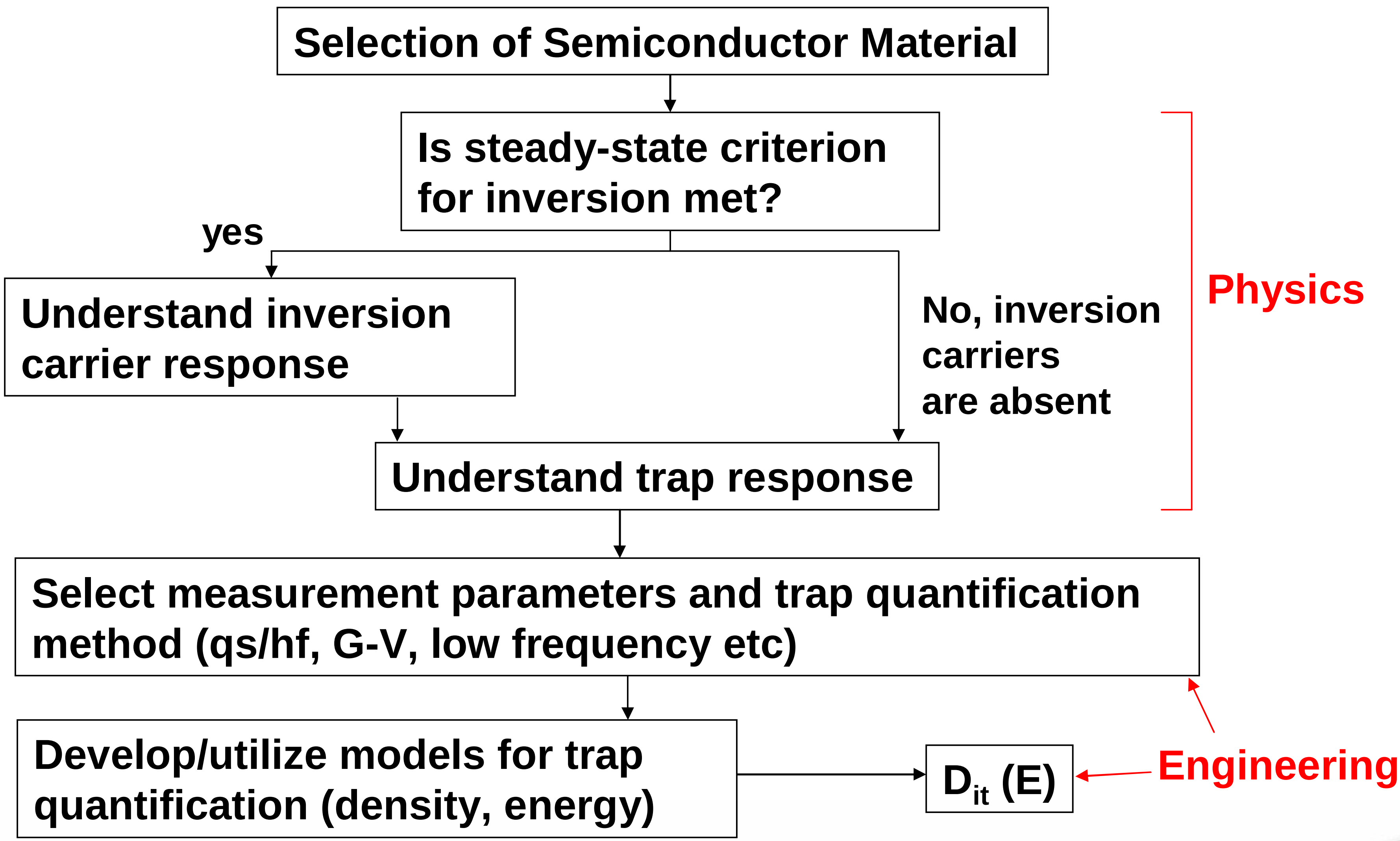




When changing the bandgap, MOS physics needs to be investigated and measurement parameters adjusted accordingly

Admittance-Voltage: Flow Chart



Admittance-Voltage: Flow Chart

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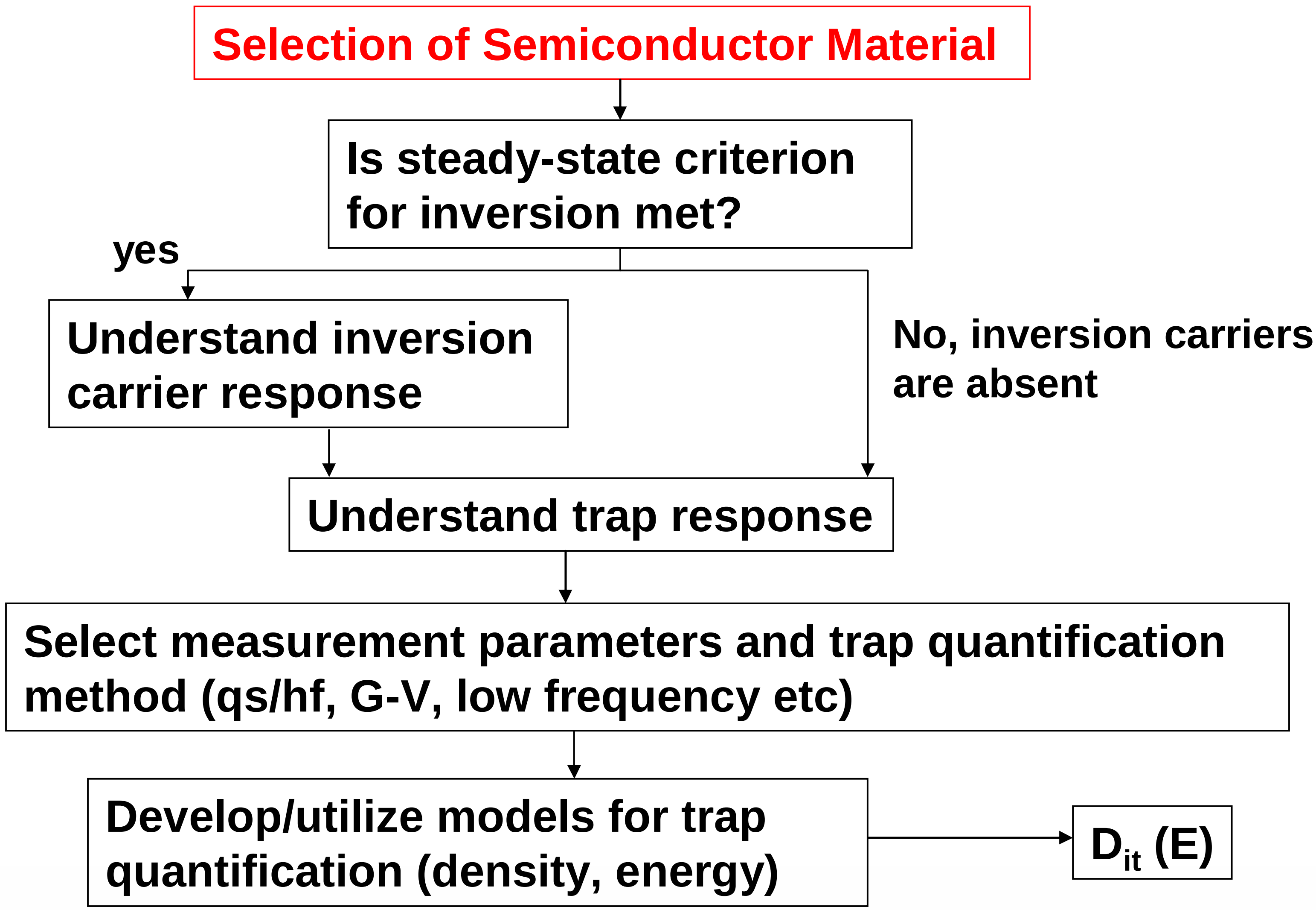

Selection of Semiconductor Material

Very important because:

- *Trap time constants vary over many orders of magnitude as a function of bandgap, energy position, and temperature*
- *Measurement techniques need to be properly selected*
- *Measurement parameters need to be adjusted*
- *Models for trap quantification need to be suitable*

In this tutorial:

- *Start with a wide range of materials from InAs to GaAs*
  0.35 eV $\leq$ bandgap $\leq$ 1.42 eV: inversion vs. deep depletion condition
- *Subsequently focus on InAs: dispersion due to traps, selection of measurement techniques, parameters, and trap quantification model*

Admittance-Voltage: Flow Chart

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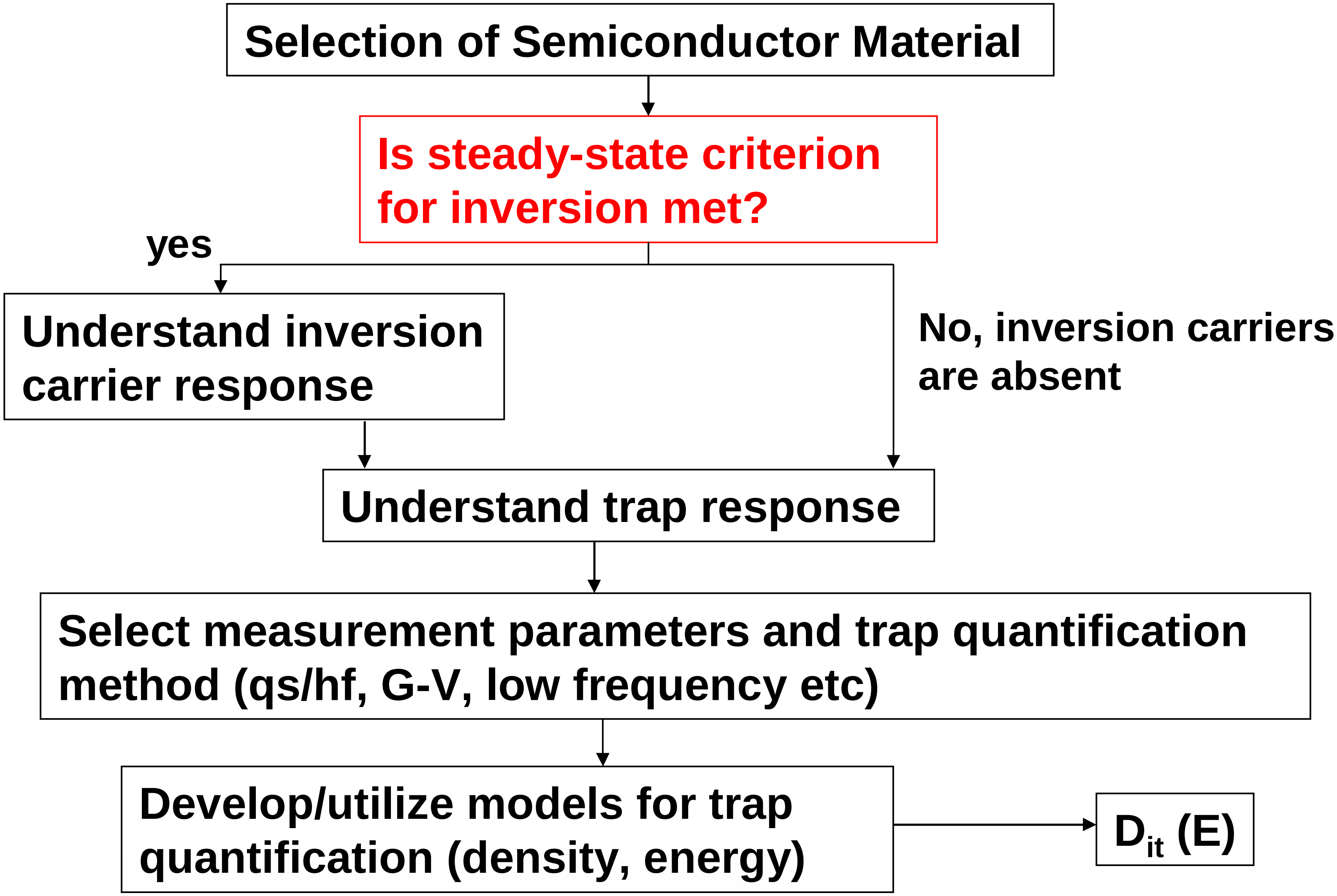

Steady-State Criterion for Inversion (n-type)

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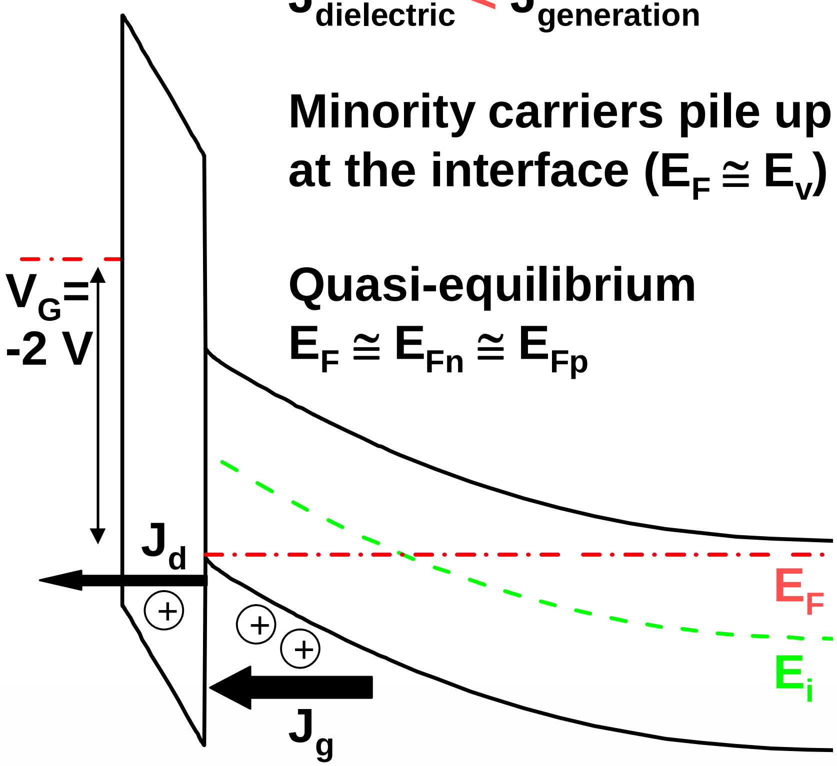
INVERSION

$J_{dielectric} < J_{generation}$

Minority carriers pile up at the interface ($E_F \cong E_v$)

Quasi-equilibrium
$E_F \cong E_{Fn} \cong E_{Fp}$

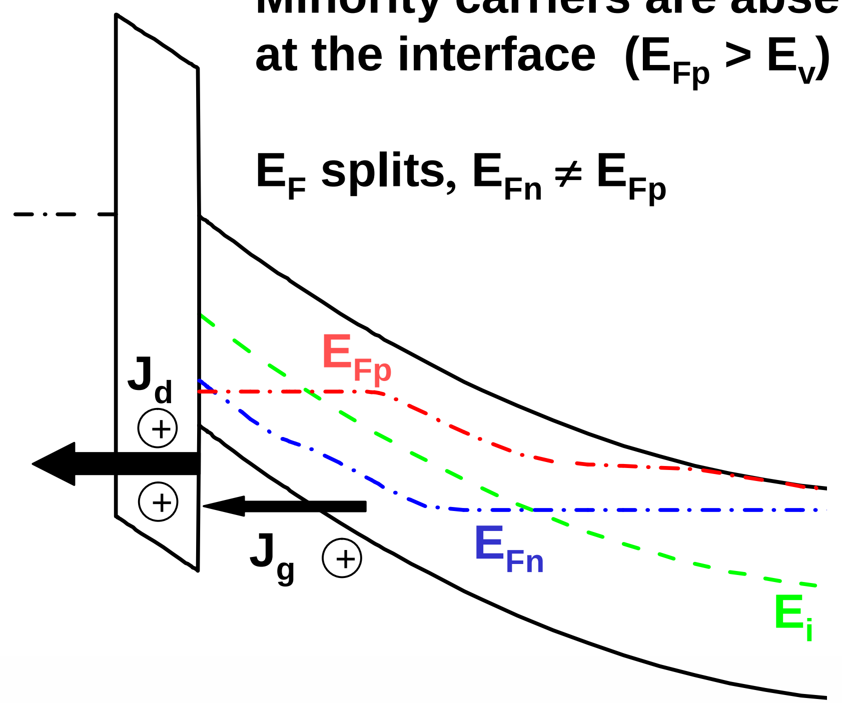


DEEP DEPLETION

$J_{dielectric} > J_{generation}$

Minority carriers are absent at the interface ($E_{Fp} > E_v$)

E_F splits, $E_{Fn} \neq E_{Fp}$



JAP, vol. 81, pp. 7647 (1997)

Quasi-Equilibrium vs. Steady-State Deep Depletion

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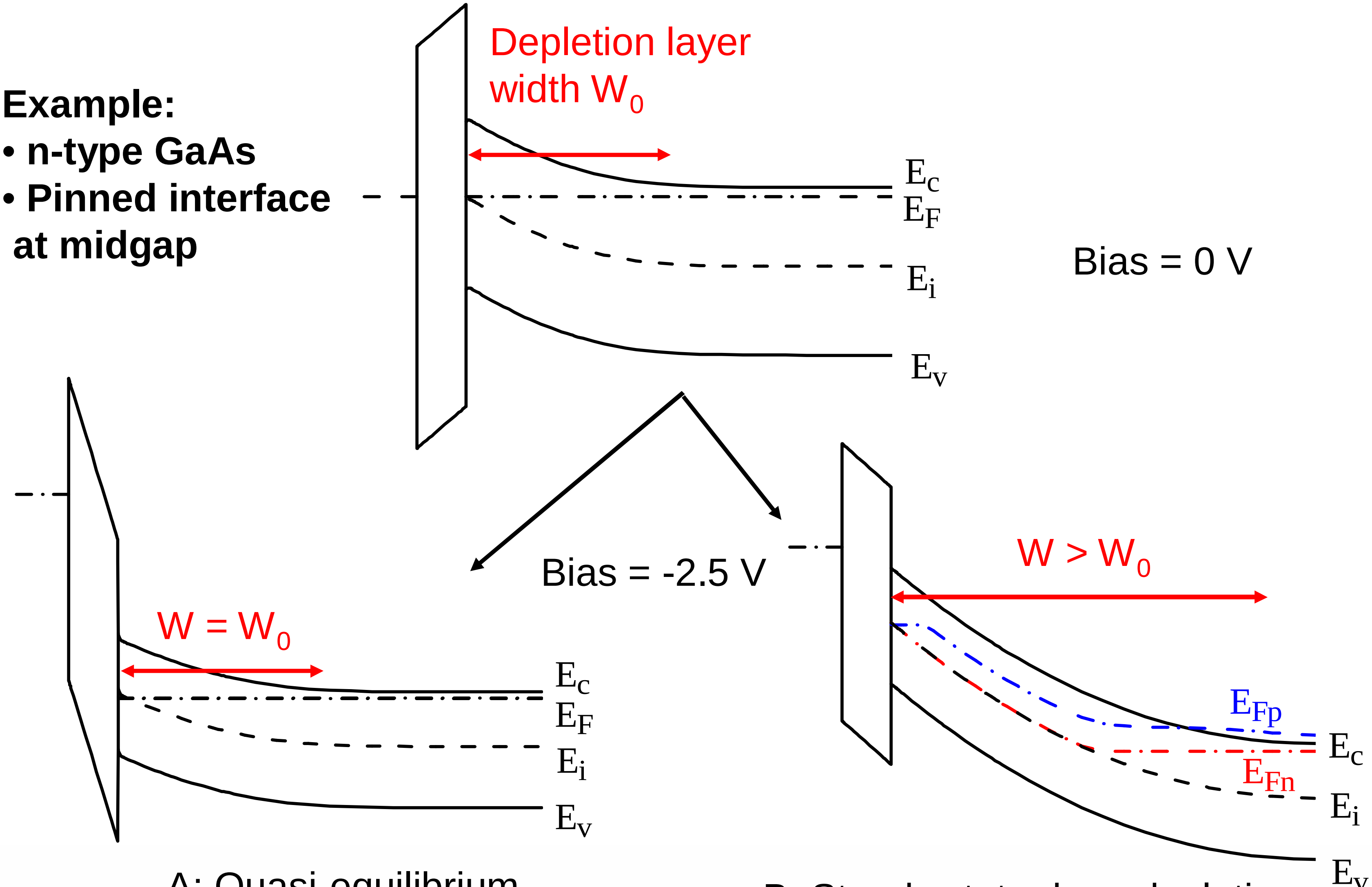
Example:
- **n-type GaAs**
- **Pinned interface at midgap**



A: Quasi-equilibrium

B: Steady state deep depletion

A: Quasi-Equilibrium and Pinned Fermi Level

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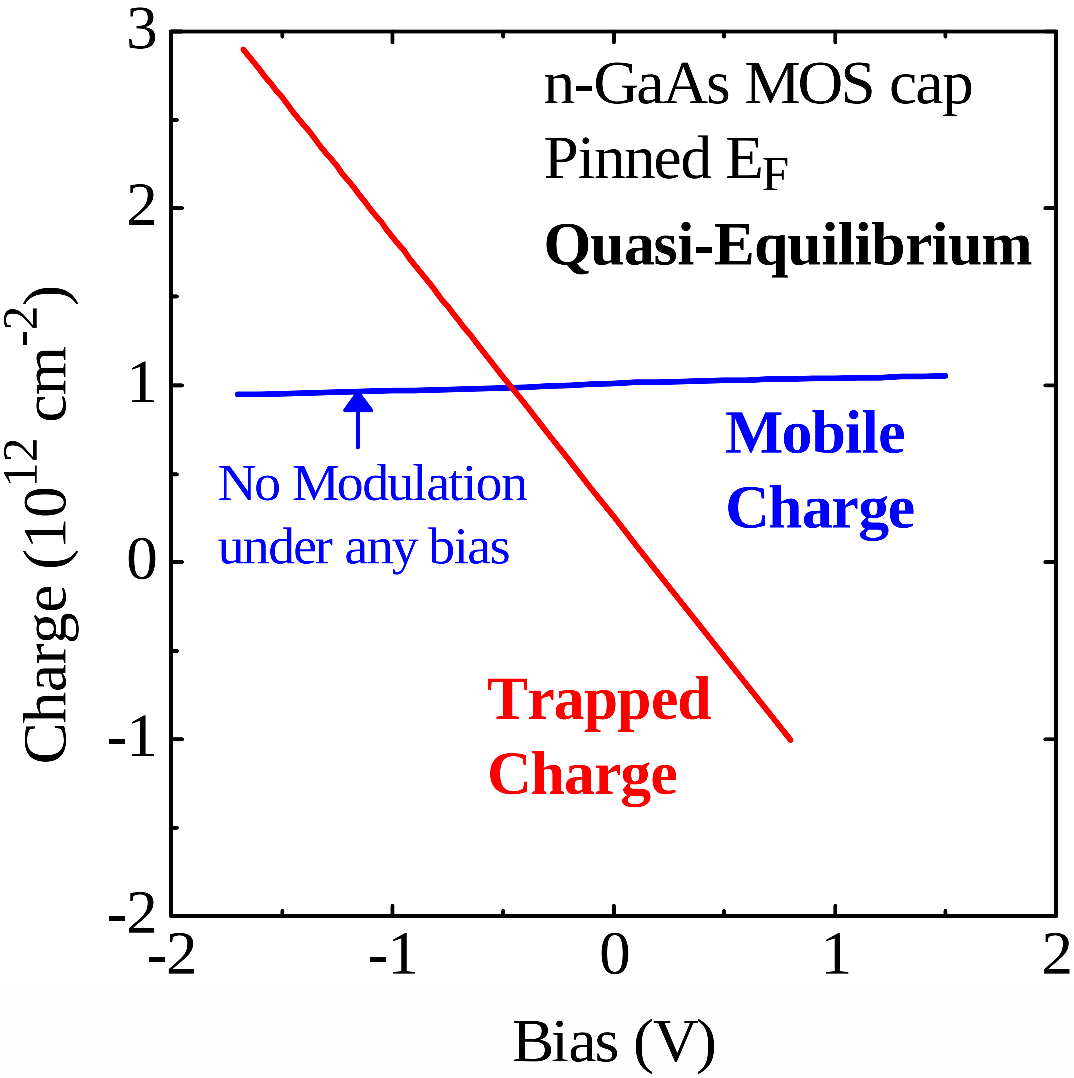

Quasi-equilibrium:

$\Rightarrow$ Mobile Charge **can not** be modulated

$\Rightarrow$ D_{it} **is** detectable at the capacitor's terminals

MOSFETs **do not** work

B: Deep Depletion and Pinned Fermi Level

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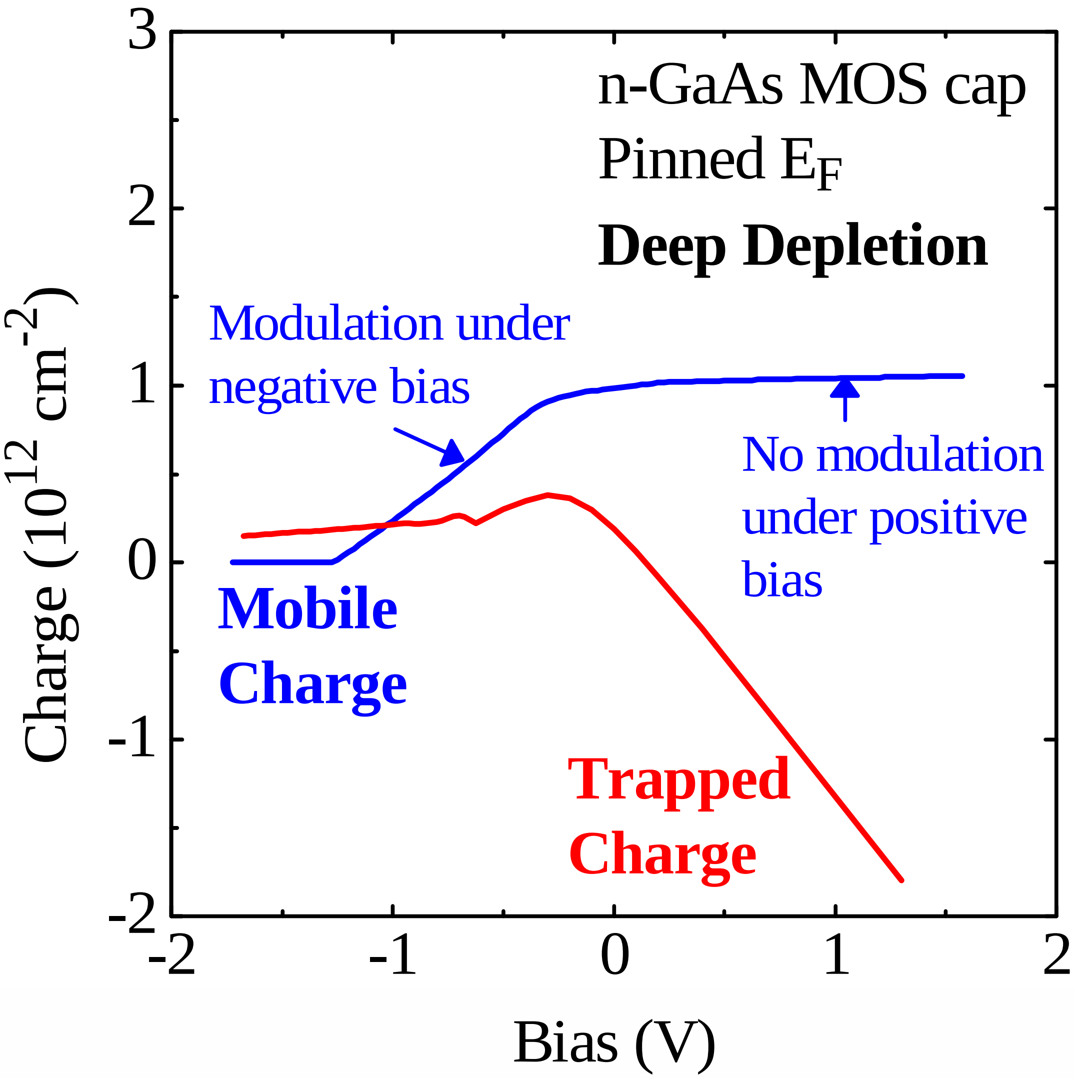

Positive Bias:

⇒ No modulation of mobile charge possible (Enhancement-mode MOSFETs **do not** work)

Deep Depletion:

⇒ Mobile Charge **can be** modulated and depleted (Depletion-mode MOSFETs **can** work)

⇒ D_{it} **is not** detectable at the capacitor's terminals

Steady-State Criterion for Inversion (300 K)

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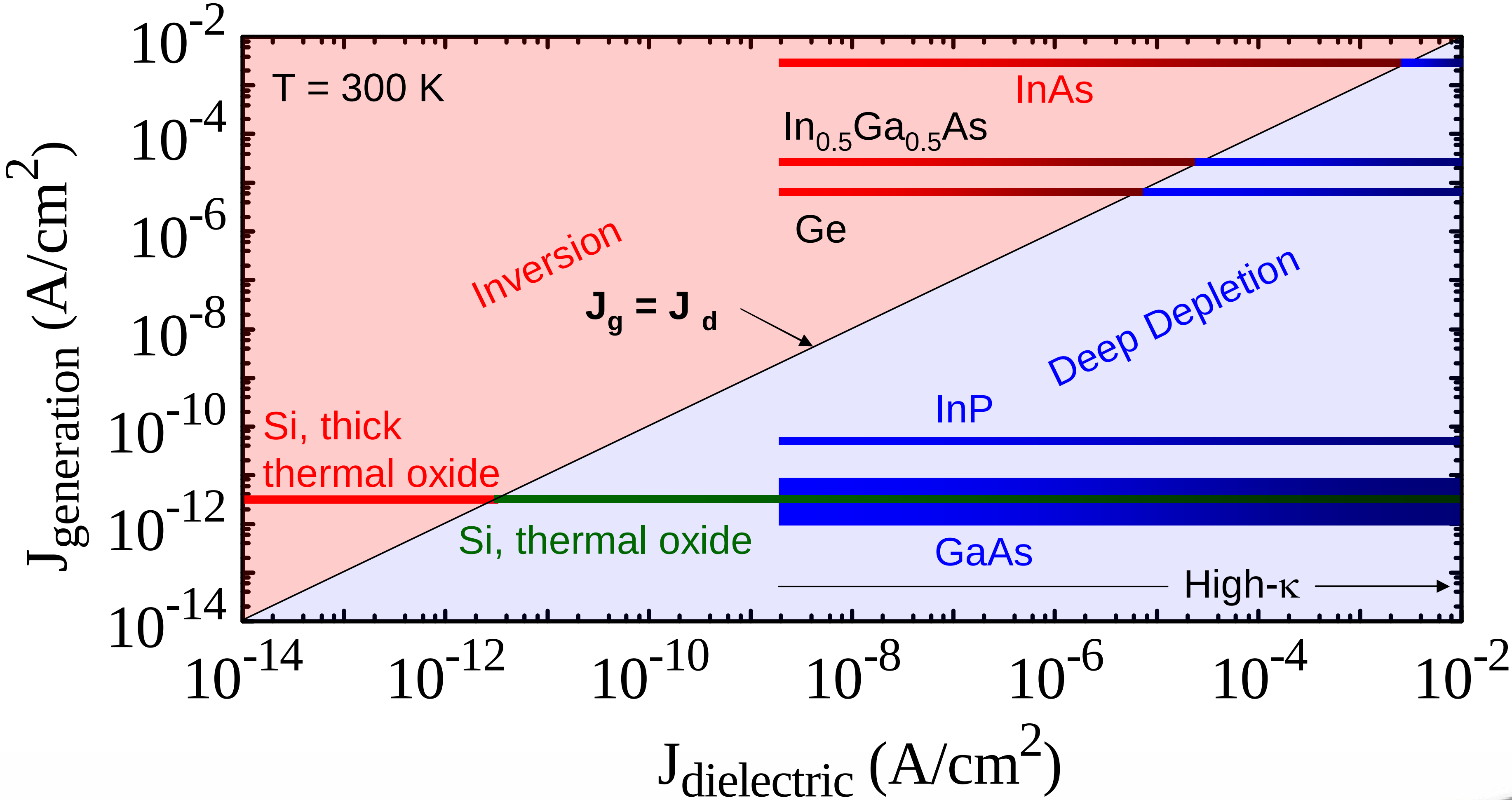

Parameters: bulk lifetime, effective generation length

Admittance-Voltage: Flow Chart

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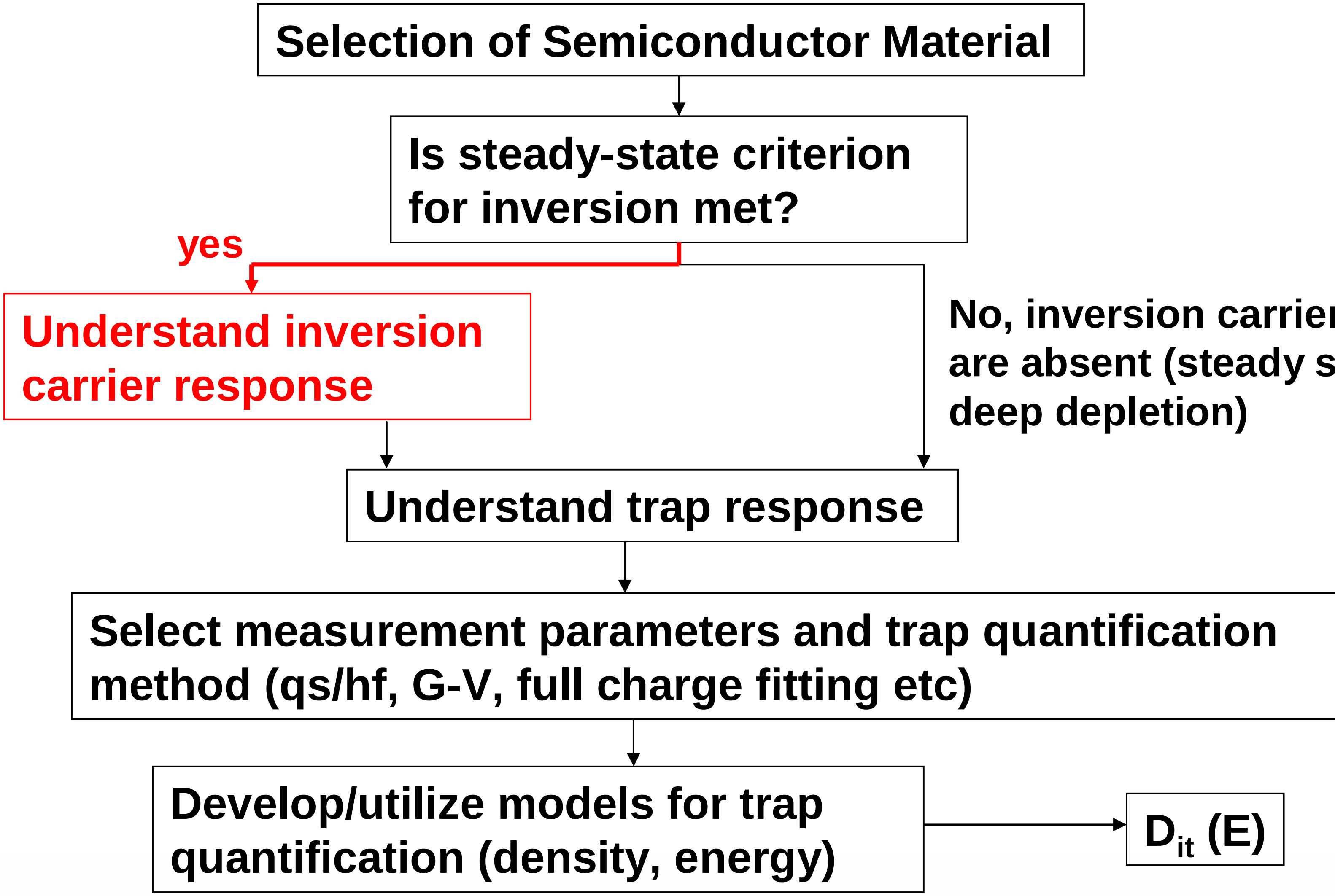

Inversion Carrier Response (f_m)

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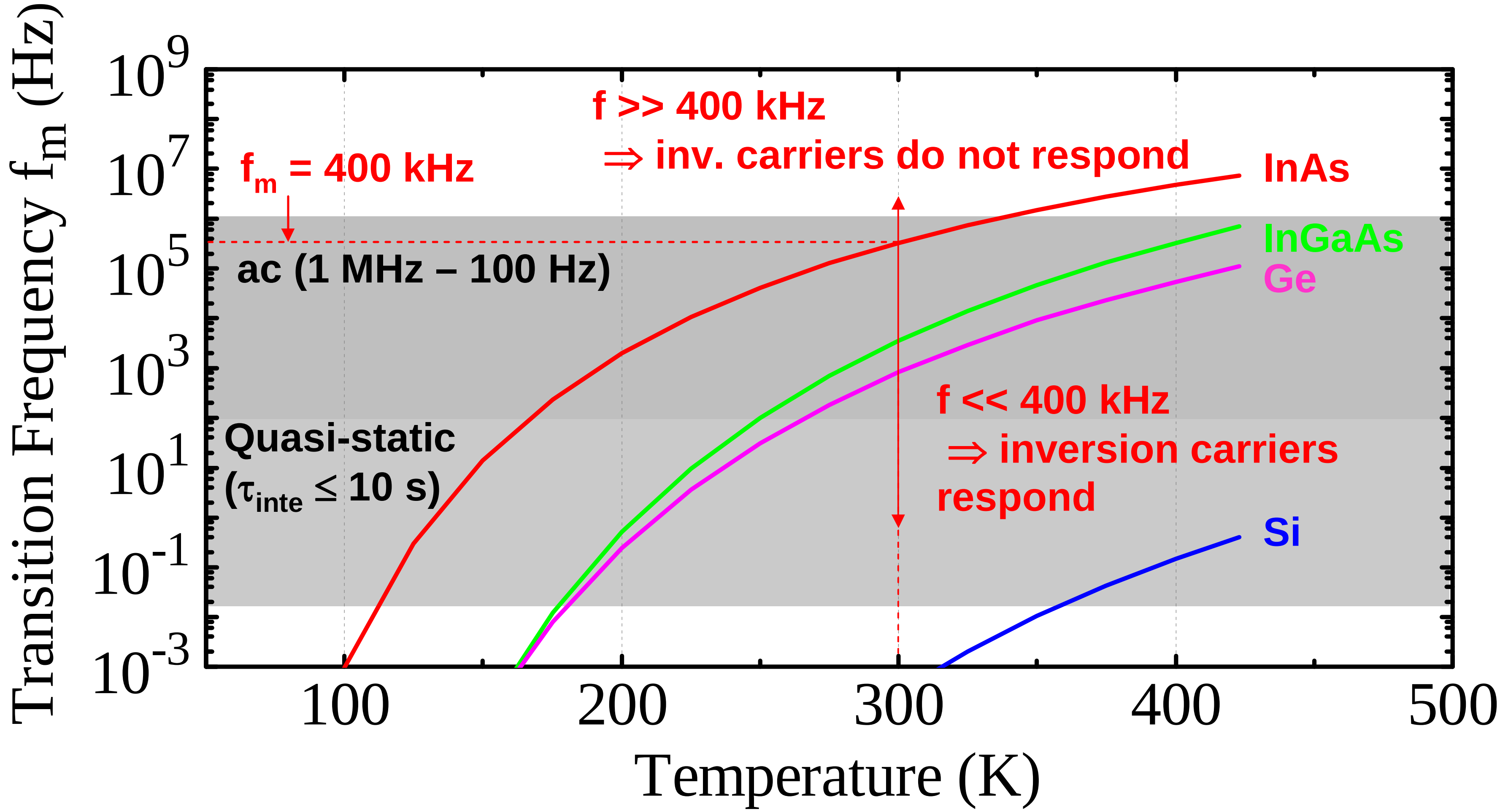

Example: InAs at 300 K

Parameters: bulk lifetime, doping density

Admittance-Voltage: Flow Chart

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Selection of Semiconductor Material

Is steady-state criterion for inversion met?

yes → Understand inversion carrier response

No, inversion carriers are absent

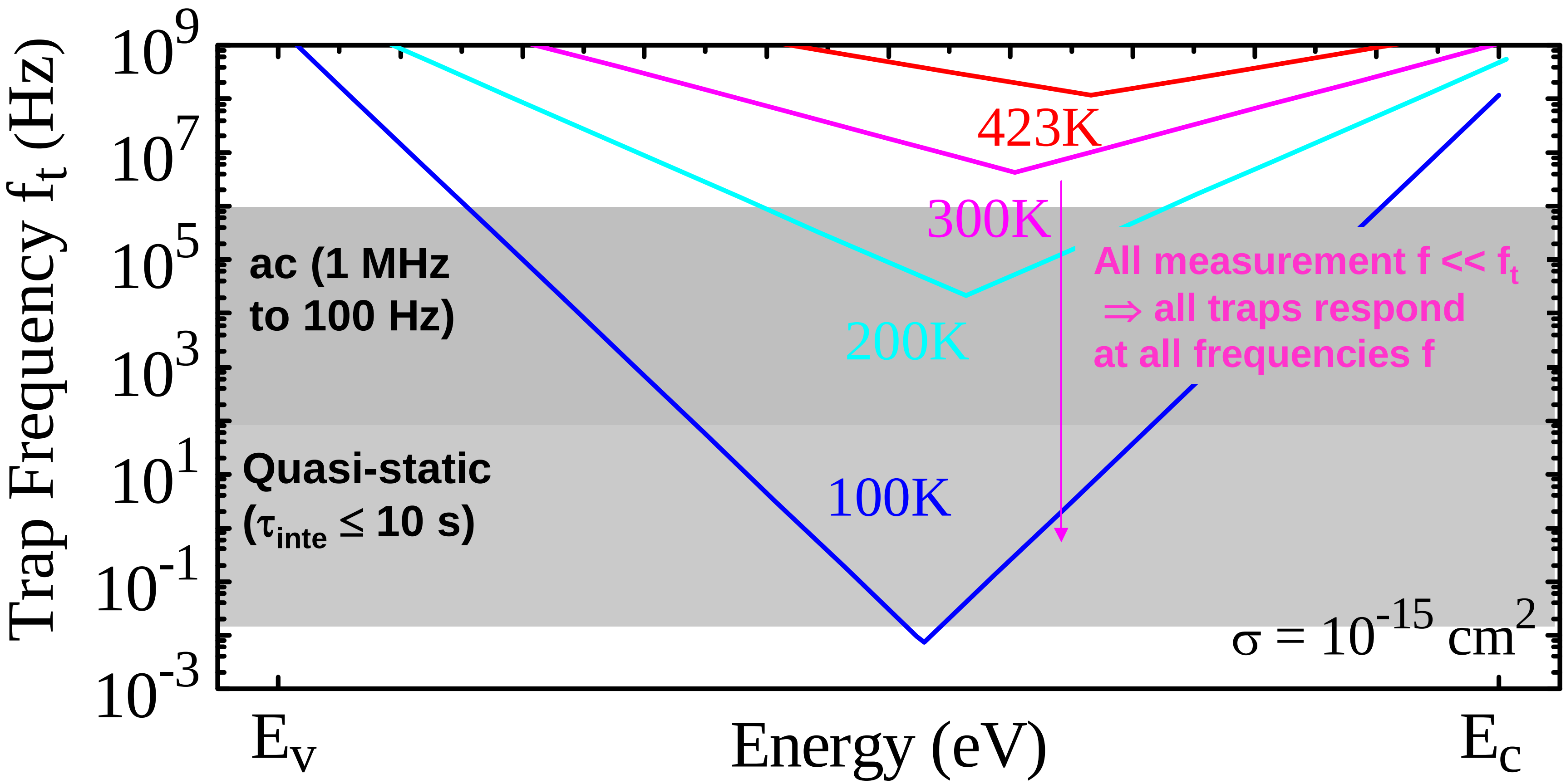
Understand trap response

InAs

Select measurement parameters and trap quantification method (qs/hf, G-V, low frequency etc)

Develop/utilize models for trap quantification (density, energy) → D_{it} (E)

Trap Response (InAs)



Example: 300 K

Admittance-Voltage: Flow Chart

TSMC Property

Selection of Semiconductor Material

↓

Is steady-state criterion for inversion met?

- yes → Understand inversion carrier response → Understand trap response
- No, inversion carriers are absent → Understand trap response

↓

Select measurement parameters and trap quantification method (qs/hf, G-V, low frequency etc)

↓

Develop/utilize models for trap quantification (density, energy) → D_{it} (E)

Measurement Parameters and Trap Quantification Method (InAs)

Findings (predictions):

- Inversion carriers respond for $f < 100$ kHz at 300K
- All traps throughout the bandgap are expected to respond to $f < 100$ kHz at 300K ($\sigma = 10^{-15}$ cm^2)

$\Rightarrow$ No frequency dispersion expected for $f < 100$ kHz

Selecting measurement parameters:

$\Rightarrow$ ac measurements (100 Hz – 100 kHz) at 300K

Selecting appropriate trap quantification method:

$\Rightarrow$ Low frequency C-V method (all traps must respond to dc sweep and ac signal) to extract D_{it} is most convenient

$\Rightarrow$ other methods such as lf/hf, G-V, and Terman rely on partial trap response and don't appear to be as suitable (require to go to low temperature and/or much higher frequency)

Capacitance-Voltage measurements (InAs)

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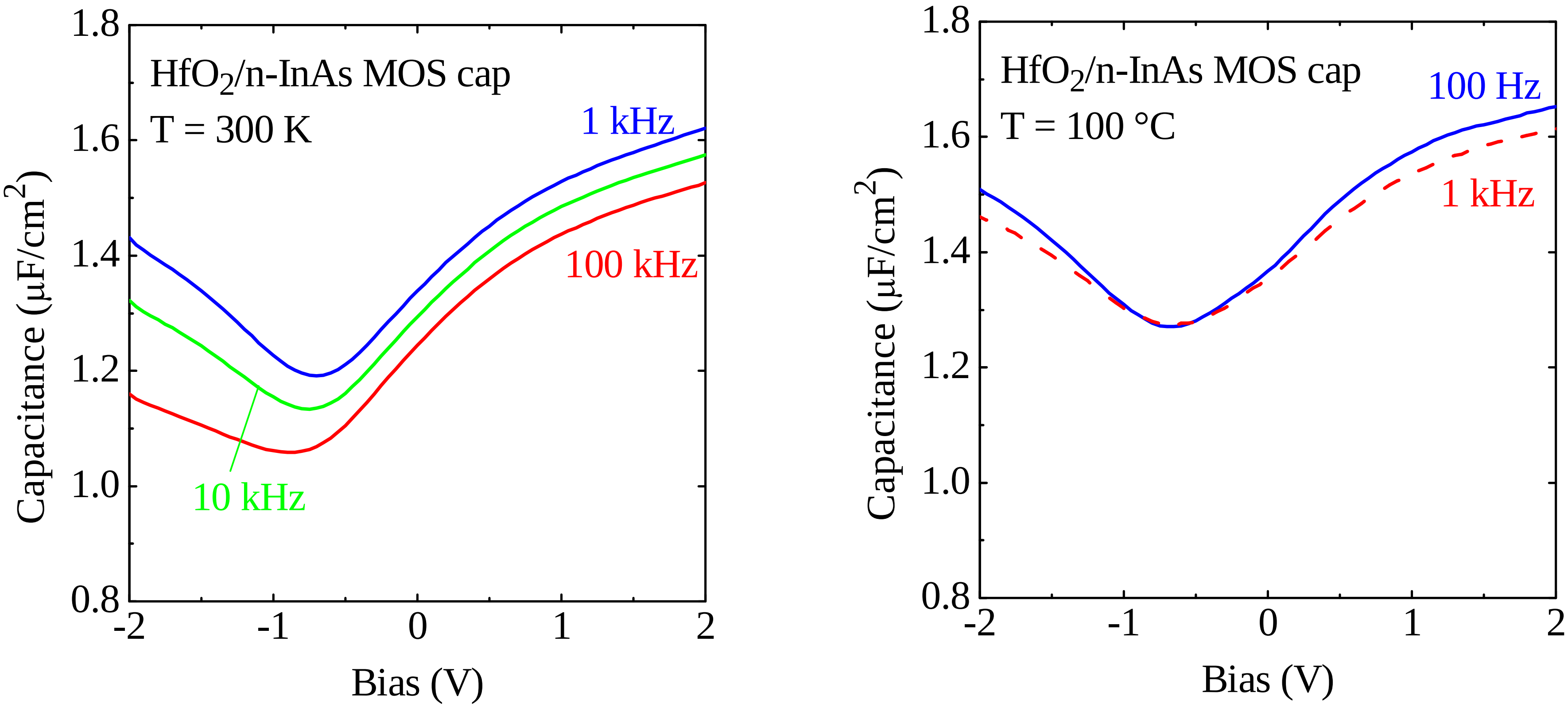

Frequency dispersion is experimentally observed at 300 K and below f = 100 kHz contrary to expectations

C-V curves essentially collapse onto each other at elevated T and low f ⇒ these curves are suitable for the low frequency method

Reconcile Prediction with Reality (InAs)

Prediction: No frequency dispersion for $f < 100$ kHz

Measurement: Dispersive between 1 MHz and 1 kHz, curves essentially collapse onto each other only for $f < 1$ kHz at elevated temperature

Prediction can be reconciled with reality assuming small (effective) capture cross section ($\leq 10^{-18}$ cm^2)

$\Rightarrow$ this points toward border traps or oxide bulk traps

$\Rightarrow$ abruptness of interface is likely major issues

Effect of Capture Cross Section σ on Trap Response (InAs)

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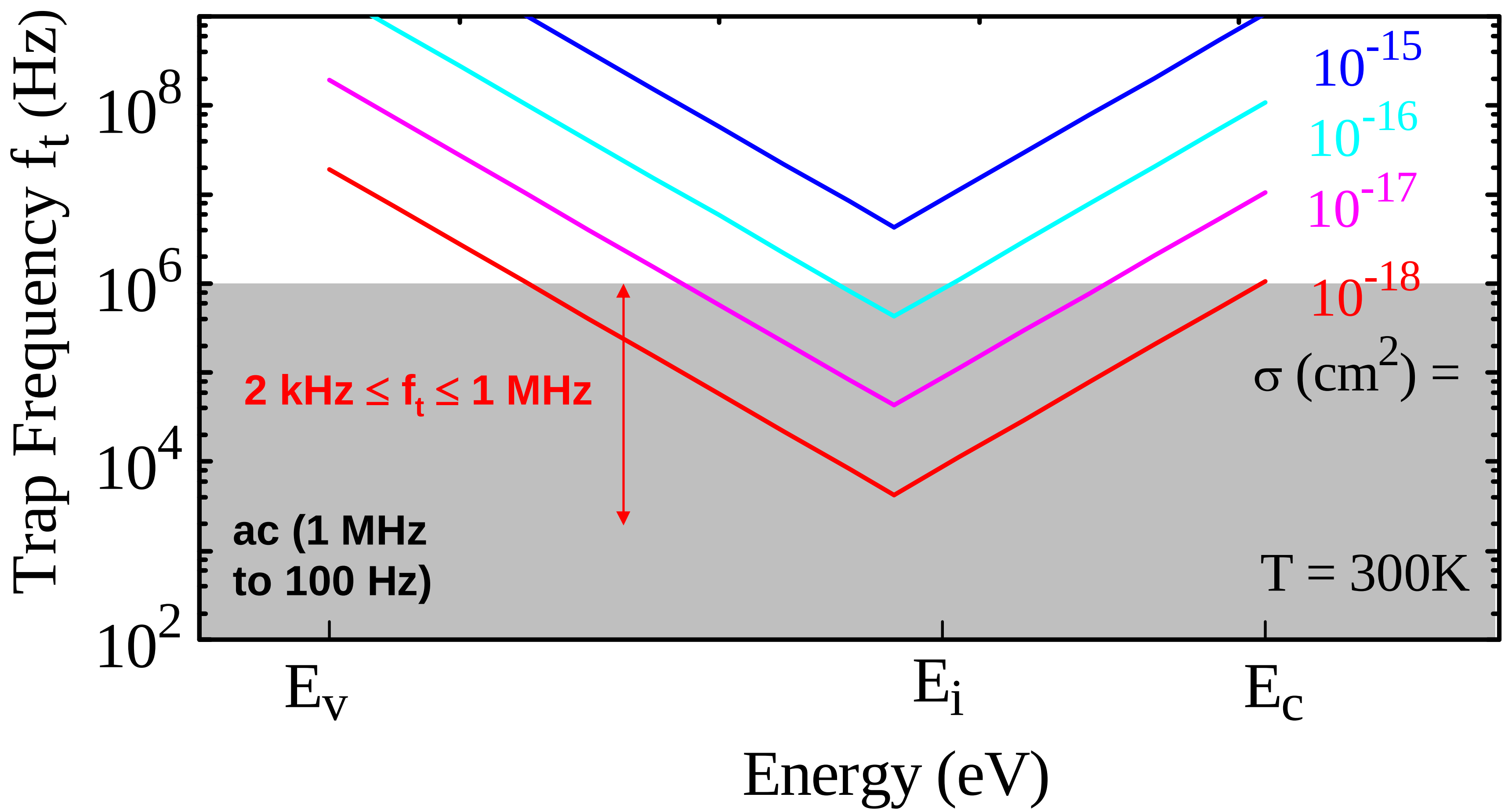

Experimentally observed frequency dispersion can be explained by small capture cross sections of e.g. $\sigma = 10^{-18}$ cm^2

Reconcile Prediction with Reality (InAs)

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Next: Low frequency method to determine D_{it} distribution from 100 Hz, 100 °C C-V data

Admittance-Voltage: Flow Chart

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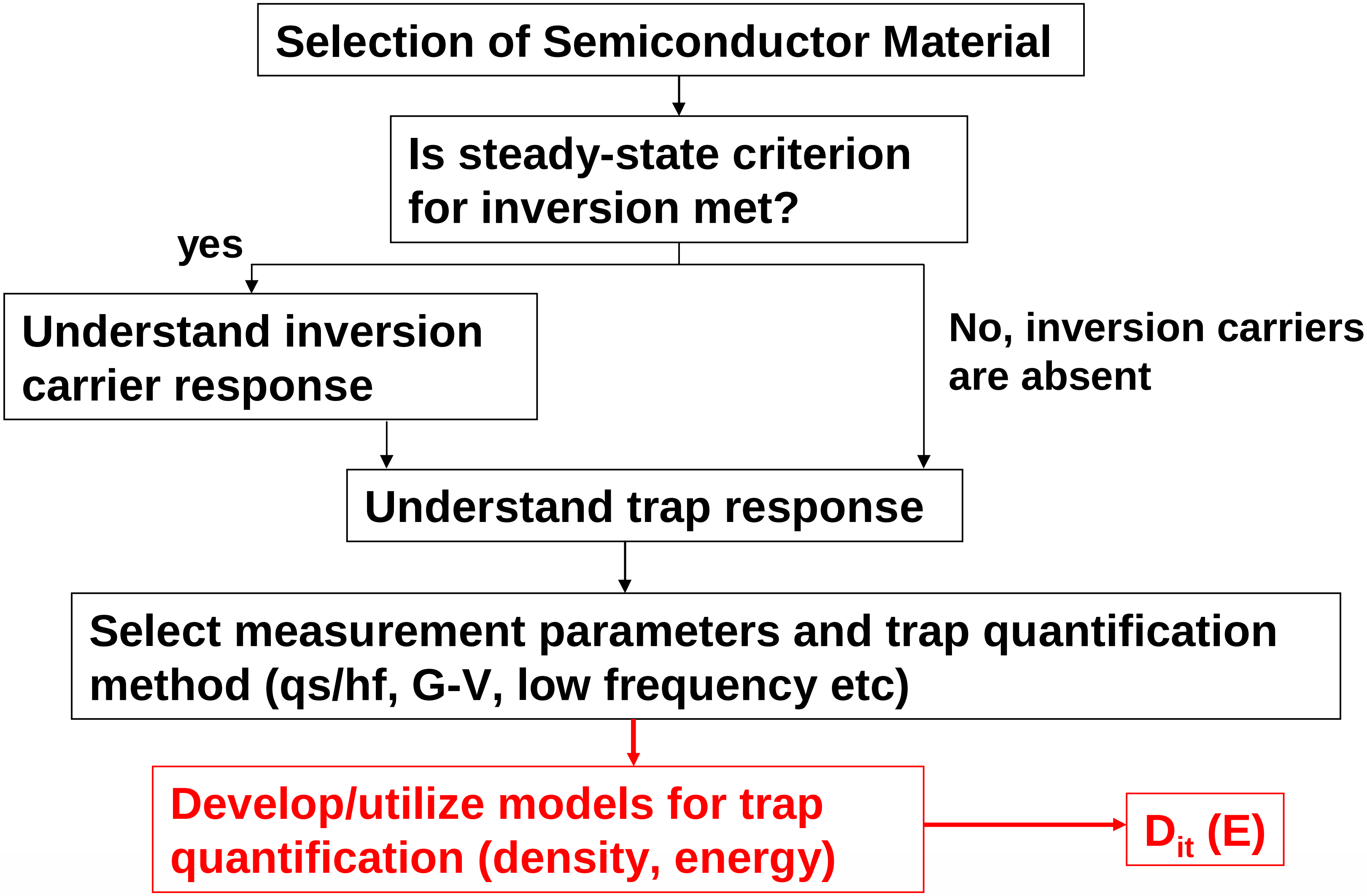
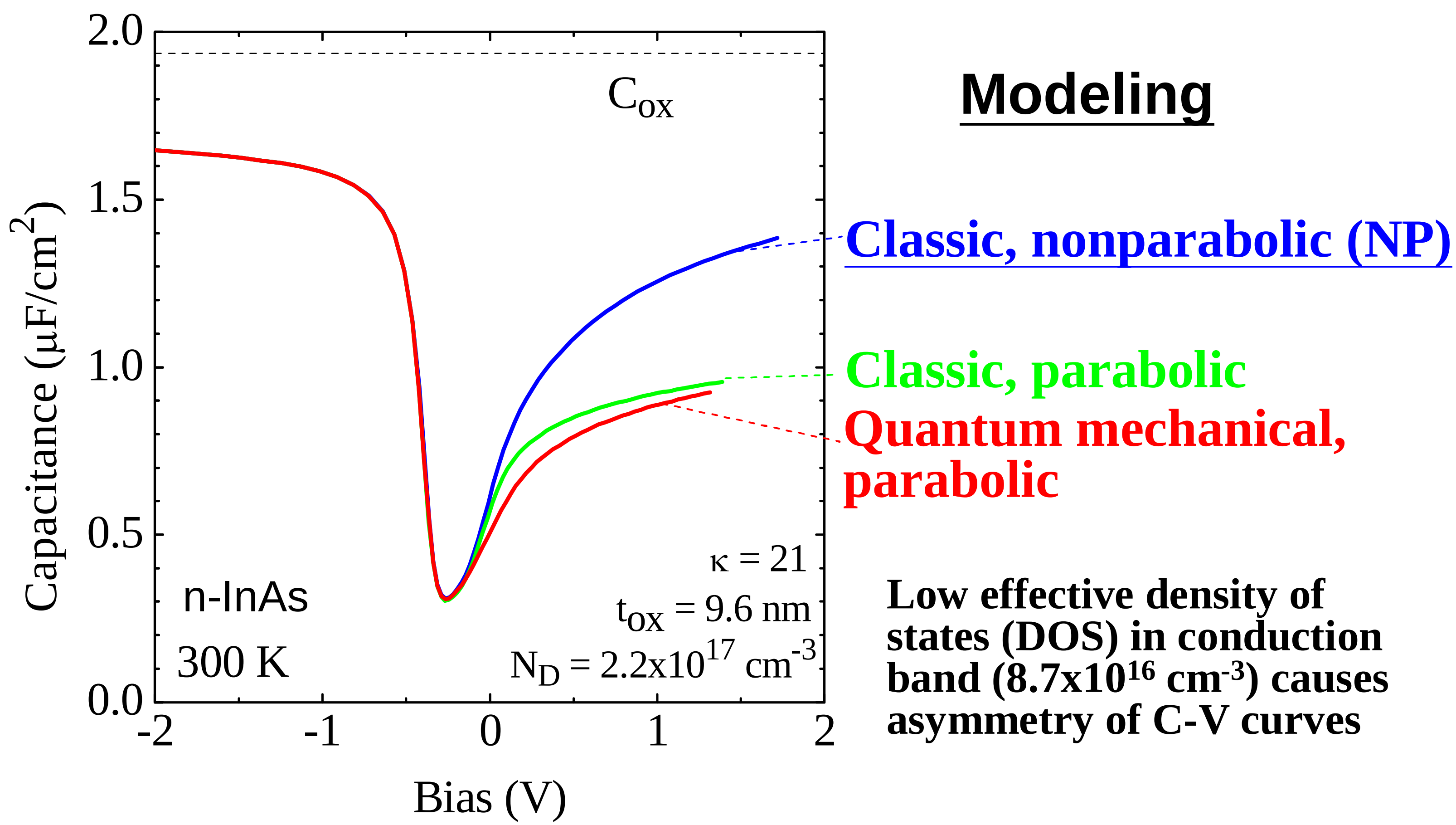


D_{it} Quantification: Low Frequency Method (InAs)

TSMC Property



Modeling

Low effective density of states (DOS) in conduction band (8.7×10^{16} cm^{-3}) causes asymmetry of C-V curves

- **Model needs to include Fermi-Dirac statistics, nonparabolicity, quantization $\Rightarrow$ accurate solution requires tight binding or k·p**
- **NP model is within 5-10% for bulk InAs (E. Lind et al., APL vol. 96, 2010)**

D_{it} Quantification: Low Frequency Method (InAs)

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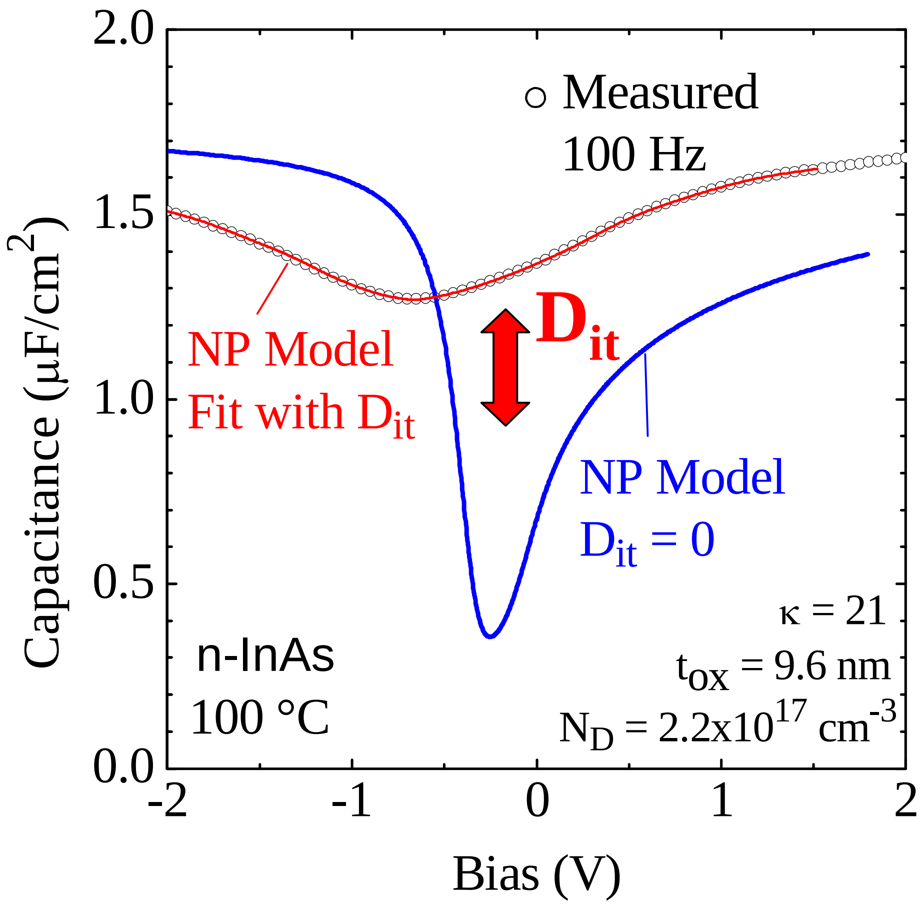

Simulations are fitted to measured MOS cap results using numerical technique

⇒ **Excellent fit of modeled data to MOS cap results**

Discrepancy between ideal model (D_{it} = 0) and experimental capacitor data due to D_{it}

D_{it} Quantification: Low Frequency Method (InAs)

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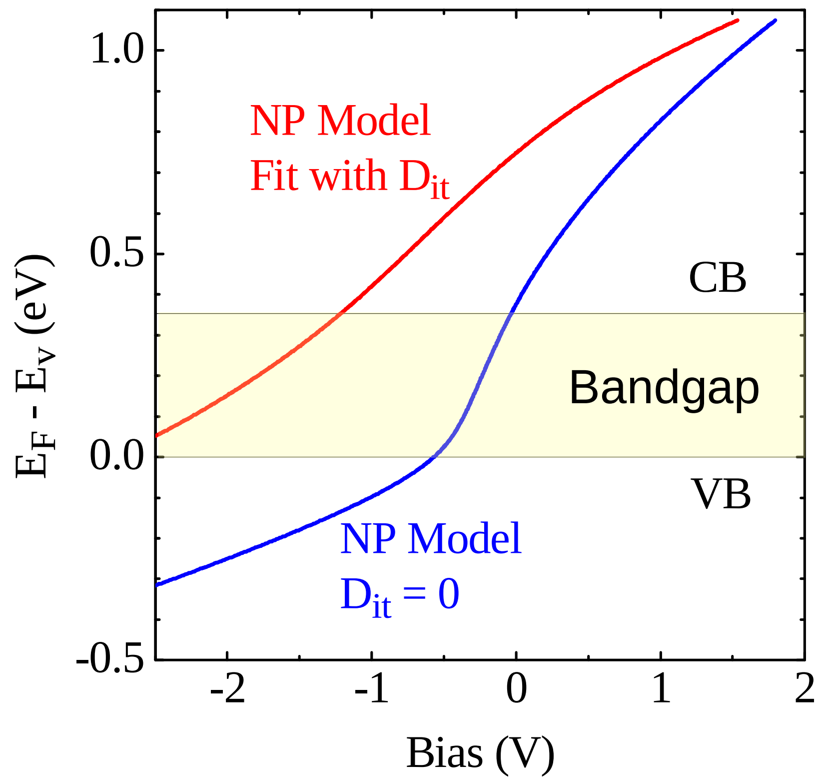
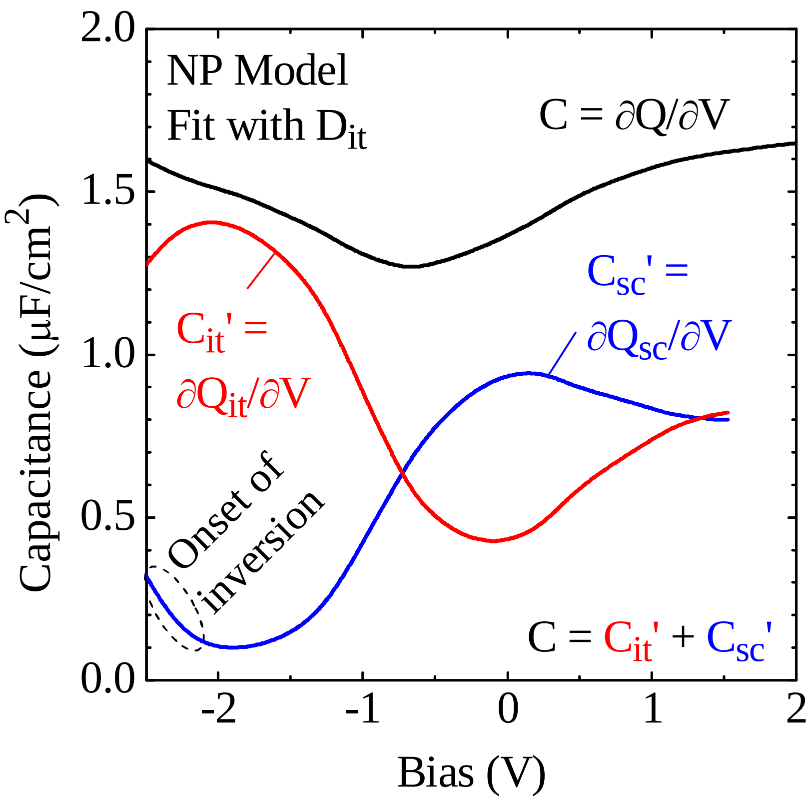
Insights





- Due to interface traps, Fermi level at interface does not move into VB
- No minority carrier contribution to gate capacitance down to -2V (upturn of total capacitance is due to D_{it})

D_{it} Quantification: Low Frequency Method (InAs)

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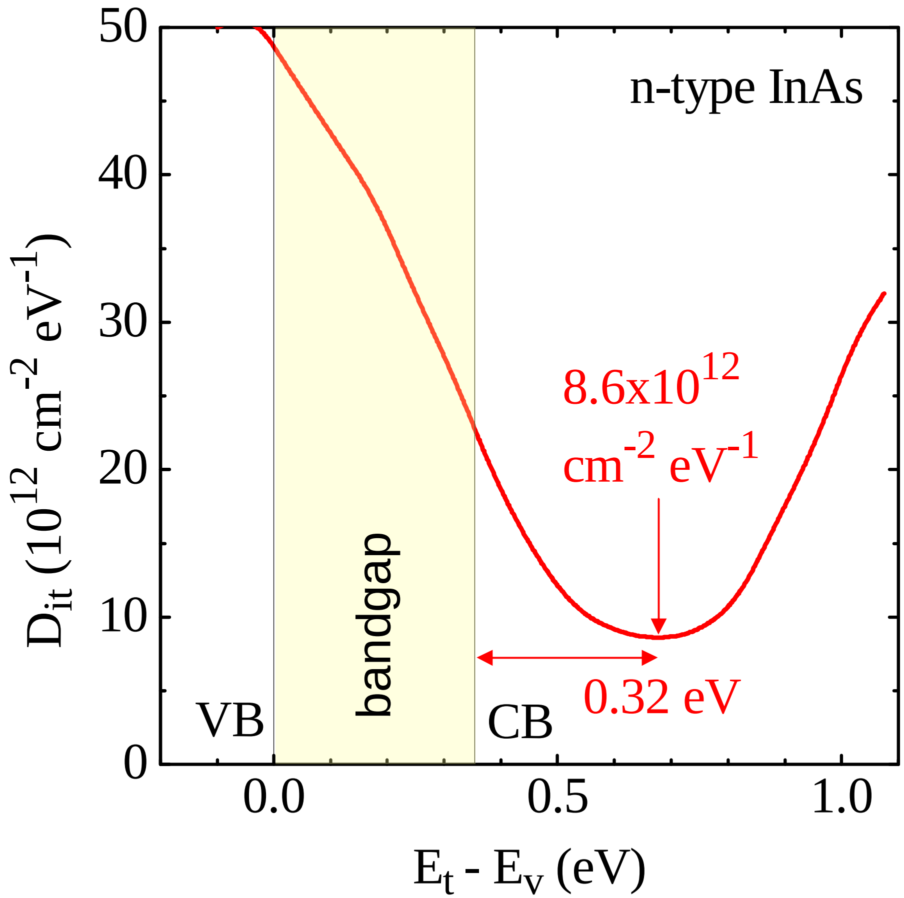

Final result: D_{it} distribution

- D_{it} obtained throughout the InAs band gap and inside CB
- D_{it} minimum has density of ≅ 10^{13} $cm^{-2}eV^{-1}$ at ≅ 0.3eV inside CB

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Conclusions and Acknowledgement: D_{it} Quantification on InAs

D_{it} minimum ≅ 10^{13} cm^{-2} eV^{-1} and is located at 0.3 eV above conduction band minimum

⇒ *Inadequate for devices*

Virtually all frequency dispersion originates from traps

⇒ *Many traps have very small (≤ 10^{-18} cm^2) effective capture cross section*

⇒ *this points toward border traps or oxide bulk traps*

⇒ *abruptness of interface is likely major issues*

Inversion carriers (holes) of noticeable density are absent

⇒ *Inversion carrier response time becomes a moot point*

Acknowledgement

- *Georgios Vellianitis: C-V measurement*
- *Gerben Doornbos: C-V and D_{it} modeling*

Further Reading

TSMC Property

E. H. Nicollian and J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology. New York: Wiley, 1982.

M. Passlack, M. Hong, E.F. Schubert, G.J. Zydzik, J.P. Mannaerts, W.S. Hobson, and T.D. Harris, "Advancing metal-oxide semiconductor theory: Steady-state nonequilibrium conditions," J. Appl. Phys., vol. 81, no.11. pp. 7647-7661, 1997.

G. Brammertz, H.-C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, "On the interface state density at $In_{0.53}Ga_{0.47}As$/oxide interfaces," Appl. Phys. Lett. vol. 95, pp. 202109, 2009.

E. Lind, Yann-Michel Niquet, Hector Mera, and Lars-Erik Wernersson, "Accumulation capacitance of narrow band gap metal-oxide-semiconductor capacitors," Appl. Phys. Lett. vol. 96, pp. 233507, 2010.

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Quiz Solution

Trap (D_{it}) Analysis Using Recombination

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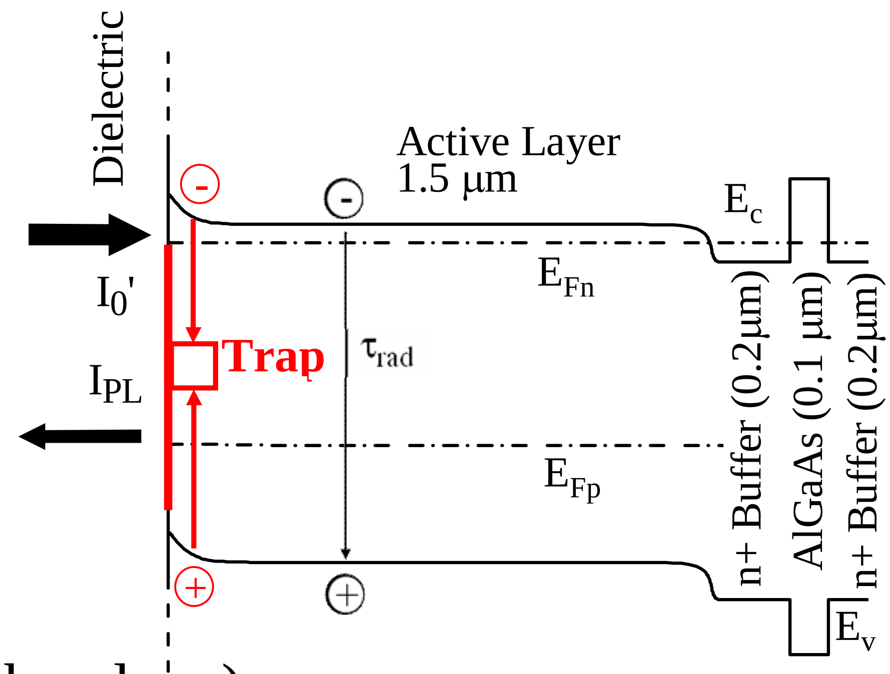
Laser Excitation of Intensity I_0

Photoluminescence of Intensity I_{PL}



$\eta = I_{PL}/I_0 \Rightarrow$
N_{it} (D_{it} integrated over bandgap)

Carrier Lifetime $\tau_{n/p} = 1/(\sigma\, v_{th} N_{it}) \neq f(E_T, n_i)$

Unique Tool to Screen Interfaces for Device Quality

Trap (D_{it}) Analysis Using Recombination

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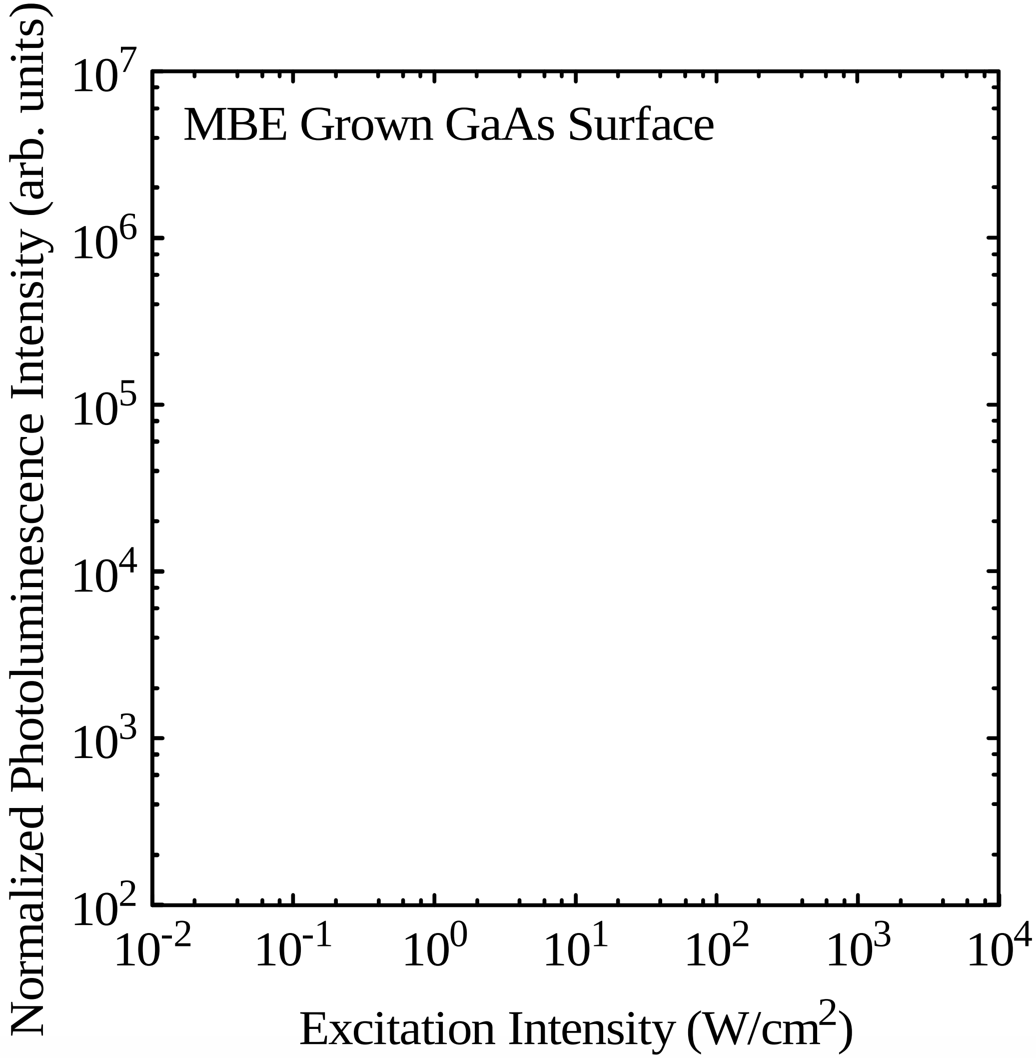

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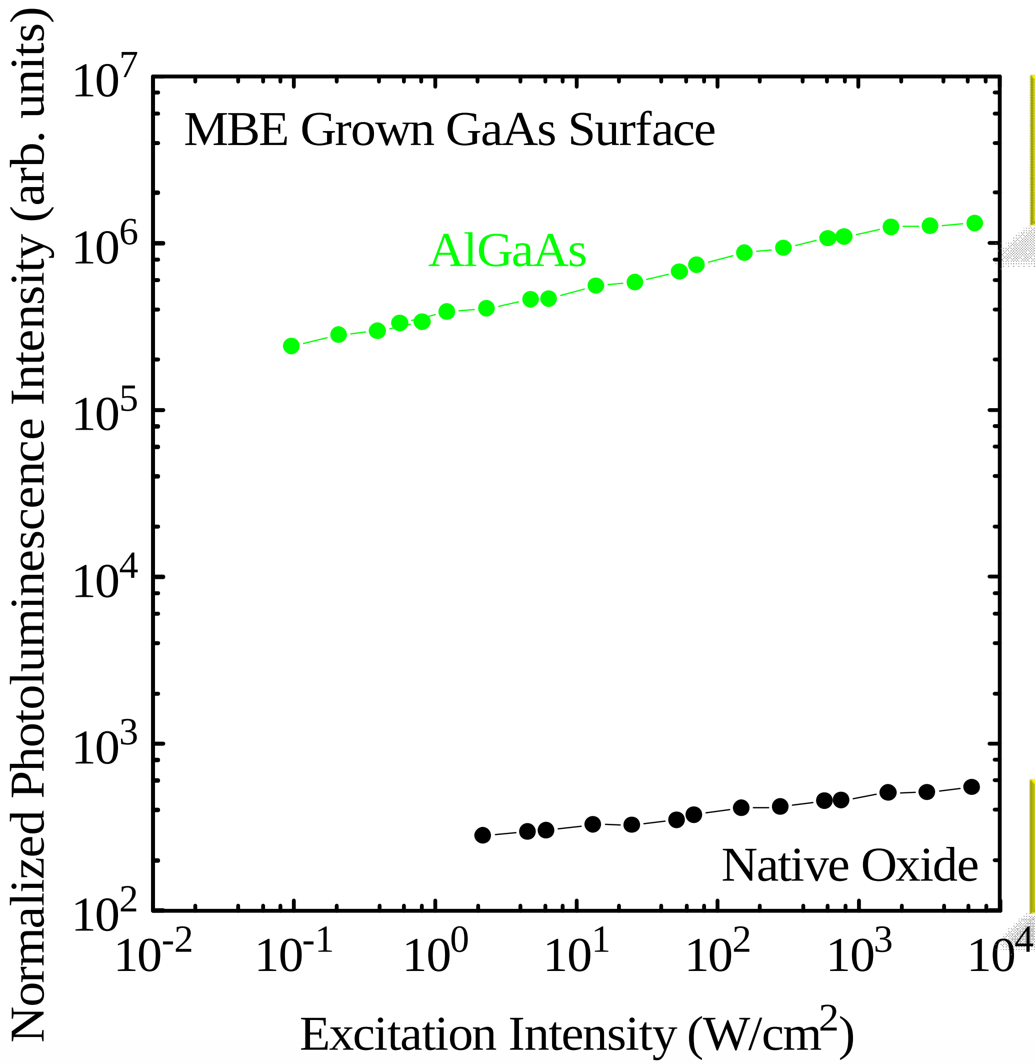

Known Best Interface: AlGaAs/GaAs

Known Worst Interface: Native Oxide/GaAs

Trap (D_{it}) Analysis Using Recombination

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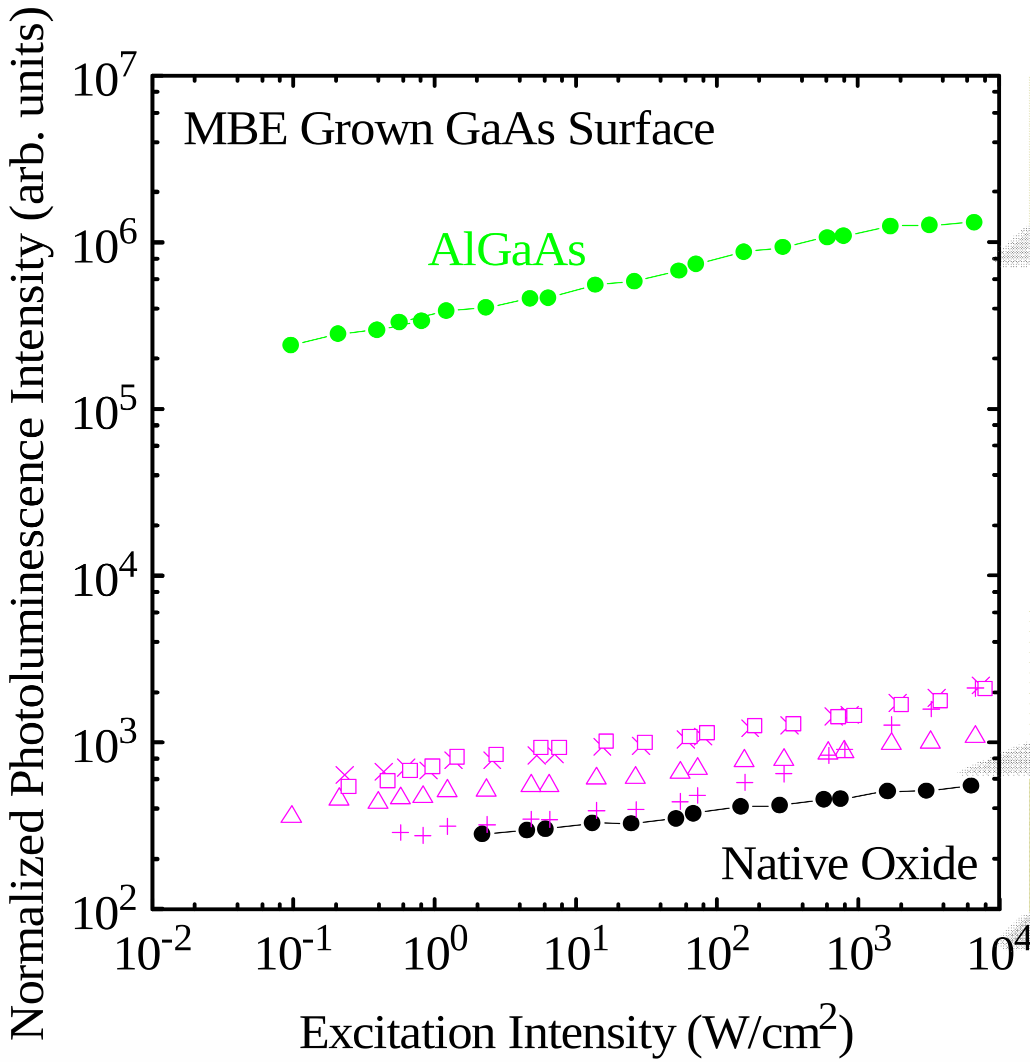

Known Best Interface: AlGaAs/GaAs

Oxides, Nitrides on GaAs: Native Oxide Behavior

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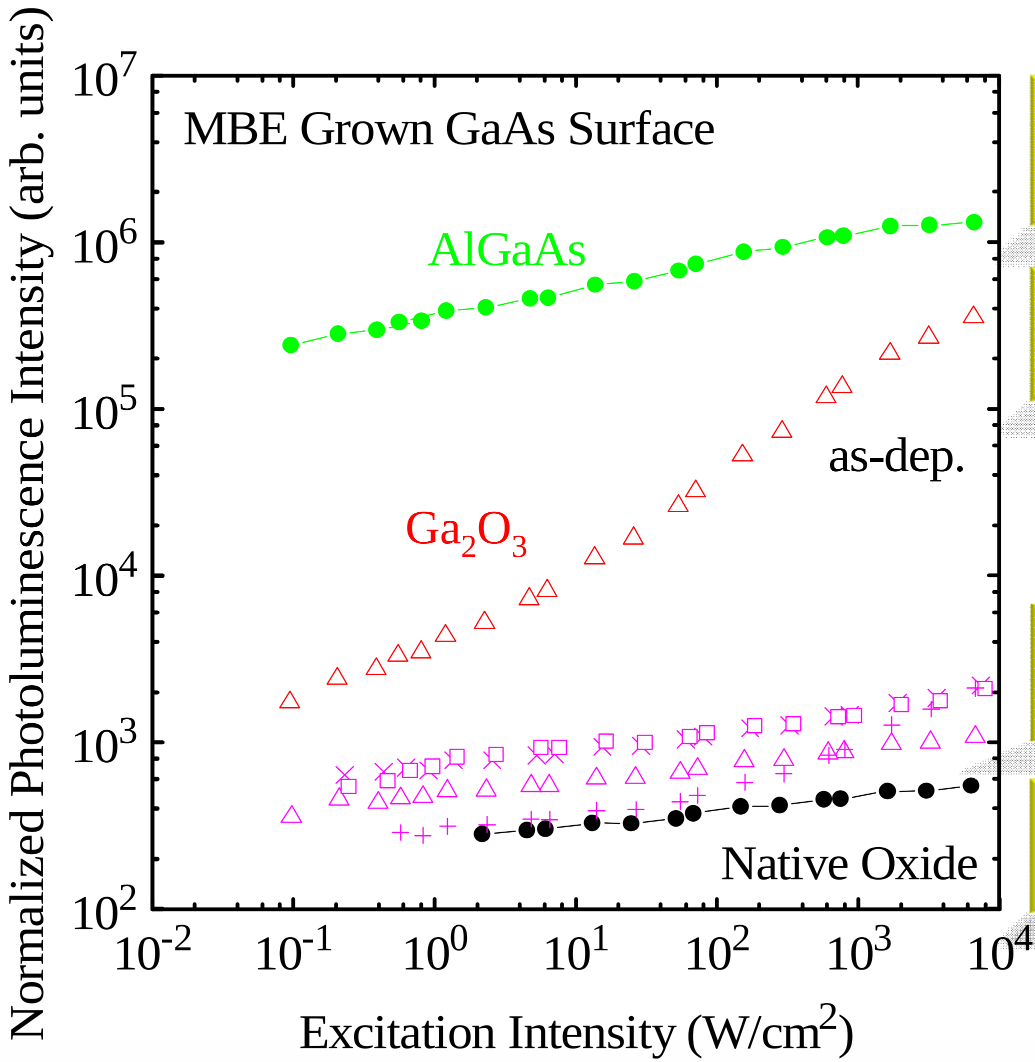

Known Best Interface: AlGaAs/GaAs

Device Quality Interface: Ga_2O_3/GaAs

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Trap (D_{it}) Analysis Using Recombination

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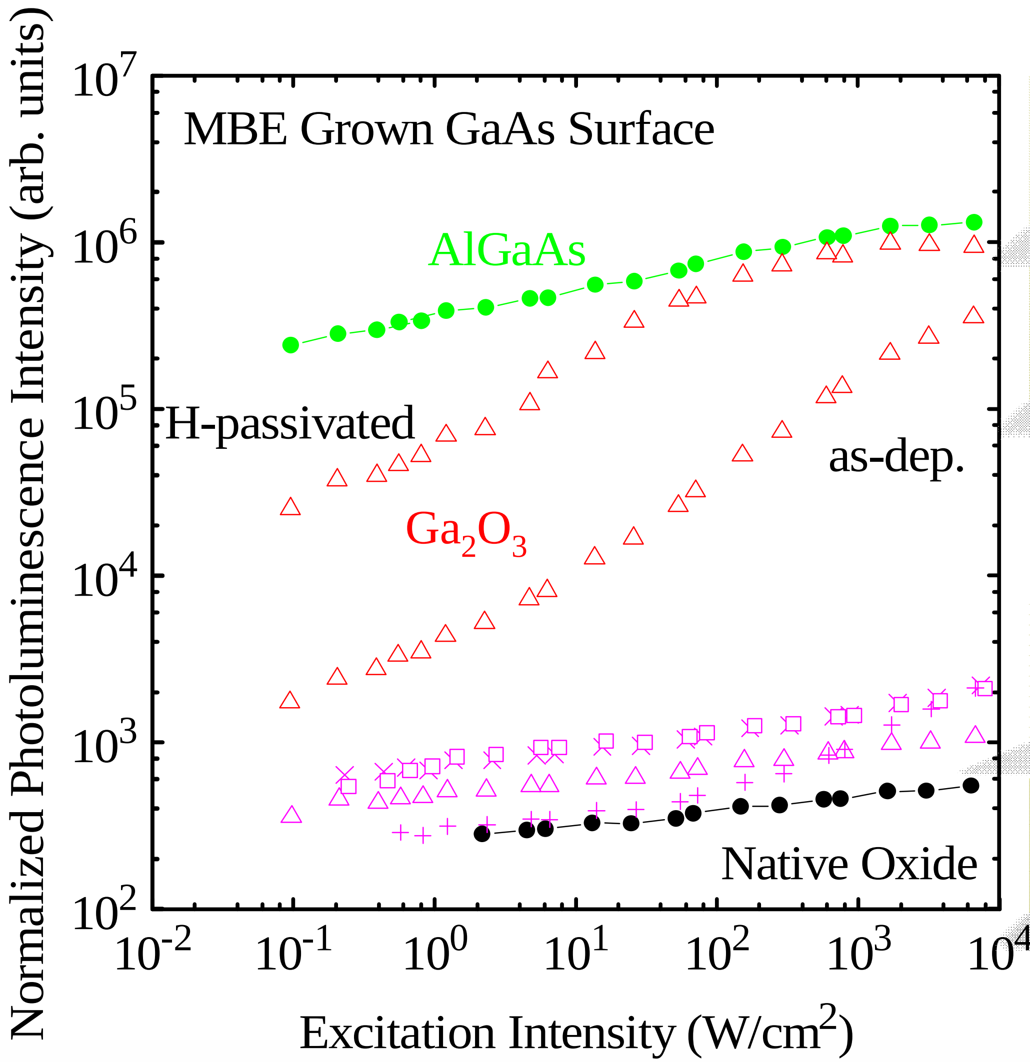

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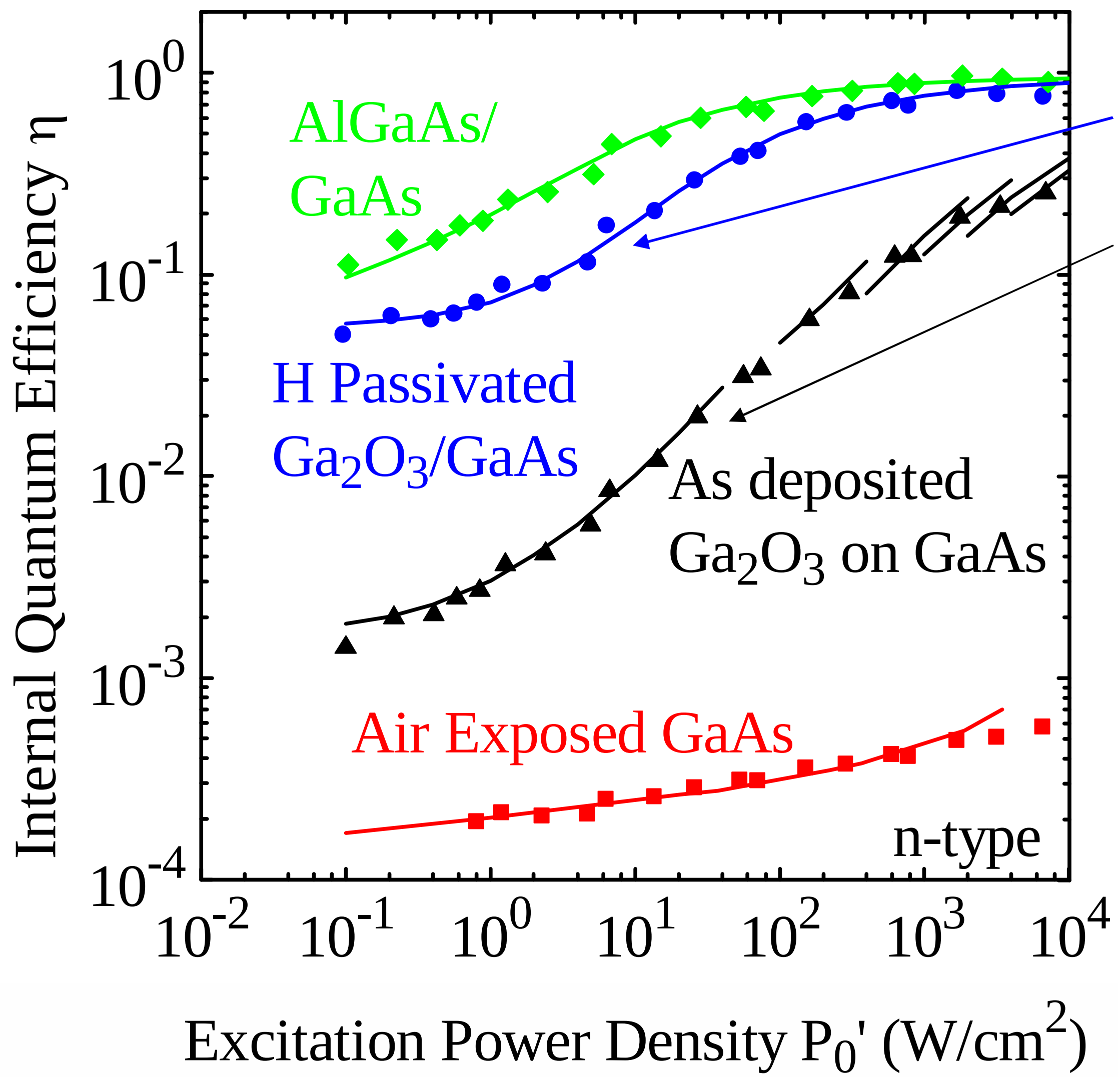

Midgap D_{it} =

1.1×10^{11} cm^{-2} eV^{-1}

2.7×10^{11} cm^{-2} eV^{-1}

Symbols: Measured

Lines: Simulated (1d numerical drift-diffusion, also provides S and σ)

Further Reading

TSMC Property

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M. Passlack, R. Droopad, P. Fejes, and L. Wang, "Electrical Properties of Ga_2O_3/GaAs Interfaces and GdGaO Dielectrics in GaAs Based MOSFETs," IEEE Electron. Dev. Lett., vol. 30, no. 1, pp. 2 - 4, 2009.

TSMC Property

Nonsilicon Interfaces - Outline

Introduction to Nonsilicon Channel Materials

Quiz: Do You Understand Nonsilicon Interface Data?

Interface State Analysis

- *Introduction*
- *Admittance-voltage (capture/emission):*
    - *Flow chart for trap evaluation*
    - *Example D_{it} quantification*
- *Photoluminescence intensity (recombination)*

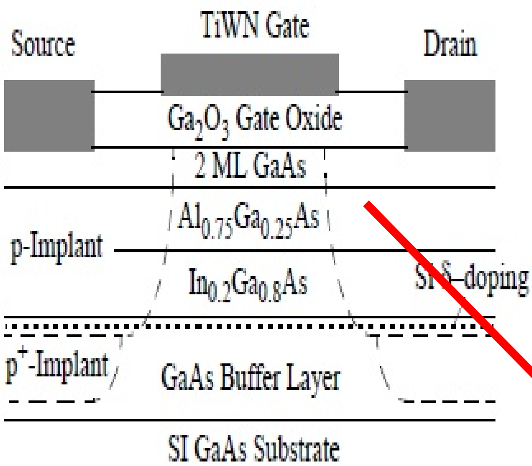
D_{it} and Heterostructures in MOSFETs

- *Heterostructure barrier layer: Introduction*
- *Shifting D_{it} distribution in energy space*
- *D_{it} amplification or reduction – Barrier layer case studies*

Quiz Solution

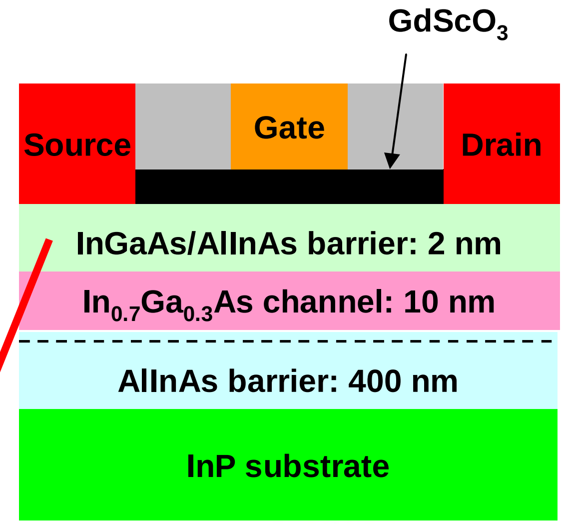
D_{it} and Heterostructures in Quantum Well MOSFETs (QWFET)

TSMC Property

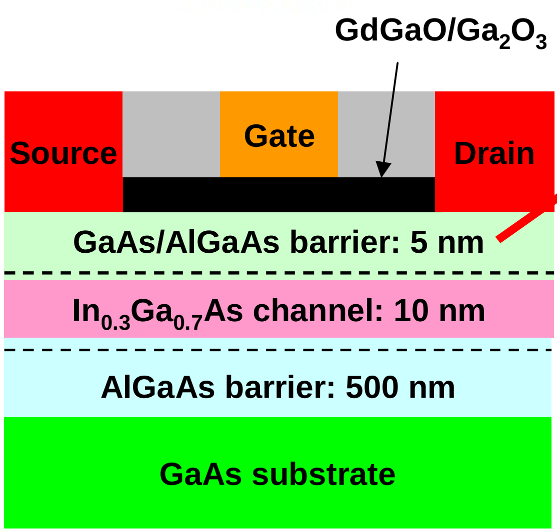


Passlack et al., IEEE EDL vol. 23, 2002, pp. 508

Hill et al., Electronics Letters vol. 44, 2008, pp. 498, pp. 1283



Heterostructure Barrier Layer



Hill et al., IEEE EDL vol. 28, 2007, pp. 1080

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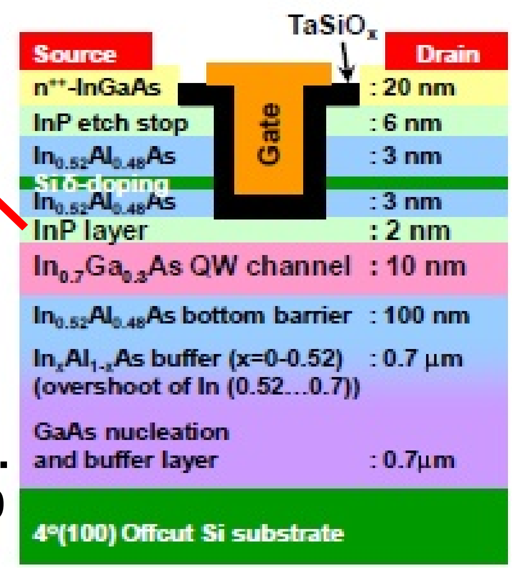


Heterostructure Barrier Layer: Introduction

Alter surface chemistry and interface bonding

- *Lower D_{it}*
- *More favorable D_{it} distribution*

Shift a given D_{it} vs E distribution with respect to channel charge

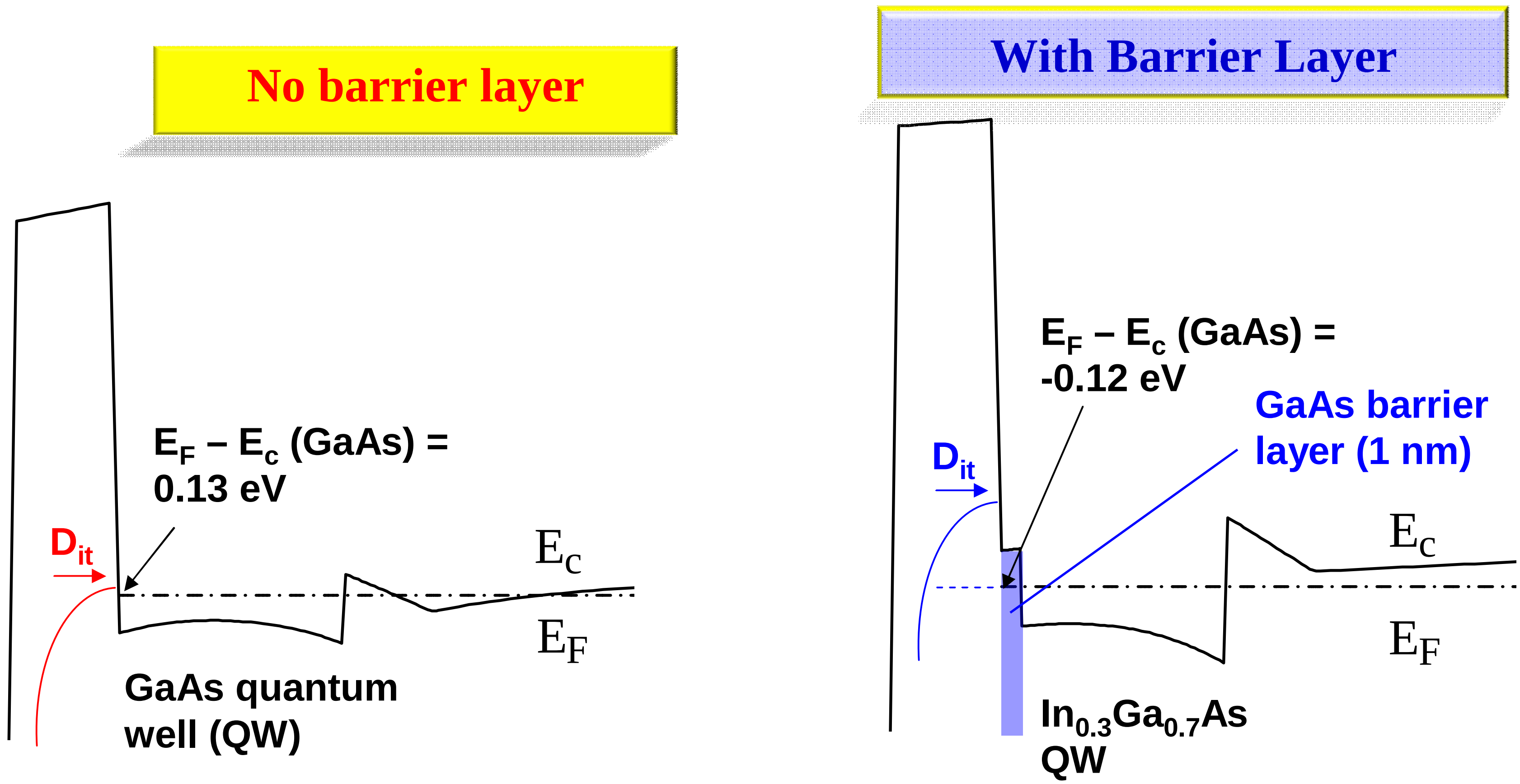
- *Avoid branch of high/rising D_{it}, e.g. close to a band edge*

Optimization considerations (electrostatics only)

- *EOT*
- *Effective D_{it}*
- *Leakage current*

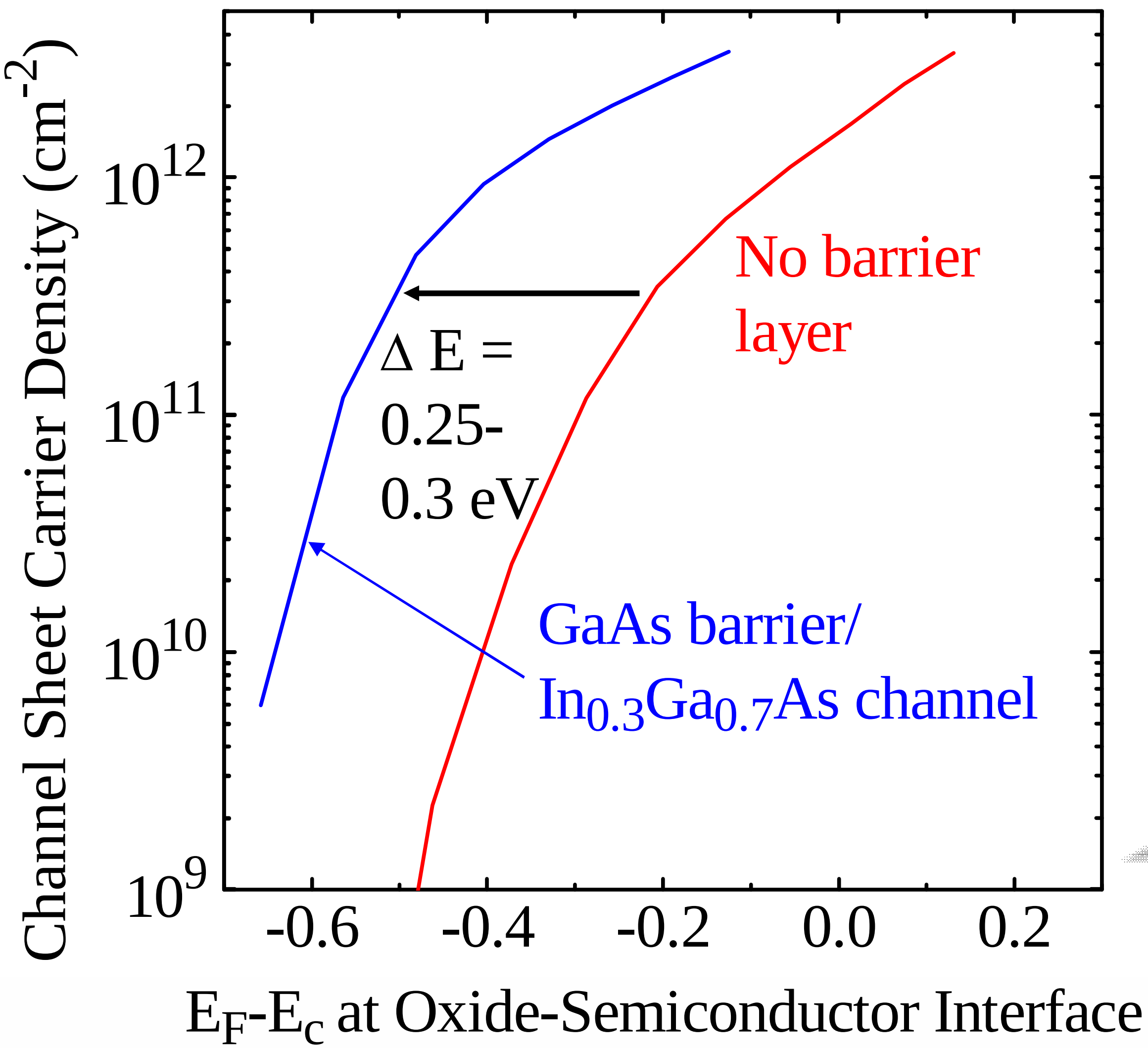
Shift of D_{it} vs E with respect to Channel Charge

TSMC Property



Fermi level position at dielectric-GaAs interface differs by 0.25 eV for identical QW sheet charge density: $n_s = 3.4\times10^{12}$ cm^{-2}

Shift of D_{it} vs E with respect to Channel Charge

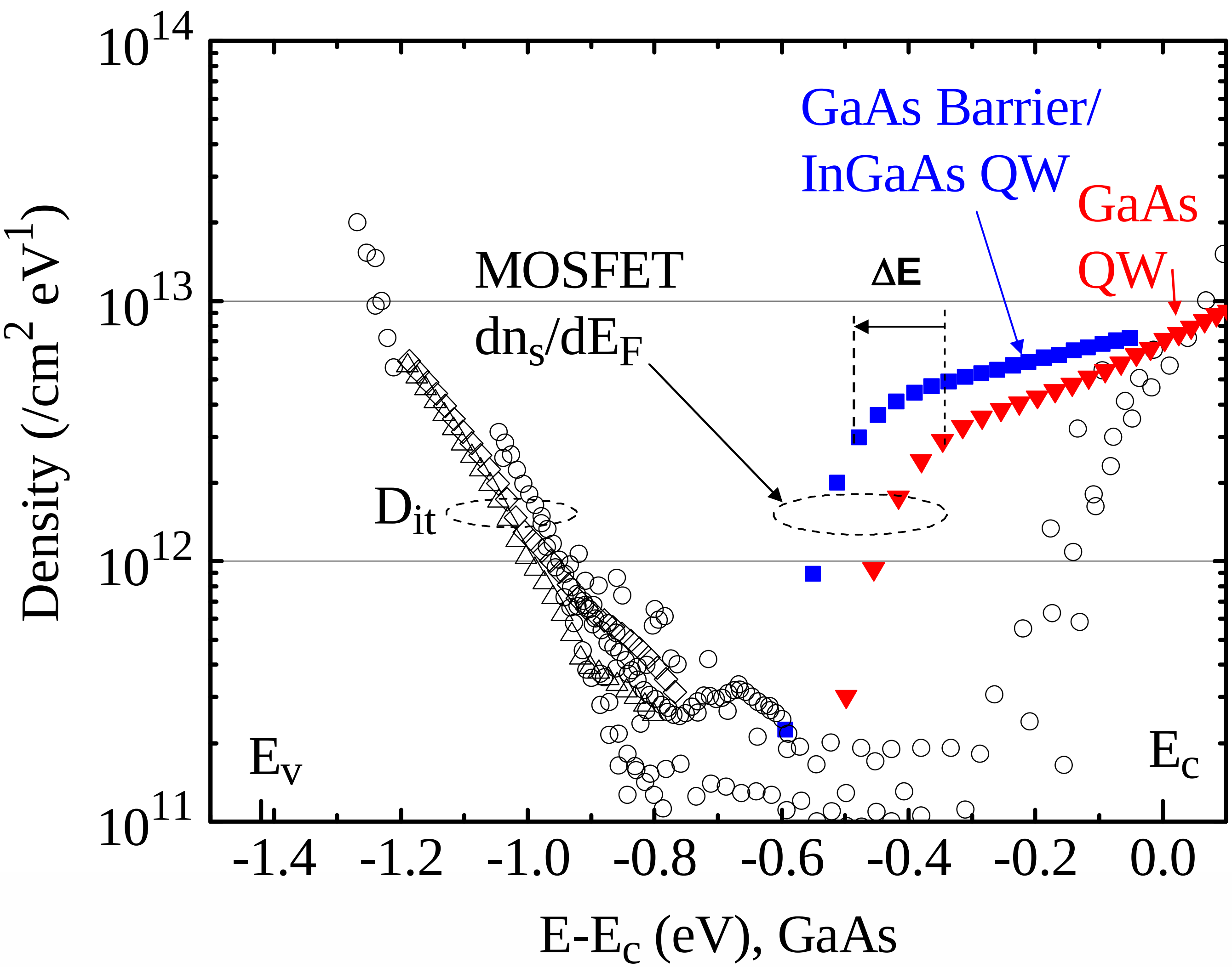


D_{it} distribution shifted along energy axis by 0.25-0.3 eV for identical channel charge n_s

Model & Simulations

Shift of D_{it} vs E with respect to Channel Charge

TSMC Property



Manufactured Devices (GaAs QWFET)

Heterostructure Barrier Layer: Case Studies

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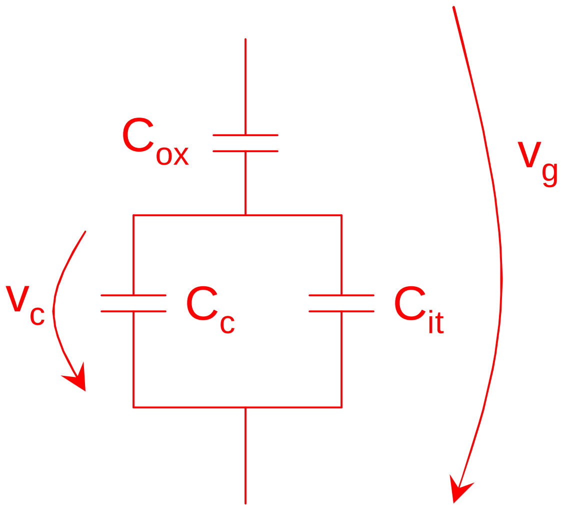
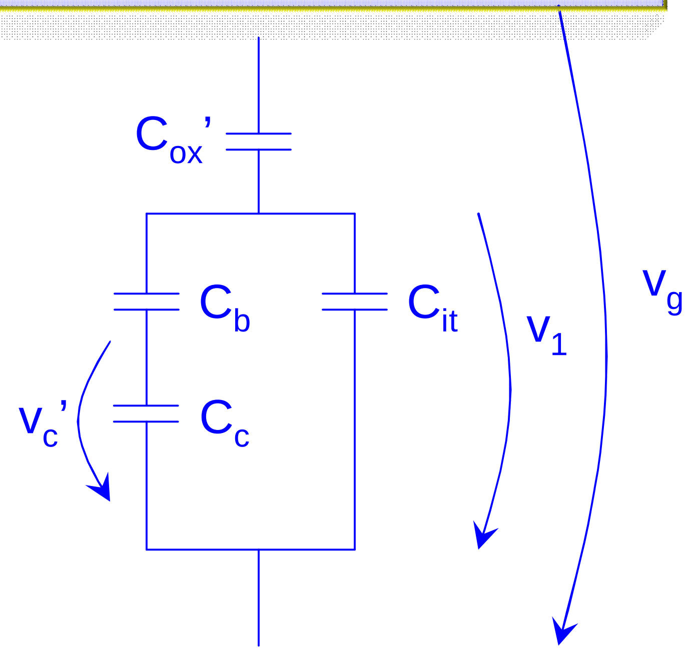
No barrier layer



C_{ox}: oxide capacitance
C_c: channel capacitance
C_{it}: D_{it} capacitance
v_g: gate voltage
v_c: channel voltage

With Barrier Layer



C_{ox}': oxide capacitance
C_c: channel capacitance
C_b: barrier layer capacitance
C_{it}: D_{it} capacitance
v_g: gate voltage
v_c': channel voltage

A: Barrier Layer Case Study with $C_{ox}' = C_{ox}$

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No barrier layer

$$\frac{v_c}{v_g} = \frac{C_{ox}}{C_c + C_{it} + C_{ox}}$$

↓

Lower modulation efficiency v_c'/v_g for barrier layer case (D_{it} amplification and EOT increase)

With Barrier Layer

$$\frac{v_1}{v_g} = \frac{C_{ox}}{\frac{C_b C_c}{C_b + C_c} + C_{it} + C_{ox}}$$

$$\frac{v_c'}{v_1} = \frac{C_b}{C_b + C_c}$$

$$\frac{v_c'}{v_g} = \frac{C_{ox}}{C_c + \frac{C_b + C_c}{C_b} C_{it} + \frac{C_b + C_c}{C_b} C_{ox}}$$

D_{it} amplification (> 1) Increase in EOT

Radosavljevic et al.: 1.8
Hill et al.: 2.8

B: Barrier Layer Case Study with Identical EOT

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C_{ox} [C_{ox}' / C_b]

$C_{ox}' \rightarrow \infty$, $C_b = C_{ox}$ (Schottky gate)

$C_b >> C_{ox}$ (no barrier layer)

$$C_{ox}' = \frac{C_b C_{ox}}{C_b - C_{ox}}$$

No barrier layer

$$\frac{v_c}{v_g} = \frac{C_{ox}}{C_c + C_{it} + C_{ox}}$$

With Barrier Layer

$$\frac{v_c'}{v_g} = \frac{C_{ox}}{C_c + \left[\frac{C_b + C_c}{C_b}\right]\left[\frac{C_b - C_{ox}}{C_b}\right] C_{it} + C_{ox}}$$

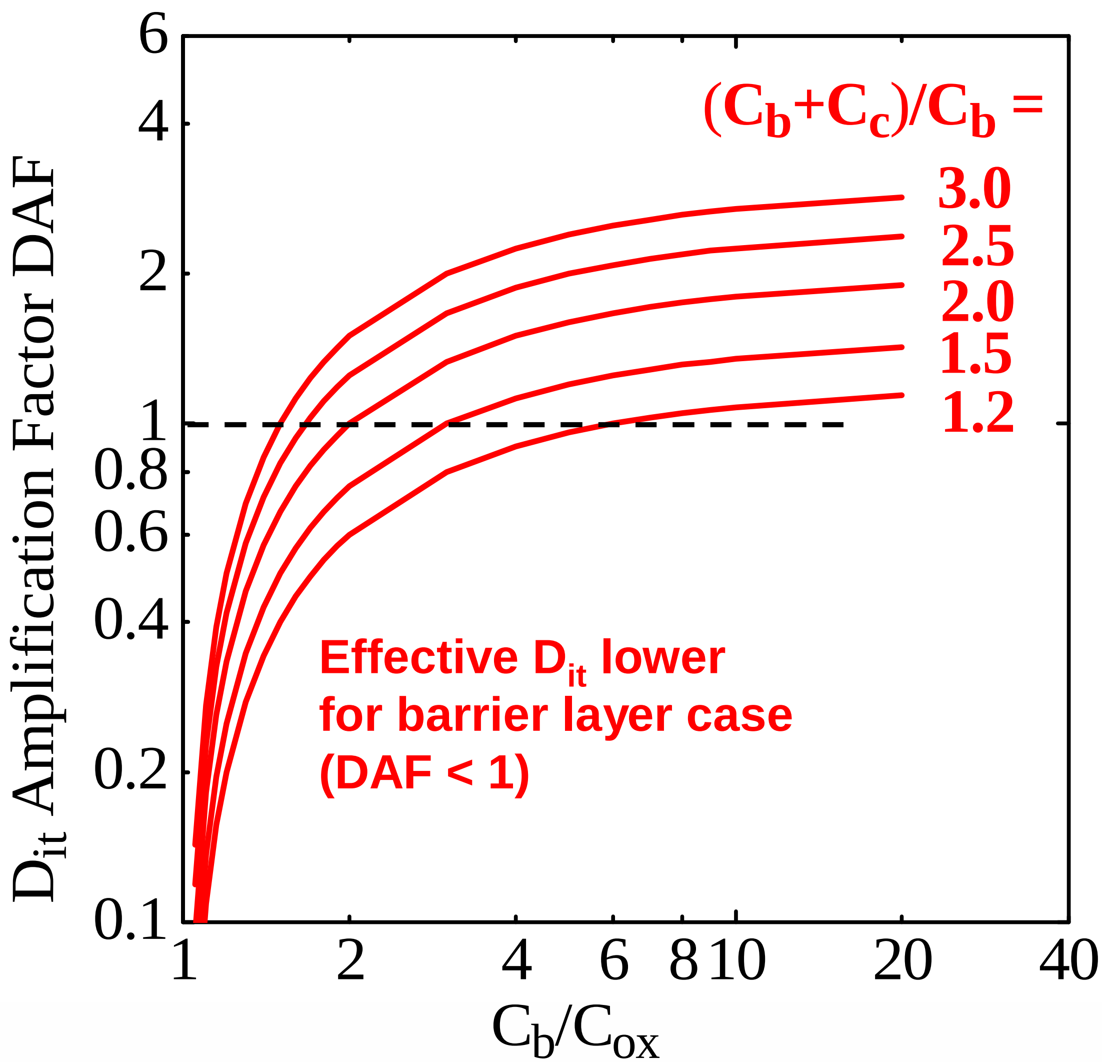
> 1

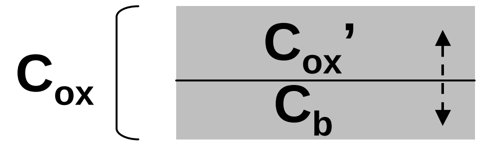
≤ 1
0 for $C_b = C_{ox}$
(Schottky gate limit)

D_{it} Amplification Factor DAF

Higher modulation efficiency v_c'/v_g possible for barrier layer case but leakage current penalty

Barrier Layer Case Study: Identical EOT





$C_{ox}' \rightarrow \infty$, $C_b = C_{ox}$
(Schottky gate)

C_{ox}: oxide capacitance without barrier layer
C_{ox}': oxide capacitance with barrier layer
C_b: barrier layer capacitance

Further Reading

M. Passlack, J. Abrokwah, and Z. Yu, "Self-aligned metal-oxide-compound semiconductor devices and methods of fabrication," US Patent 5,945,718, August 31,1999.

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