43rd IEEE Semiconductor Interface Specialists Conference

Resistive switching materials and devices for future memory applications

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Tutorial SISC San Diego, 5 December 2012

Outline

Need for new Non Volatile Memory?

Materials ⇨ RRAM : Classification

RRAM : Memory Structure

Device ⇨ Resistive Switching Behavior

RRAM: Status

Outline

Need for new Non Volatile Memory?

Materials → RRAM : Classification

RRAM : Memory Structure

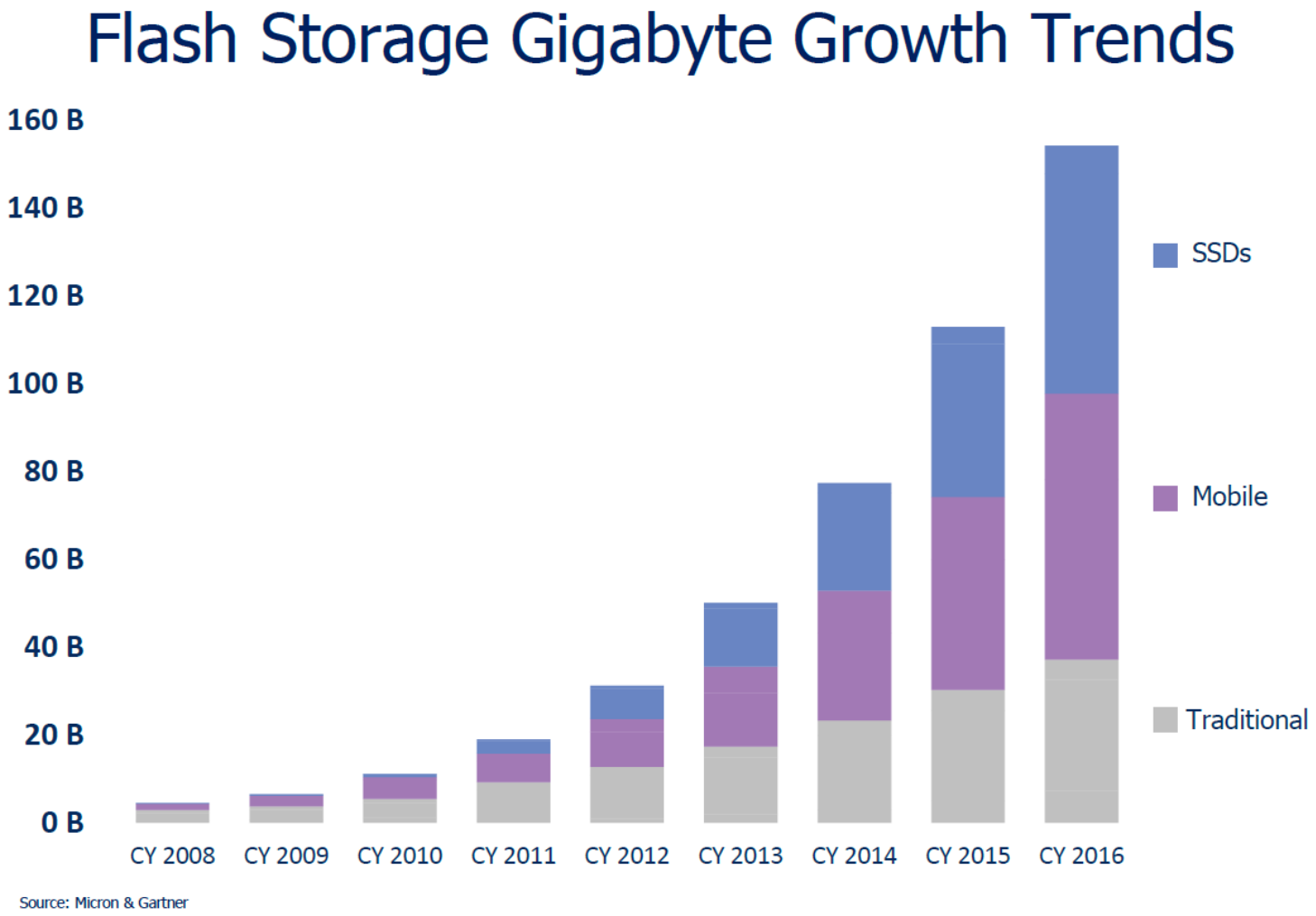
Device → Resistive Switching Behavior

RRAM: Status

Need for new Non-Volatile Memory ?

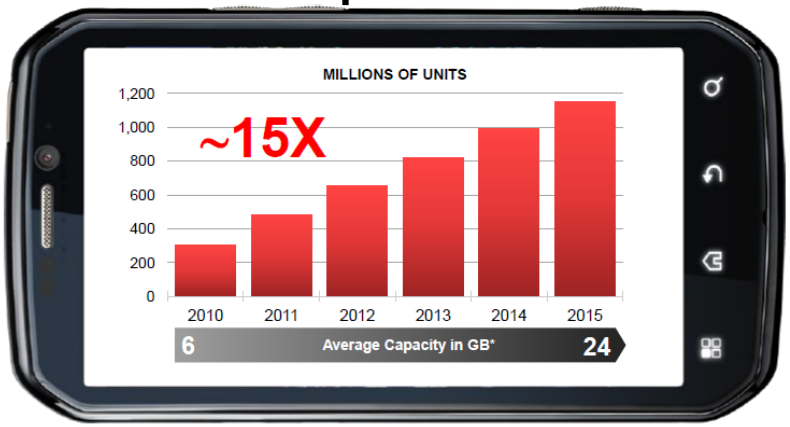
- Growing NVM market
- Flash scaling issues
- New opportunities?

NVM market is growing exponentially

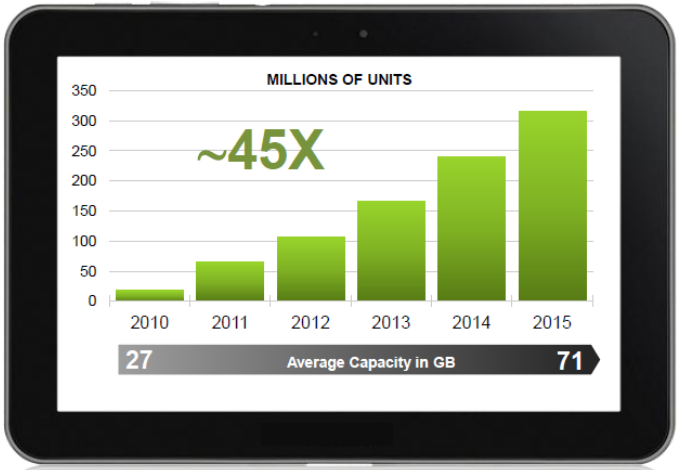


NVM Growth drivers

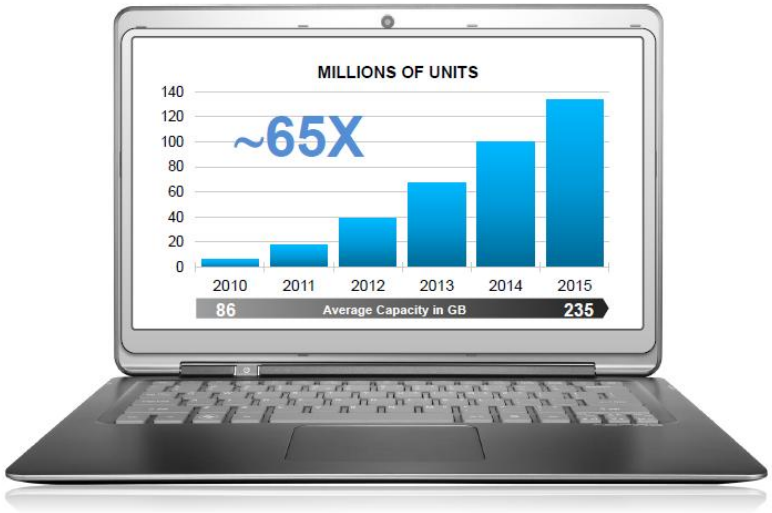
Smartphones



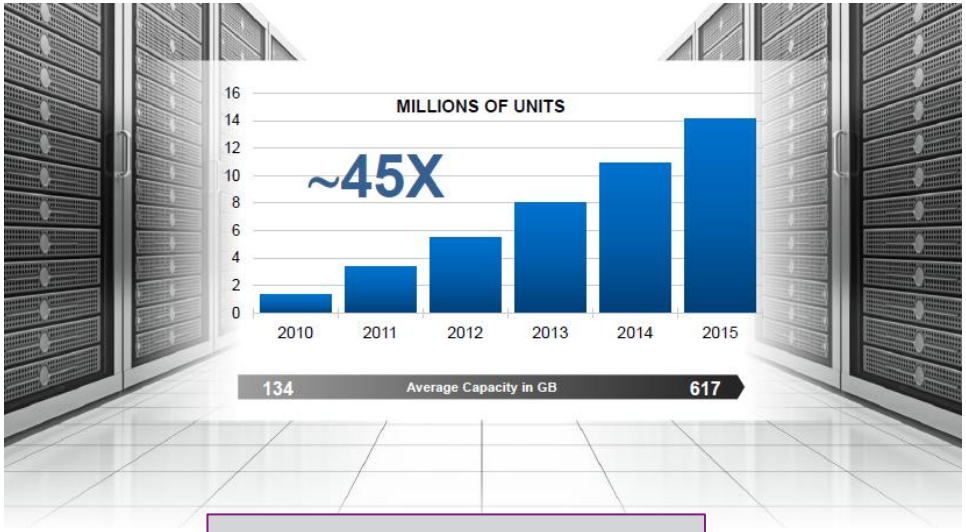
Tablets



PC SSD



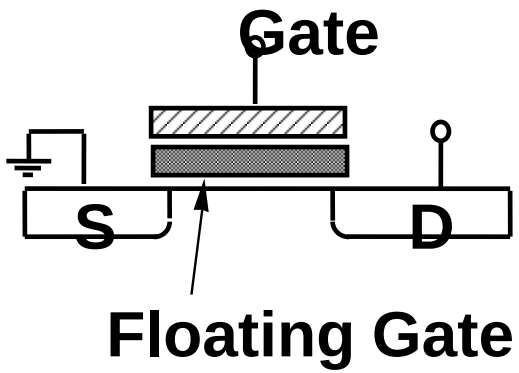
Enterprise SSD

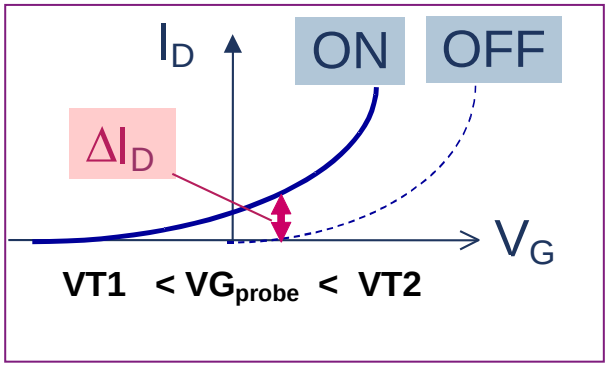


Slide courtesy G.Jurczak, imec

Main Non-Volatile Memory = FLASH

- Operation based on floating gate transistor

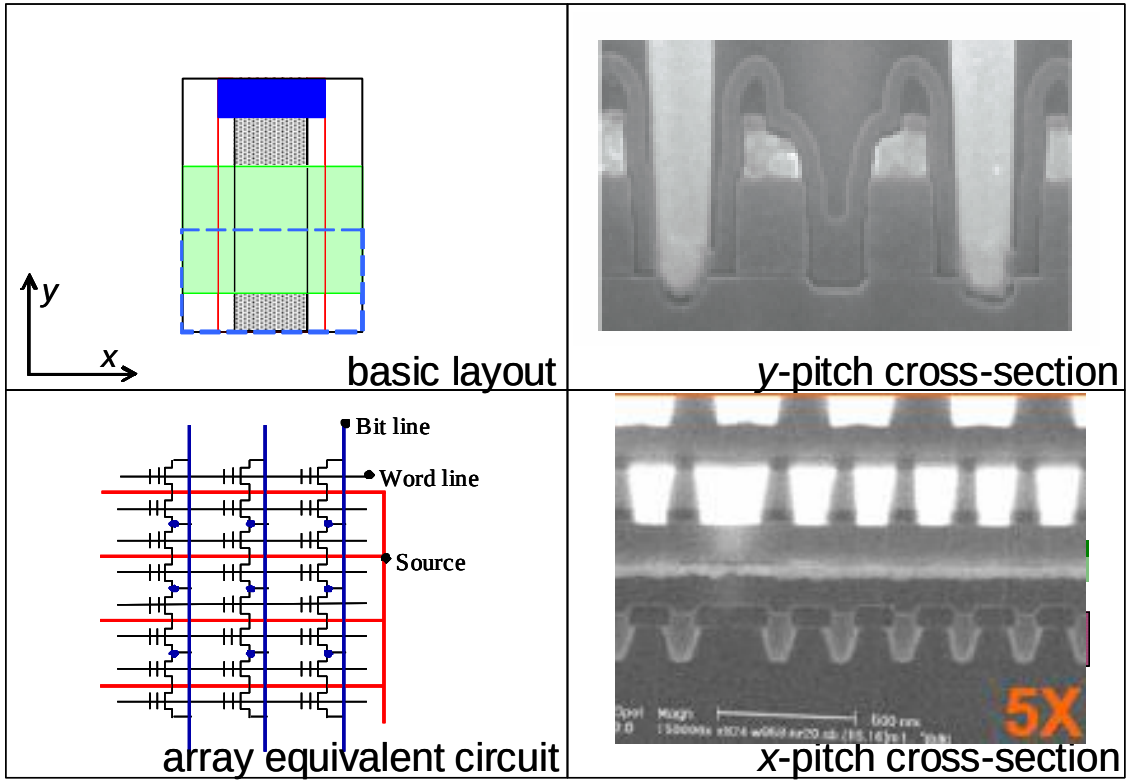


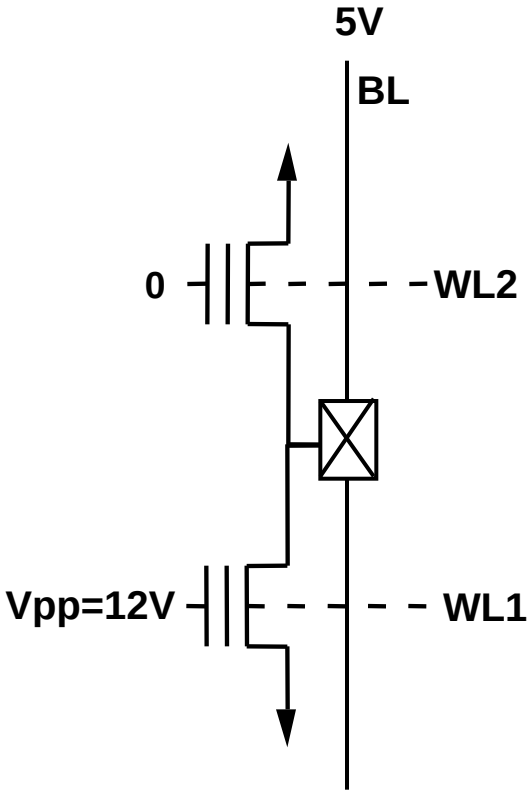


  - threshold voltage is shifted by putting (**PROGRAM**) or removing (**ERASE**) charge from the floating gate (by *hot carrier injection* or *tunneling*)
  - **READ-OUT** by selecting element and current sensing
  - mainstream nonvolatile memory technology of today due to high CMOS compatibility and high quality of silicon dioxide
- NOR and NAND type

Cell configurations : NOR

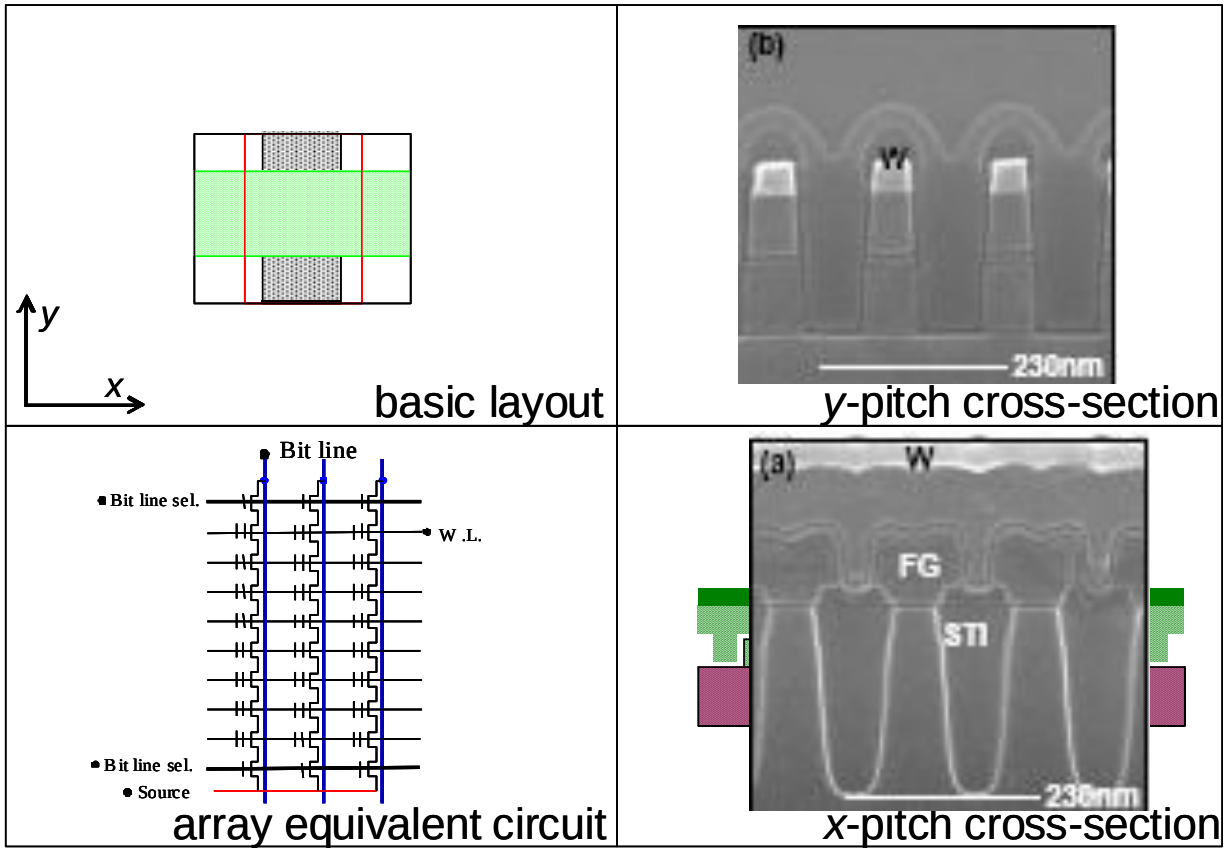
- NOR : ½ drain (BL) contact/cell
  - fast random access, fast programming, robust → **code** (Cellular)
  - Larger cell size ~10F²

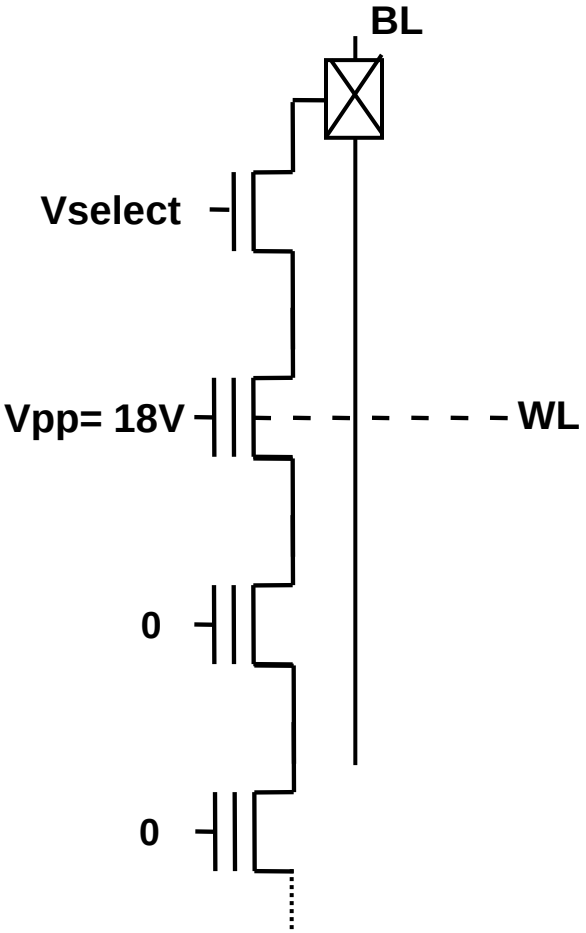




Cell configurations : NAND

- NAND : contactless:
  - slow access (but fast burst read), low program power → **data**
  - Smallest cell size : ~4F^2

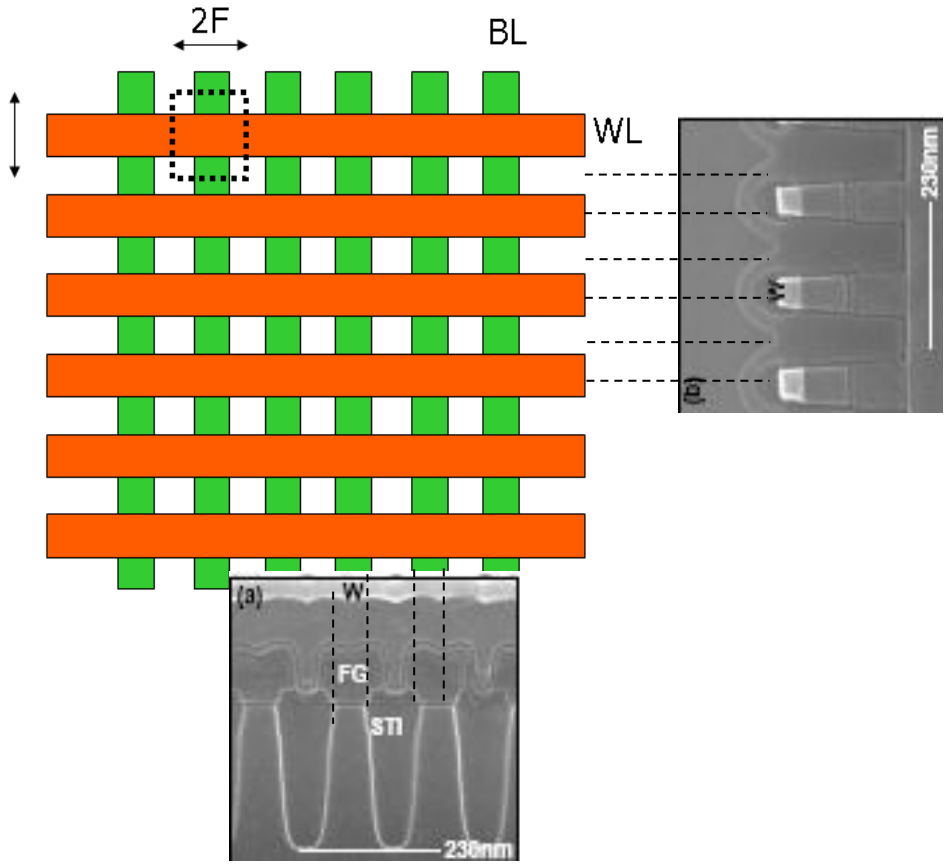




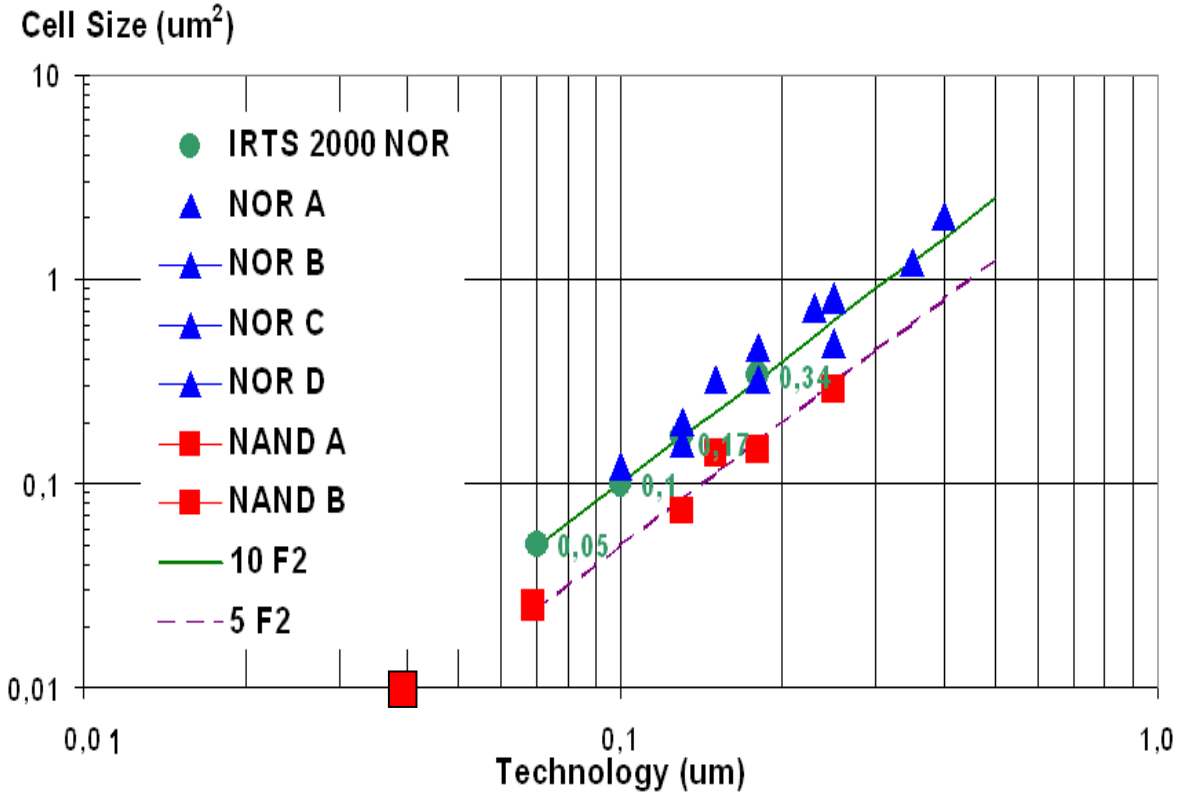
NAND = minimal cell size memory !!!

NAND Flash is TRUE Cross-Point (XP) memory !

Cell size = $4F^2$

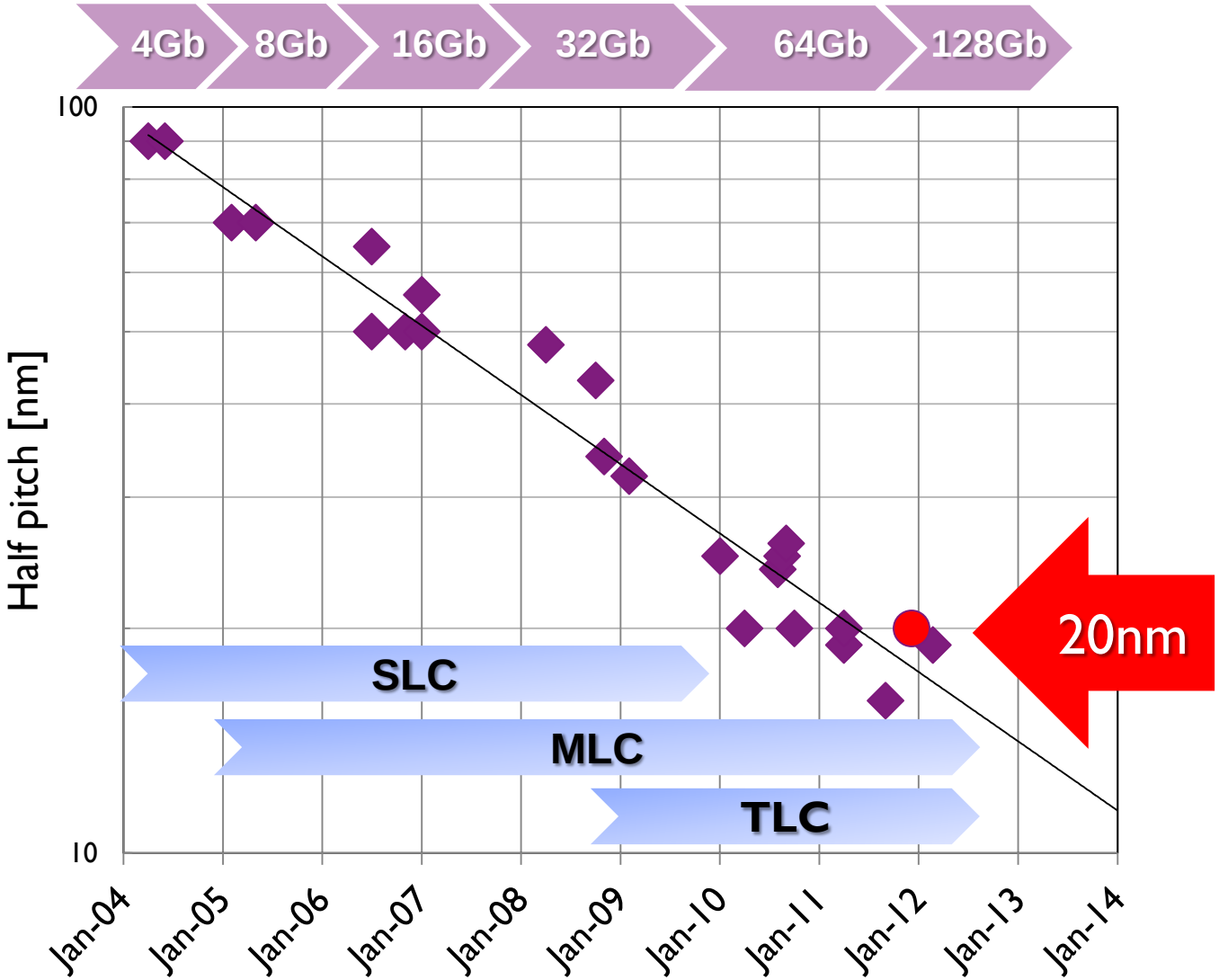


Success of FLASH = small 1T cell & scalability



From IMST Whitebook 2007

FLASH scaling trends and limits

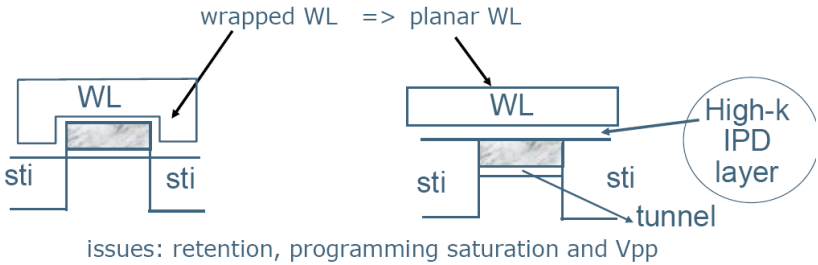


Slide courtesy G.Jurczak, imec

NAND Flash scaling issues

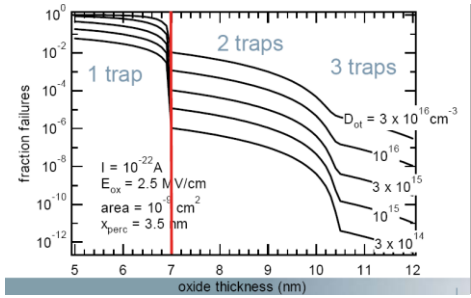
Scaling limitations

- Reduced FG coupling of scaled device

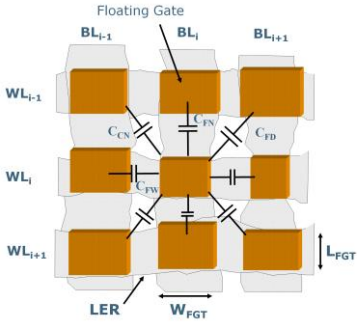


issues: retention, programming saturation and Vpp

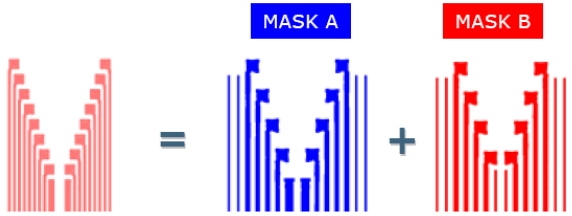
- Limit of tunnel ox scaling
  - No further voltage scaling



- Electrostatic interaction between neighboring cells



- Dense patterning requirements ahead of advanced litho
  - Dual patterning developments

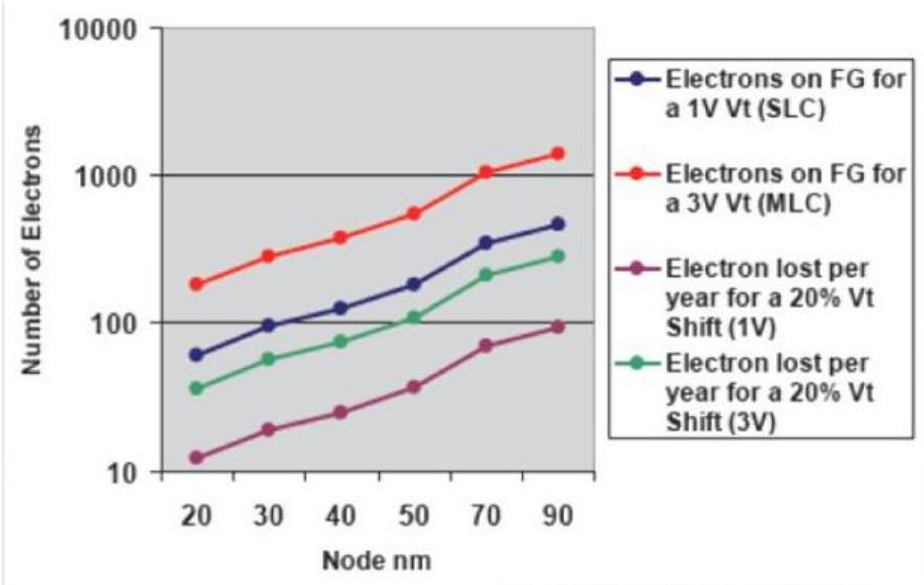


Charge = quantized !

Flash scalability based on **charge density** <> total charge DRAM

Hower, ultimately charge is made up from **electrons**...

- At 20nm, less than 100 electrons are present on the FG for Vt=1
- If 20% charge loss is the spec, we talk about ~10 electrons…
- for 10 yrs retention, **I_{leak}<<1e/yr…**

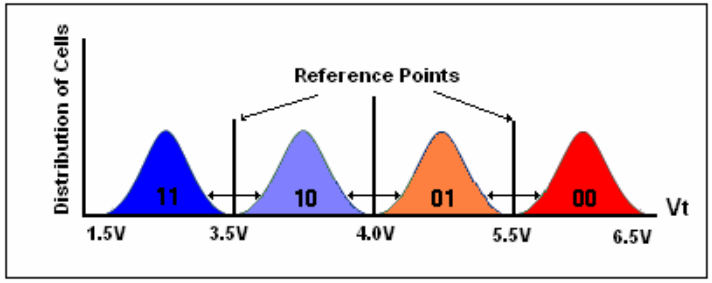


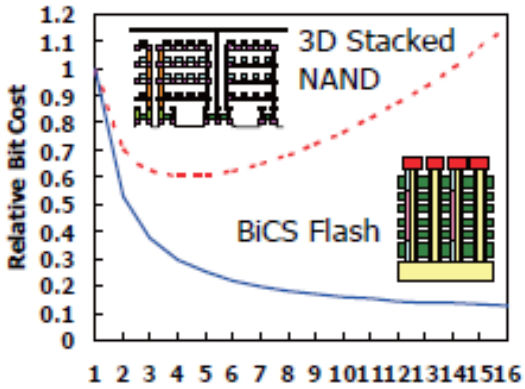
K.Prall, NVSMW, 2007

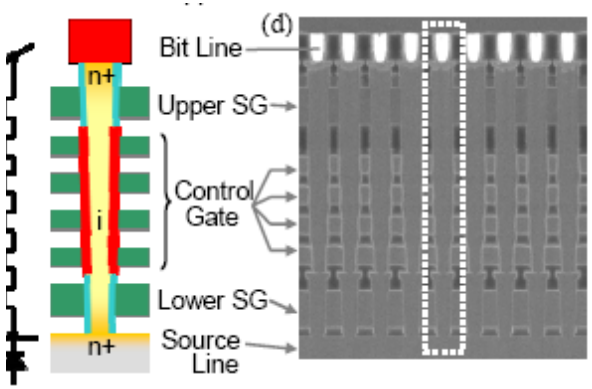
Scaling advantage of new **non-charge based** memories concepts ?

Flash explores other scaling routes

- **Multi-level programming**
  - 2-3-4 bits/cell
  - Currently implemented
- **Planar → 3D Flash**
  - Effective cell area : divided by number of layers!
  - Cost-effective integration to stack bits vertically
  - Different 3D concepts (BICS, TCAT, VSAT)
  - Not (yet) in production







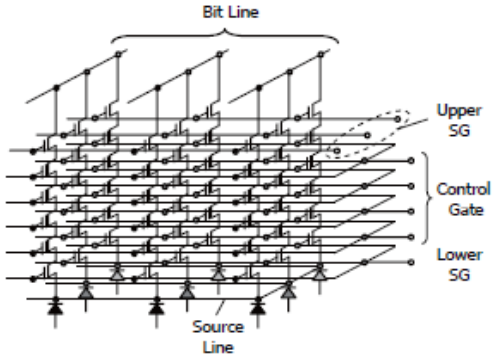
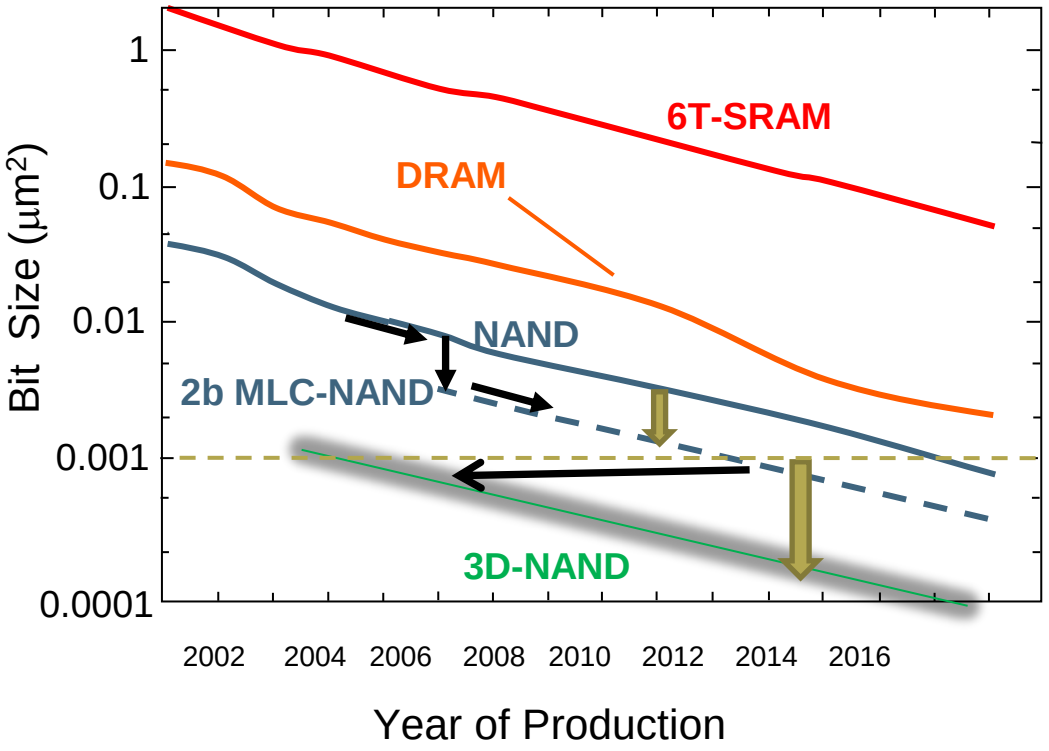


Fig. 4 Equivalent circuit of BiCS flash memory.

Bit Cost Scaling FLASH, Toshiba IEDM 2007

Flash BIT scaling

right metric
= **F^2/bit**

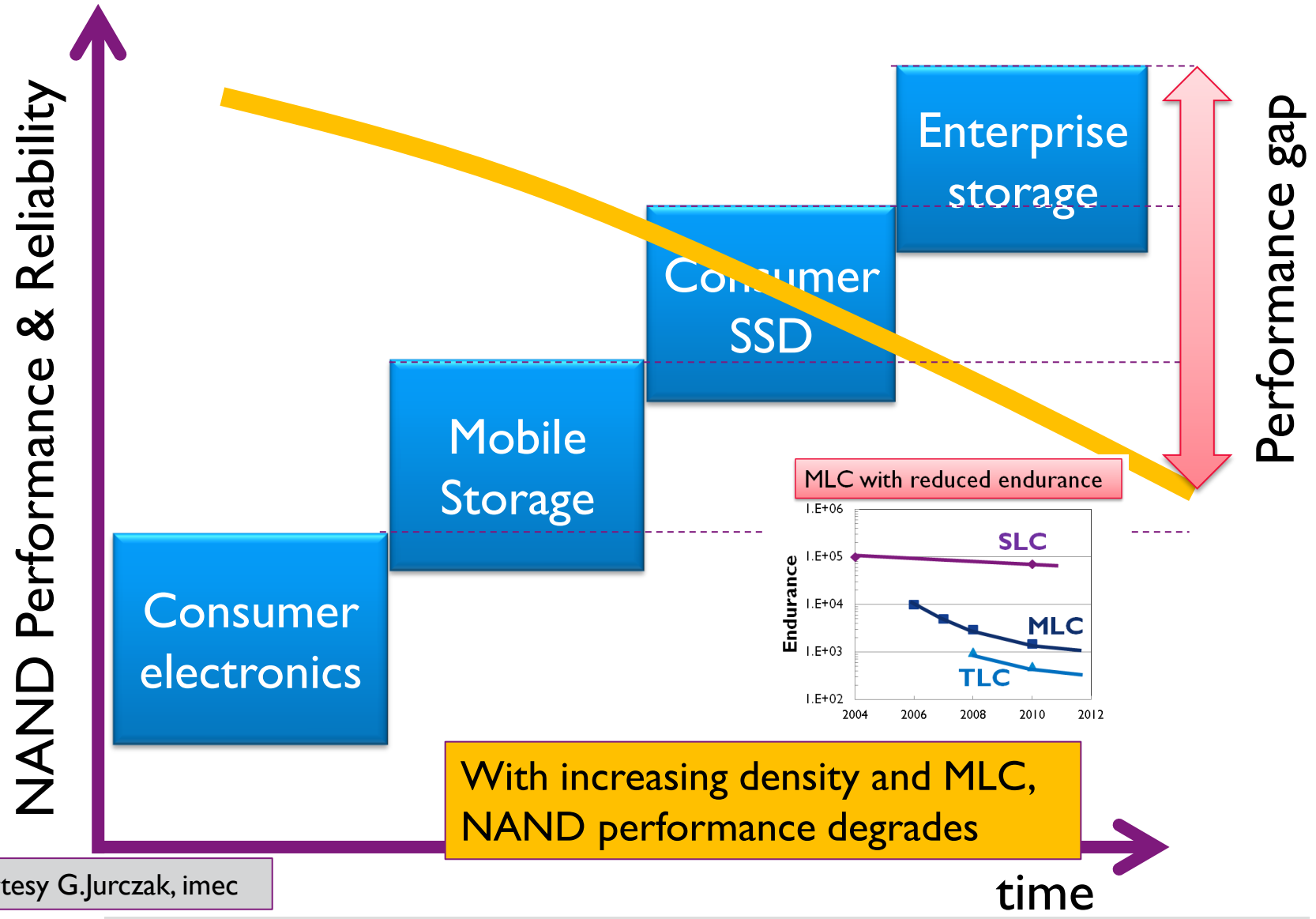


After H.E. Maes and J. Van Houdt, keynote @IEEE NVSMW 2003

Same bit size for larger node

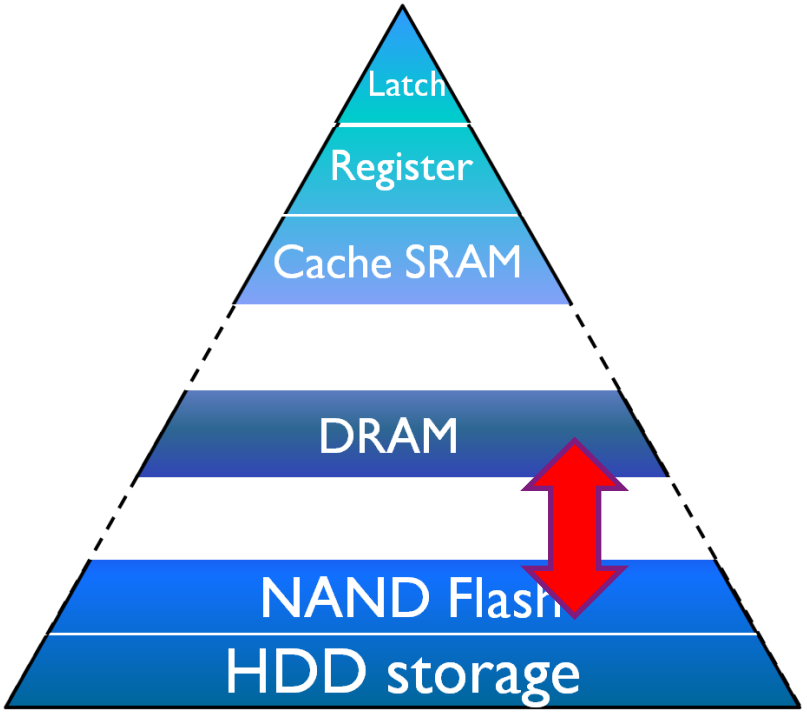
Any new technology competing with Flash should enable ***all*** scaling routes

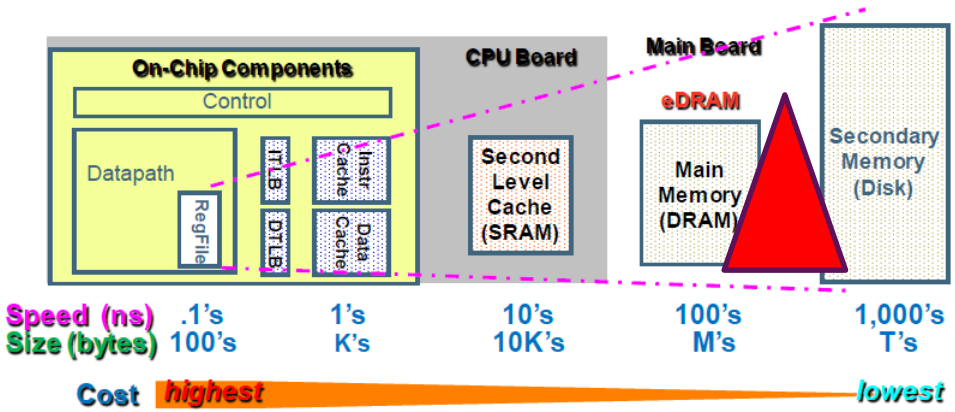
Performance degradation of scaled Flash



Slide courtesy G.Jurczak, imec

Latency GAP between DRAM and NAND





Opportunity for new class of (NV) memories :
Storage Class Memory (SCM)
~ "performant FLASH"

DIFFERENT CLASSES OF SCM

Storage type SCM : (close to HDD)

- **a high-performance solid-state drive**, accessed by the system I/O controller much like an HDD

Memory type SCM: (close to DRAM)

- should offer a **read/write latency of less than 1 µs**. These specifications would allow it to remain synchronous with a memory system, allowing direct connection from a memory controller and bypassing the inefficiencies of access through the I/O controller.

ERD ITRS meeting Potsdam 2011

Outline

Need for new Non Volatile Memory?

Materials → RRAM : Classification

RRAM : Memory Structure

Device → Resistive Switching Behavior

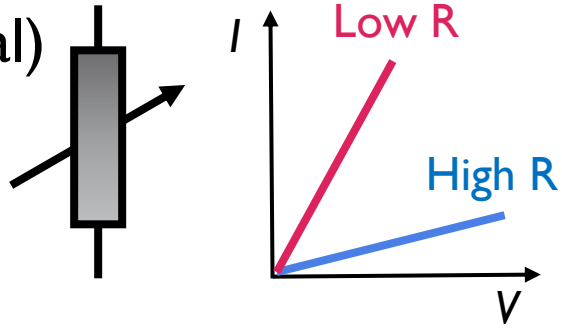
RRAM: Status

RRAM : classification & materials

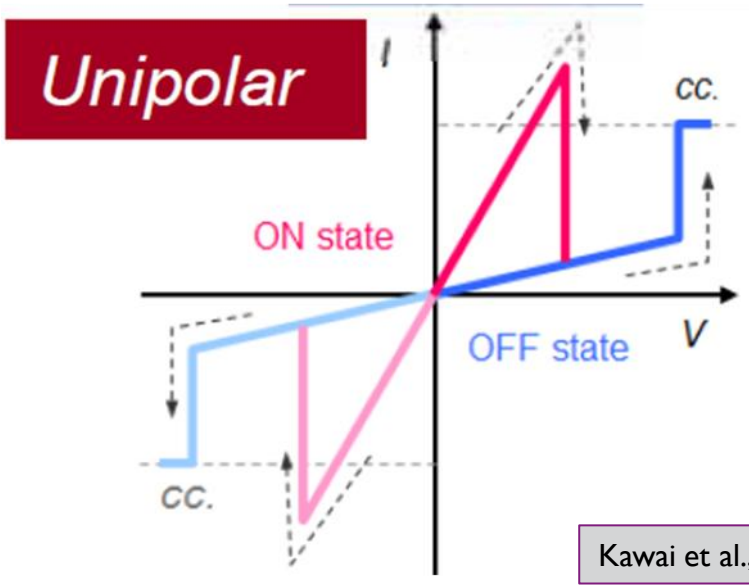
- **RRAM : general definitions & history...**
- Classification
- Filamentary switching
  - Properties of filamentary switching
  - Thermo-chemical RRAM
  - Bipolar "oxygen vacancy drift" RRAM
  - Electro-chemical CBRAM
- Interfacial switching

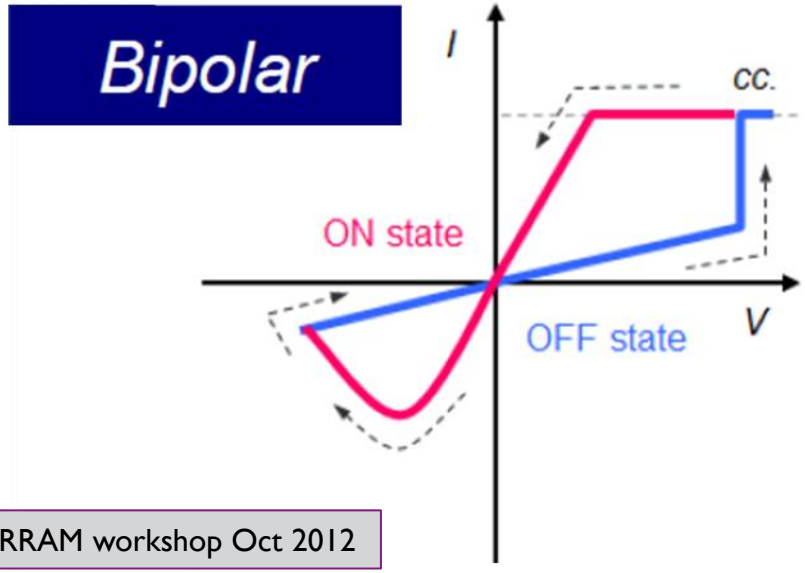
Resistive Switching Memories

- Memory element is R (MIM-type 2-terminal)
  - ρ can be altered by applying V/I on R
  - readout R at low voltage



- Bipolar or Unipolar Switching depending on mechanism





Kawai et al., 2nd RRAM workshop Oct 2012

Resistive Switching Memories

- **A 2-terminal resistor element with electrically alterable resistivity**
  - typically a low and high conductive state, although (controllable) multi conductive states would be an asset (MLC)
  - focus on programming with an electrical signal (e.g. not magnetic)
- **Focus on non-volatile resistivity change**
  - Different from Ovonic switching (electronic switching from low to high-conductive state, but requiring a hold current to remain in high-conductive state), and also of typical Mott transition element (as VO_2)
- **Focus on elements that can switch repeatedly from low to high conductive state.**
  - Different from typical Fuse or anti-Fuse element (limited application to OTP)

The Time-Voltage Dilemma

How can we make a 2-terminal NVM ?

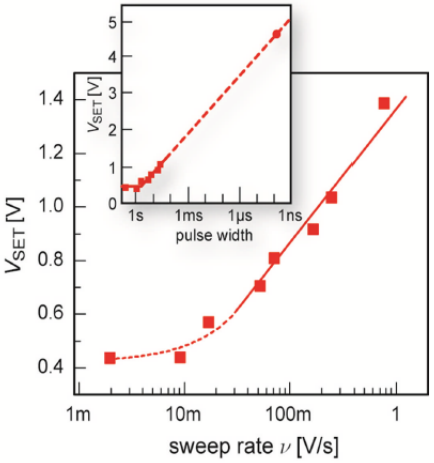
Fast programming

- At ~**1V**, need programming in **~10nsec**

Good retention

- At ~**0.1V**, need stable read for ~ 10 years

Write kinetics in Cu-SiO_2



Cu / SiO_2 (15nm) / Ir cells

SET voltage (write threshold) depends exponentially on rate of voltage change but saturates at high rates due to *nucleation overpotential* (for this case Cu on Ir)

C. Schindler, G. Staikov, and R. Waser, "Electrode kinetics of Cu–SiO_2-based resistive switching cells: Overcoming the voltage-time dilemma of electrochemical metallization memories," Appl. Phys. Lett., 94, 072109 (2009).

11

Need operation mechanism with extreme non-linear behavior:

>15 orders of magnitude in time over 1 decade in voltage

R.Waser (RWTH/Julich)

Discovery resistive switching in oxides : 1960's !

SiO !

Vol 11, May 1964, p. 243

IEEE TRANSACTIONS ON ELECTRON DEVICES

The Reversible Voltage-Induced Initial Resistance in the Negative Resistance Sandwich Structure

P. H. NIELSEN
N. M. BASHARA
Dept. of Elec. Engrg.
University of Nebraska
Lincoln, Neb.

Recently the authors have found that a high initial resistance can be read out for long periods of time as long as the voltage is kept well below that for maximum current.

The above obviously suggests use of this device as a memory element which can read out nondestructively and which can be "erased" at will by increasing the voltage to a value beyond that for maximum current. The upper frequency limit of this effect has not been determ neither has the usable read-out time.

Au/SiO/Au structure

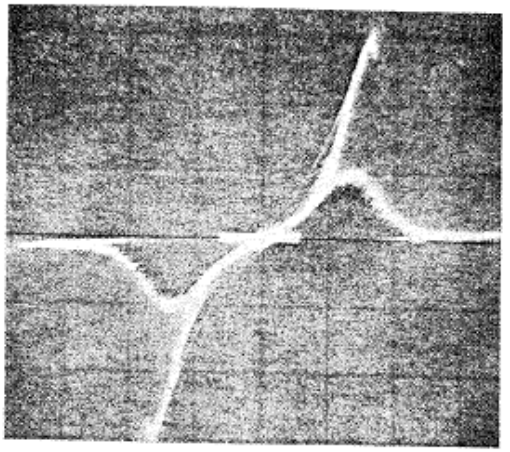


Fig. 1—Current-voltage locus, 60 cps. Ordinate scale is 40 ma/div, abcissa 2v/div. Superimposed is the high initial resistance locus resulting from *sudden* voltage removal at about 7-volts peak. The upper negative resistance curve is for voltage increasing, the lower for voltage decreasing.

The Radio and Electronic Engineer, August 1967

New Thin-film Resistive Memory

By
J. G. SIMMONS,
B.Sc., Ph.D., F.Inst.P.†
AND
R. R. VERDERBER,
B.Sc., M.Sc.‡

Summary: A new thin-film metal–insulator–metal device is described. After the insulator has undergone a forming process, which consists of the electrolytic introduction of gold ions from one of the electrodes, its conductivity is observed to have increased quite markedly. In addition the sample displays negative-resistance and memory phenomena. It is shown that under the appropriate switching conditions the device can be used as a non-volatile analogue memory with non-destructive read-out. The theory of operation of the device is also presented.

Resistive switching effect in *Transition Metal Oxides*

- First switching of NiO was already reported in 1964!

Solid-State Electronics Pergamon Press 1964. Vol. 7, pp. 785–797. Printed in Great Britain

SWITCHING PROPERTIES OF THIN NiO FILMS*

J. F. GIBBONS and W. E. BEADLE†
Stanford Electronics Laboratories, Stanford, California
(*Received* 30 *March* 1964)

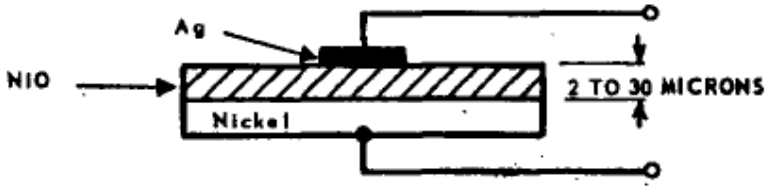


FIG. 1. Schematic representation of basic NiO thin-film device.

Whatever happened to….

- Resisitive switching memories based on these concepts eventually never developed :

  - problems of stability
  - scaling questioned
  - **emergence & rapid successful development of Si-based memories !**

Recent surge of interest

5 important events that put oxide RRAM again in the picture :

1. A.Beck, B.J.Bednorz et al, IBM Zurich, APL 2000
2. W.Zhuang et al, Sharp/Univ Houston, IEDM 2002
3. I.G.Baek et al., Samsung, IEDM 2004
4. D.B.Strukov et al, HP labs, Nature 2008
5. H.Y.Lee et al, ITRI, IEDM, Tech. Dig., p. 297 2008

1. A.Beck, B.J.Bednorz et al, IBM Zurich, APL 2000

The Radio and Electronic Engineer, August 1967

U.D.C. 537.226

New Thin-film Resistive Memory

By
J. G. SIMMONS,
B.Sc., Ph.D., F.Inst.P.†
AND
R. R. VERDERBER,
B.Sc., M.Sc.‡

- Thin oxide films for memory are back !

...ed. ... the electrolytic introduction of gold ions from one of the electrodes, its conductivity is observed to have increased quite markedly. In addition the sample displays negative-resistance and memory phenomena. It is shown that under the appropriate switching conditions the device can be used as a non-volatile analogue memory with non-destructive read-out. The theory of operation of the device is also presented.

33 yrs

APPLIED PHYSICS LETTERS VOLUME 77, NUMBER 1 3 JULY 2000

Reproducible switching effect in thin oxide films for memory applications

A. Beck, J. G. Bednorz, Ch. Gerber, C. Rossel,[a] and D. Widmer
IBM Research, Zurich Research Laboratory, CH–8803 Rüschlikon, Switzerland

(Received 13 March 2000; accepted for publication 15 May 2000)

Thin oxide films with perovskite or related structures and with transition metal doping show a reproducible switching in the leakage current with a memory effect. Positive or negative voltage pulses can switch the resistance of the oxide films between a low- and a high-impedance state in times shorter than 100 ns. The ratio between these two states is typically about 20 but can exceed six orders of magnitude. Once a low-impedance state has been achieved it persists without a power connection for months, demonstrating the feasibility of nonvolatile memory elements. Even multiple levels can be addressed to store two bits in such a simple capacitor-like structure. © *2000 American Institute of Physics.* [S0003-6951(00)04327-8]

2. W.Zhuang et al, Sharp/Univ Houston, IEDM 2002

- coined the term RRAM
- realization 1D1R array

Novell Colossal Magnetoresistive Thin Film Nonvolatile Resistance Random Access Memory (RRAM)

W. W. Zhuang[1], W. Pan[1], B. D. Ulrich[1], J. J. Lee[1], L. Stecker[1], A. Burmaster[1], D. R. Evans[1], S. T. Hsu[1], M. Tajiri[2], A. Shimaoka[2], K. Inoue[2], T. Naka[2], N. Awaya[2] K. Sakiyama[2], Y. Wang[3], S. Q. Liu[3], N. J. Wu[3], and A. Ignatiev[3]

1: Sharp Laboratories of America, 5700 NW Pacific Rim Blvd, Camas, WA 98607, USA
2: Sharp Corporation, IC Group, 2613-1 Ichinomoto-cho, Tenri, Nara 632, Japan
3: Texas Center for Superconductivity and Advanced Material , University of Houston, Houston, Texas 77204-5002 USA

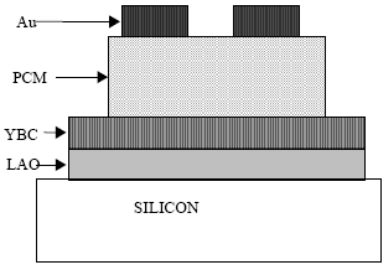


Fig.1 Pulsed Laser Deposited (PLD) test memory resistor structure. The memory material is PCMO ($Pr_{0.7}Ca_{0.3}MnO_3$). The double bottom electrode is formed with YBCO ($YBa_2Cu_3O_{7-x}$) on LAO ($LaAlO_3$)

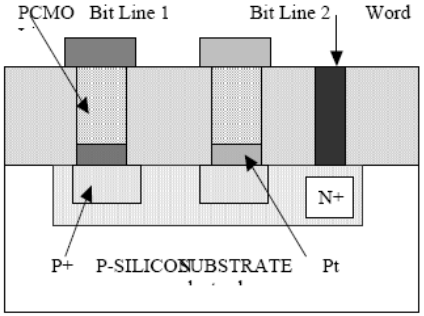


Fig.3 Resistor/diode memory array cell structure. Both top and bottom electrode of the memory resistor is made of Pt. The cell size can be as small as $4F^2$ This memory array required positive pulse for bot write and reset programming

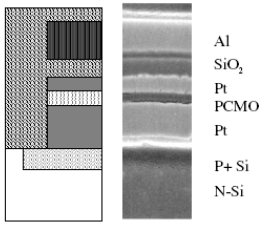


Fig.5 TEM microphotograph of a 1R1D memory cell. Shallow P+ layer is formed onto n bit line. The memory array interconnect is copper doped Al.

Principle on bulk crystals published by A.Asamitsu et al., Nature, 1997

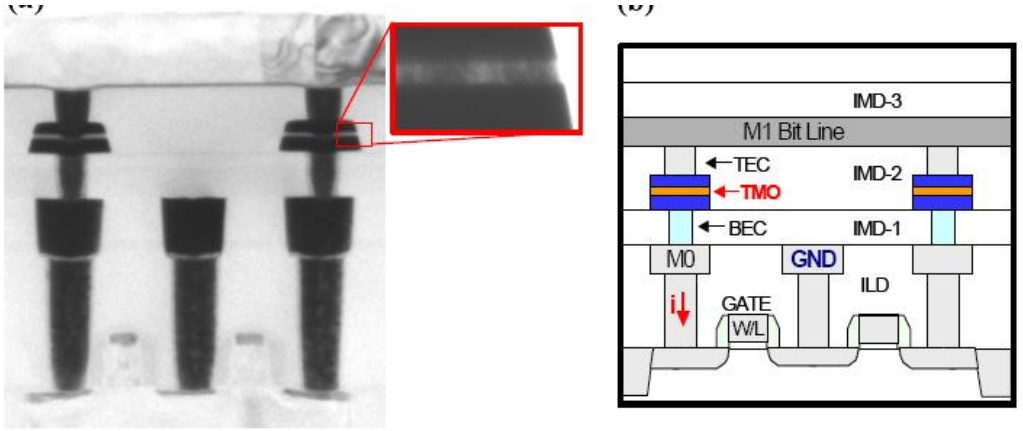
3. I.G.Baek et al., Samsung, IEDM 2004

- 1st advanced work (integrated device) with simple binary oxide (NiO)
- Coined the term OxRRAM (switching in TMO)

Highly Scalable Non-volatile Resistive Memory using Simple Binary Oxide Driven by Asymmetric Unipolar Voltage Pulses

I. G. Baek, M. S. Lee, S. Seo*, M. J. Lee*, D. H. Seo*, D.-S. Suh*, J. C. Park*, S. O. Park, H. S. Kim, I. K. Yoo*, U-In Chung and J. T. Moon

IEDM 2004



4. D.B.Strukov et al.,HP labs,Nature2008

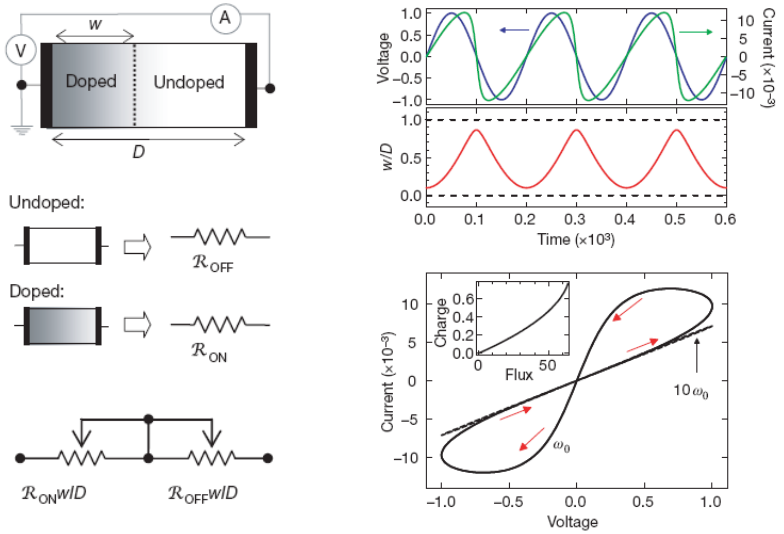
- Memristor concept applied to RRAM
- Triggered a lot of interest, especially in EE (design) world

Vol 453|1 May 2008|doi:10.1038/nature06932

The missing memristor found

Dmitri B. Strukov[1], Gregory S. Snider[1], Duncan R. Stewart[1] & R. Stanley Williams[1]

$$M(q) = \mathcal{R}_{\mathrm{OFF}}\left(1 - \frac{\mu_V \mathcal{R}_{\mathrm{ON}}}{D^2} q(t)\right)$$



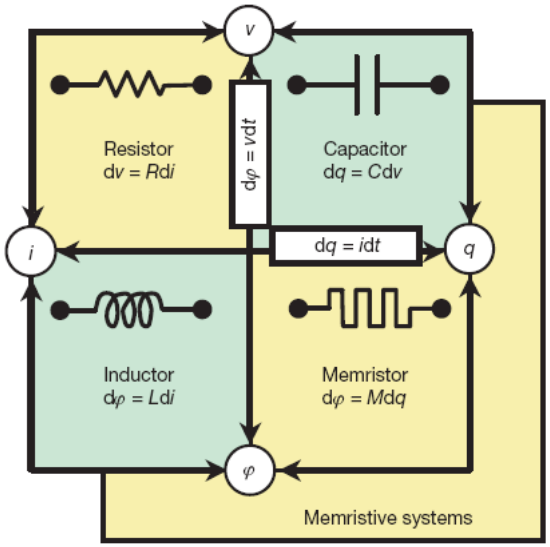


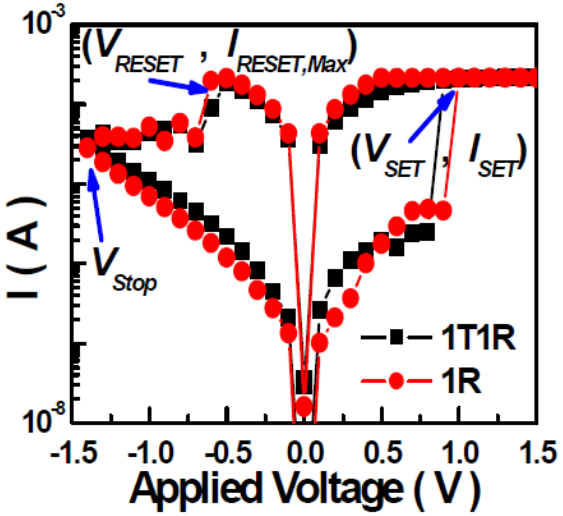
Figure 1 | The four fundamental two-terminal circuit elements: resistor, capacitor, inductor and memristor. Resistors and memristors are subsets of a more general class of dynamical devices, memristive systems. Note that R, C, L and M can be functions of the independent variable in their defining equations, yielding nonlinear elements. For example, a charge-controlled memristor is defined by a single-valued function $M(q)$.

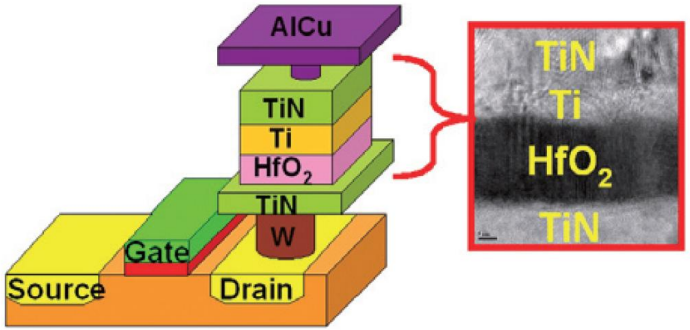
5. H.Y.Lee et al, ITRI, IEDM 2008

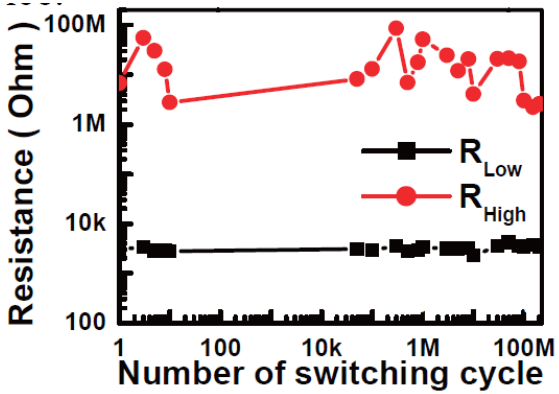
- First RRAM cell using all excellent CMOS compatible materials:
- HfO_2 as switching oxide; TiN/Ti as electrode materials
- High cyclability, bipolar switching

Low Power and High Speed Bipolar Switching with A Thin Reactive Ti Buffer Layer in Robust HfO_2 Based RRAM

H. Y. Lee[1,3], P. S. Chen[2], T. Y. Wu[1], Y. S. Chen[1], C. C. Wang[1], P. J. Tzeng[1], C. H. Lin[1], F. Chen[1], C. H. Lien[3], and M.-J. Tsai[1]





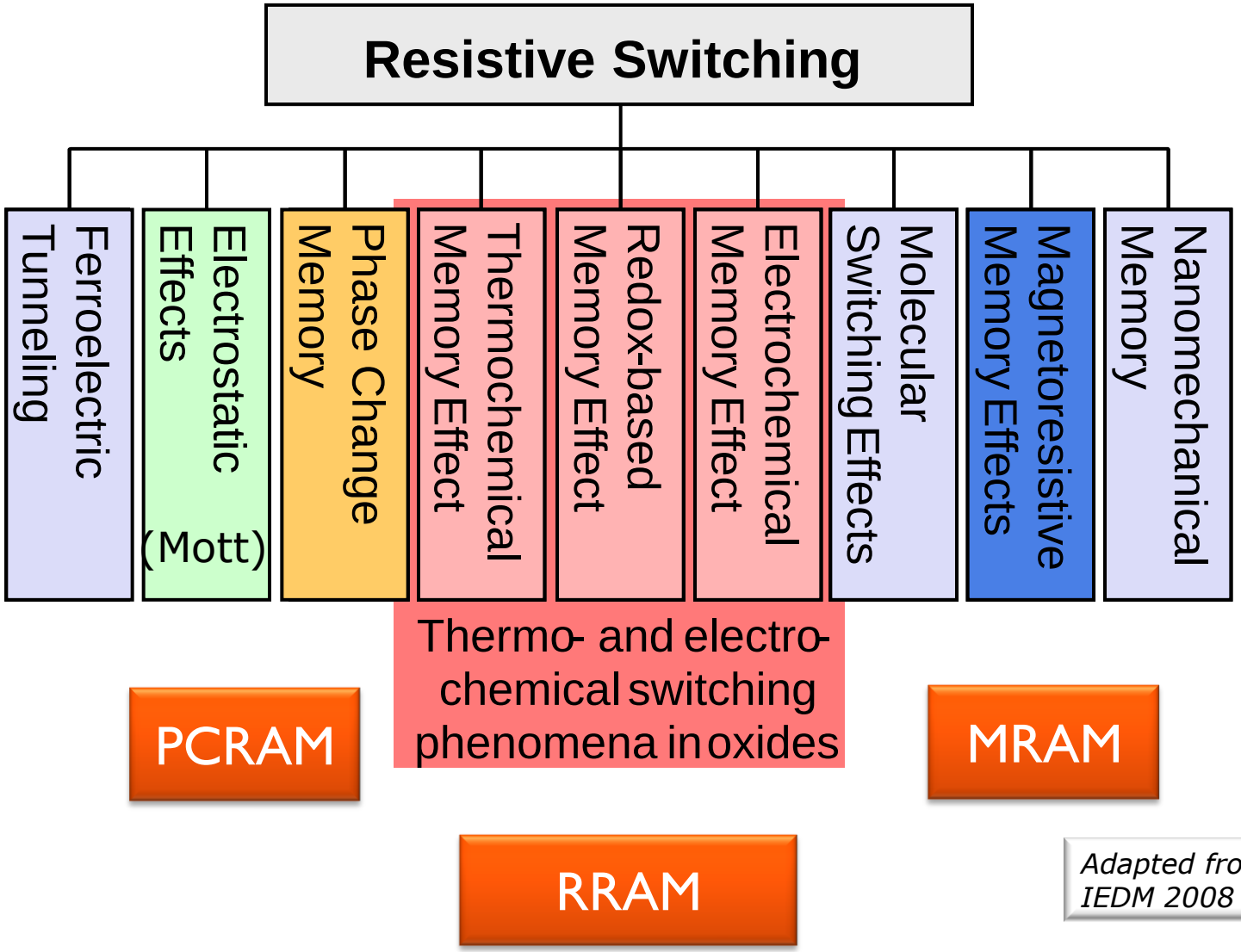


IEDM 2008

RRAM : classification & materials

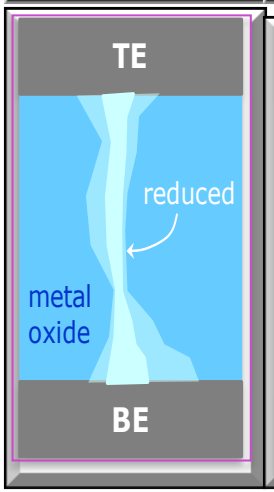
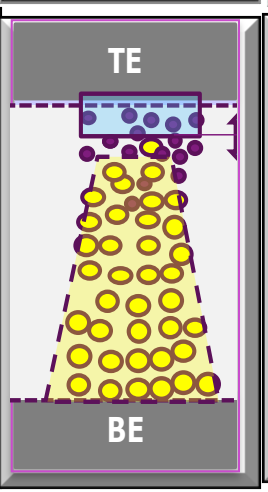
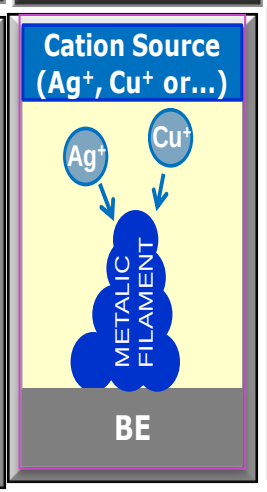
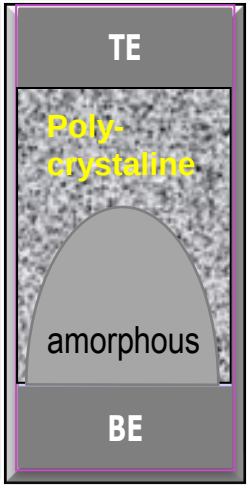
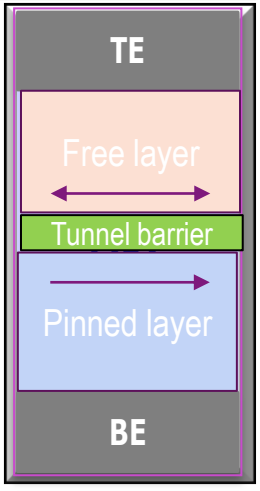
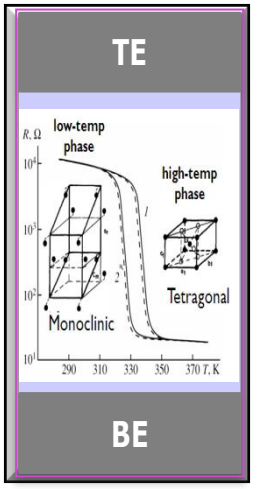
- RRAM : general definitions & history...
- **Classification**
- Filamentary switching
  - Properties of filamentary switching
  - Thermo-chemical RRAM
  - Bipolar "oxygen vacancy drift" RRAM
  - Electro-chemical CBRAM
- Interfacial switching

Taxonometry of Resistive Switching Memories : based on Mechanism



Adapted from R.Waser, IEDM 2008

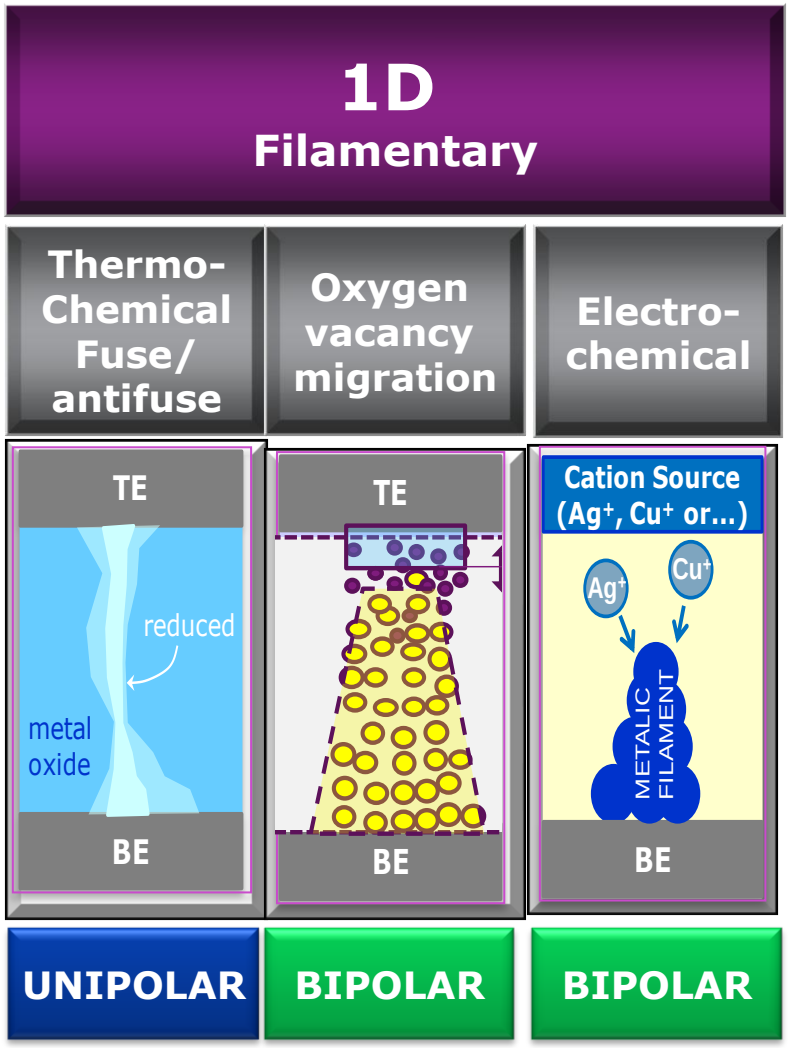
Resistance Modulation Geometry

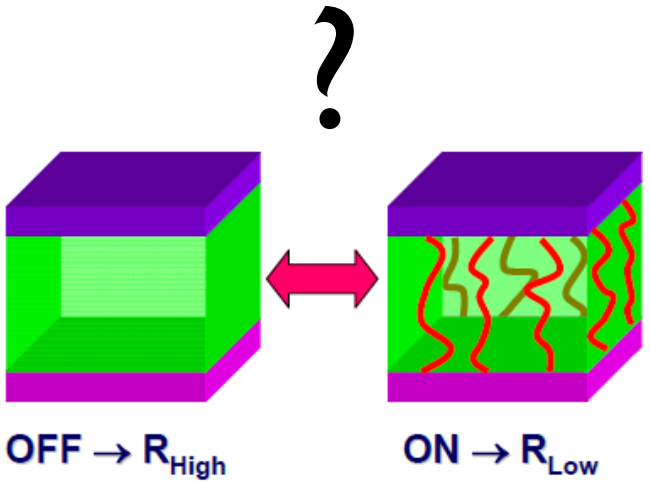
1D Filamentary			2D Interfacial	3D Bulk Transition			
Thermo-Chemical Fuse/ antifuse	Oxygen vacancy migration	Electro-chemical	Schottky barrier	Phase change	Tunnel Magneto resistance	Electronic MIT (Mott)	
							
UNIPOLAR	BIPOLAR	BIPOLAR	BIPOLAR	UNIPOLAR	BIPOLAR	UNIPOLAR	
RRAM				PCRAM	MRAM	?	

RRAM : classification & materials

- RRAM : general definitions & history...
- Classification
- **Filamentary switching**
  - **Properties of filamentary switching**
  - Thermo-chemical RRAM
  - Bipolar "oxygen vacancy drift" RRAM
  - Electro-chemical CBRAM
- Interfacial switching

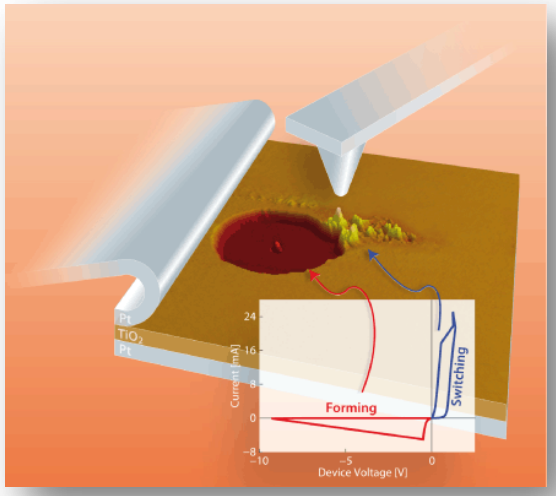
1D Filamentary switching



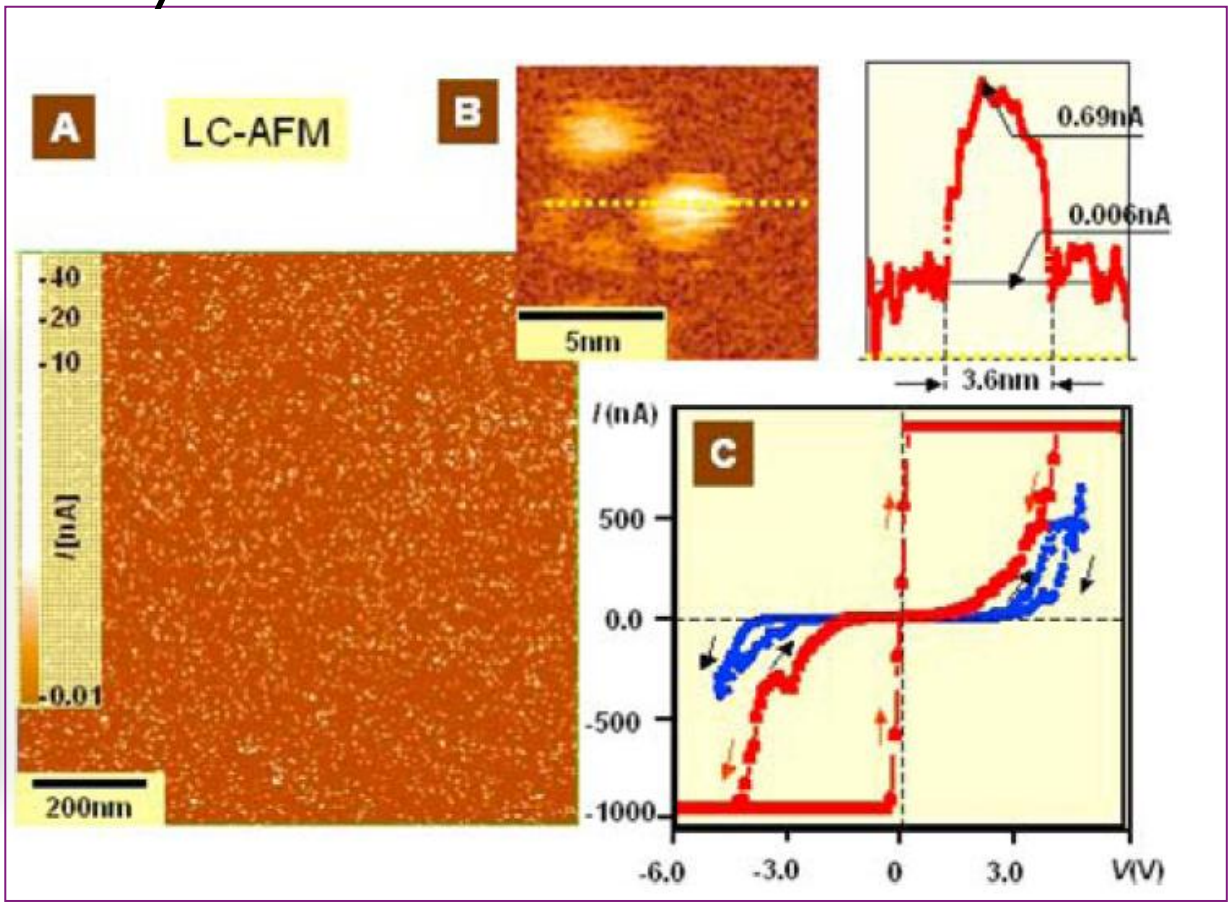


Indications for filamentary switching

From physico-chemical analysis



R. Münstermann et al., PSS RRL4 (2010) 16-18

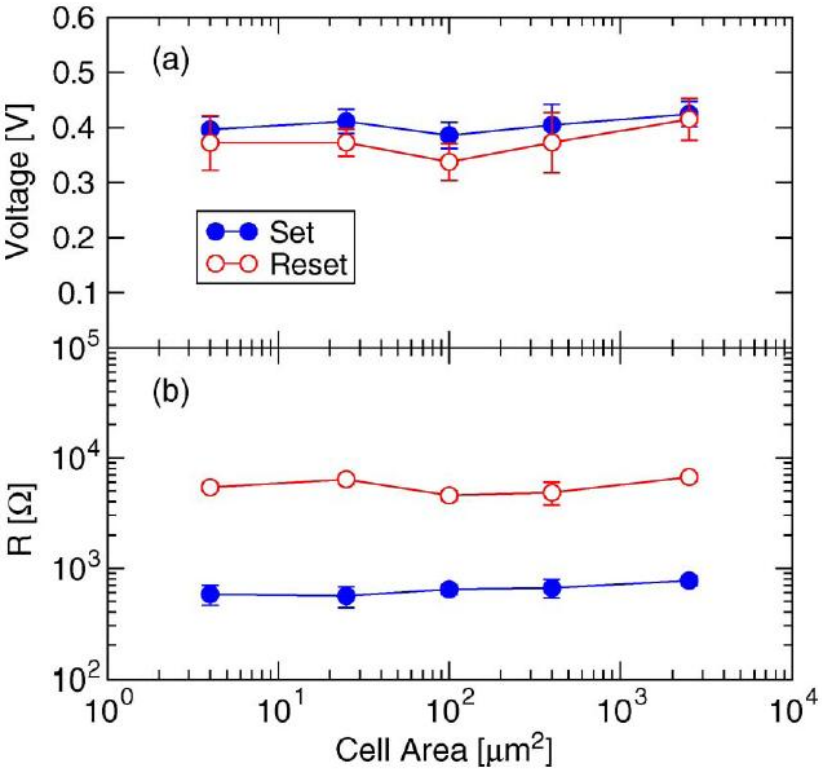


K. Szot, Phys. stat. sol. (RRL) 1, No. 2, R86–R88 (2007) / DOI 10.1002

Indications for filamentary switching

Electrical fingerprint from device characteristics

- Area (in)dependence of LRS/HRS and switching voltages

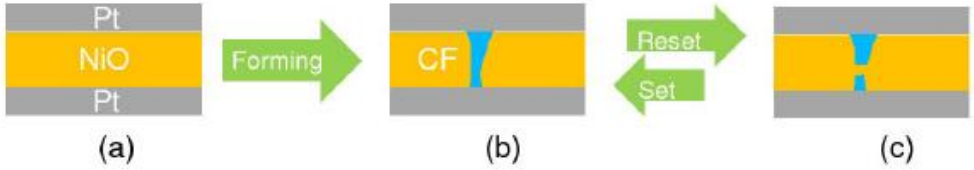


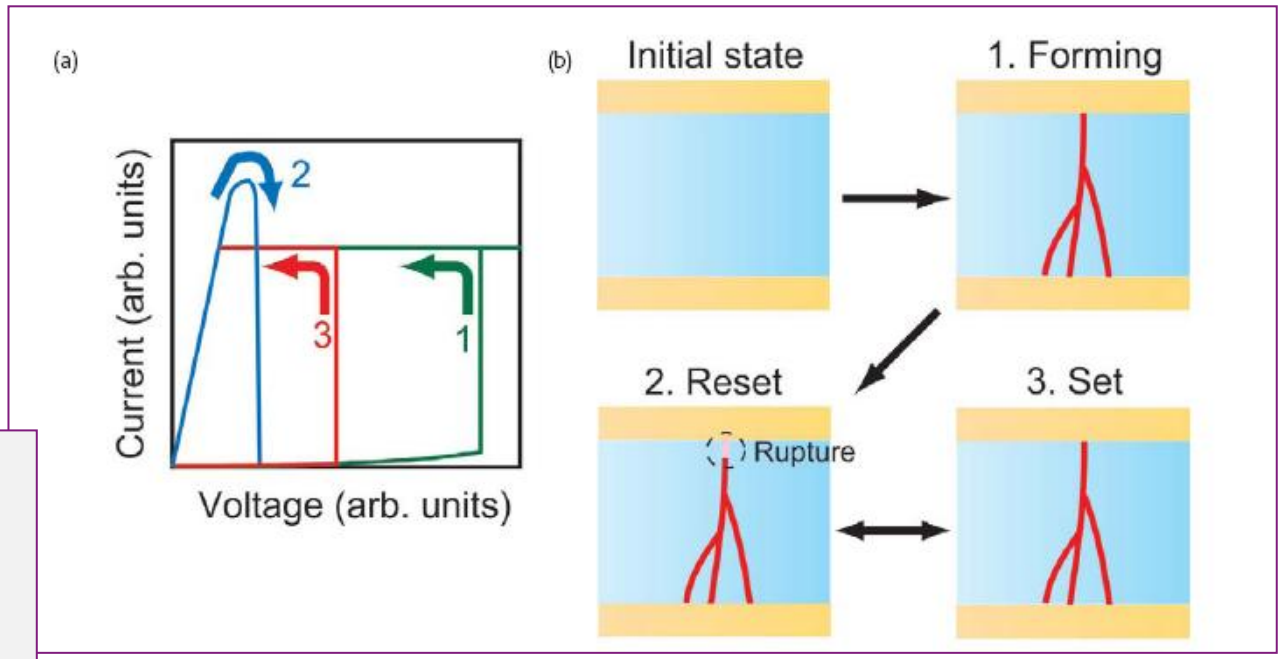
F.Nardi et al, IEEE Trans. El.Dev. 59(9). 2661 (2012)

Different steps in a filamentary switching process

C.Cagli, IEDM 2008

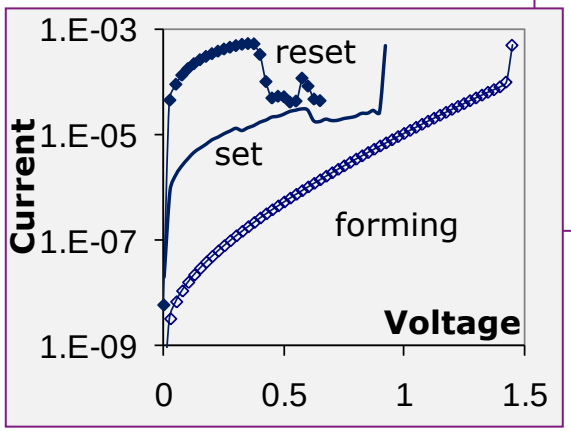
- Forming
- RESET
- SET





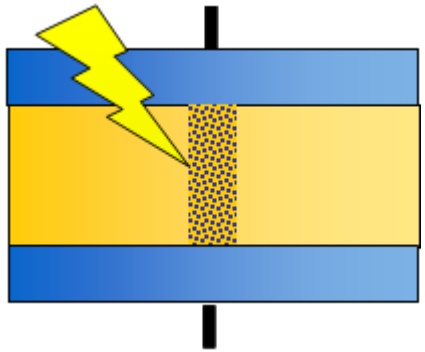
Akihito Sawa, materialstoday, Vol11(6), 2008

real switching curves

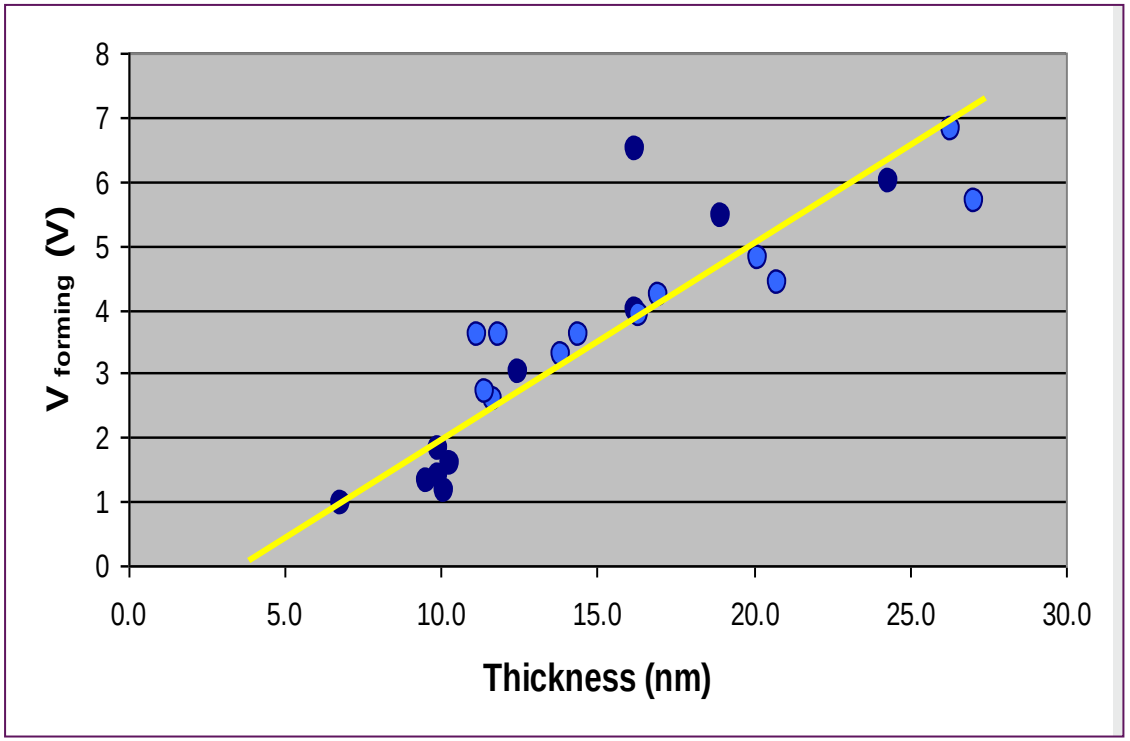


L.Goux (imec), NiO/Ni RRAM cell

Forming: creating a conduction path by "breakdown"



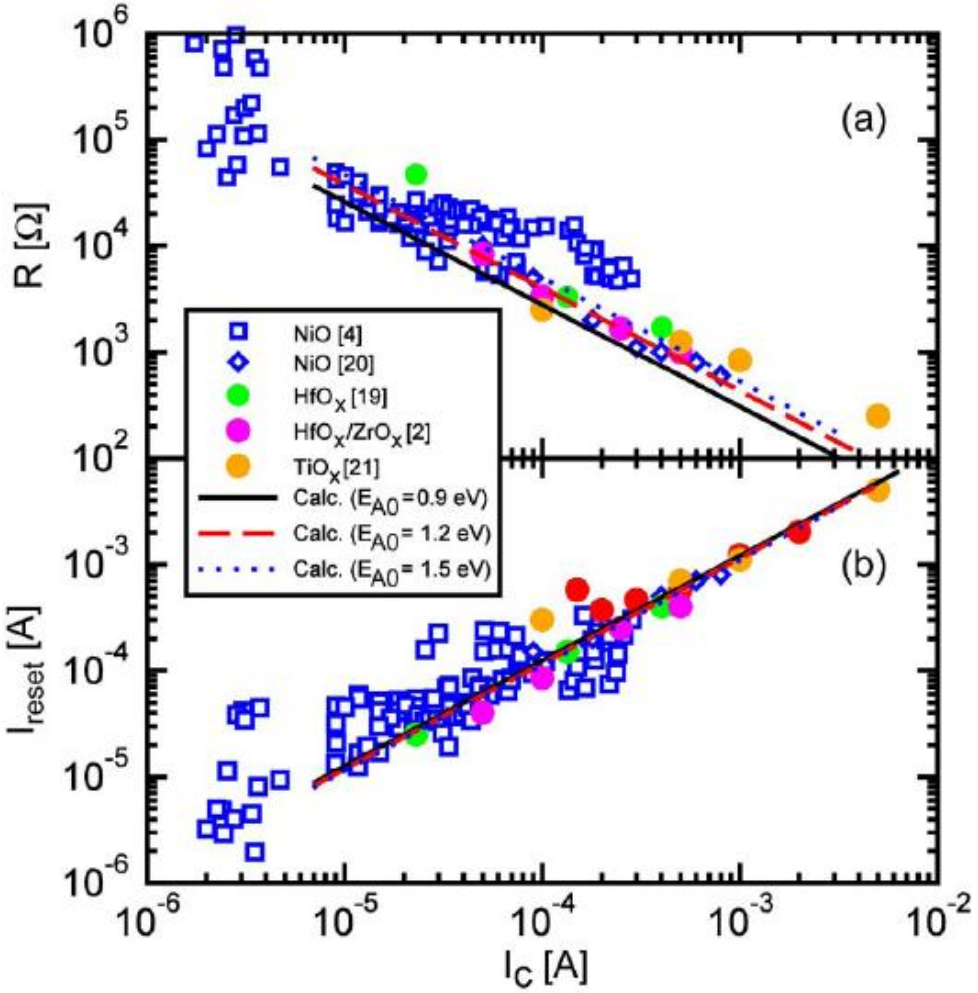
Forming voltage scales with thickness



NiO by MOCVD imec

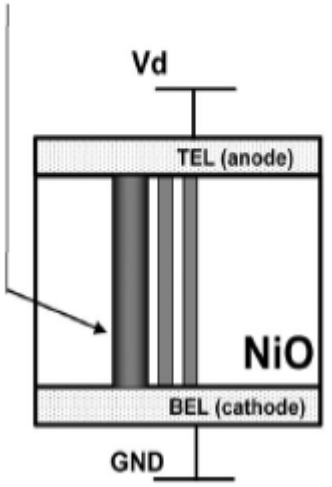
Similar to (soft) breakdown in dielectrics (defect & percolation path generation)

Maximum current during Forming(/SET) controls filament "Strength"



D.Ielmini et al, Trans.El.Dev. 58(12), p.4309, 2011

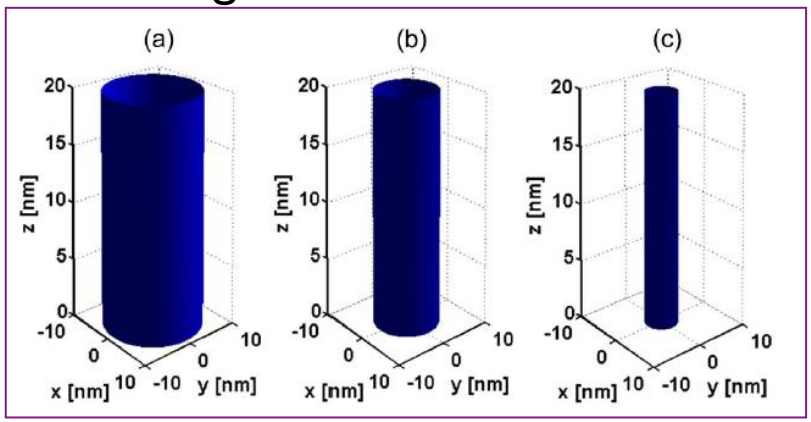
Filament size determined by SET current compliance



Y.Satoet al, Trans.El.Dev. 2008

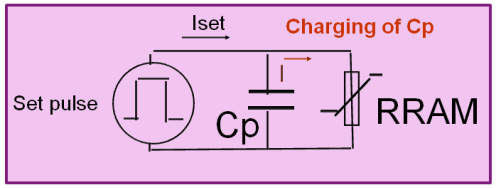
"Scaling of filamentary switching"

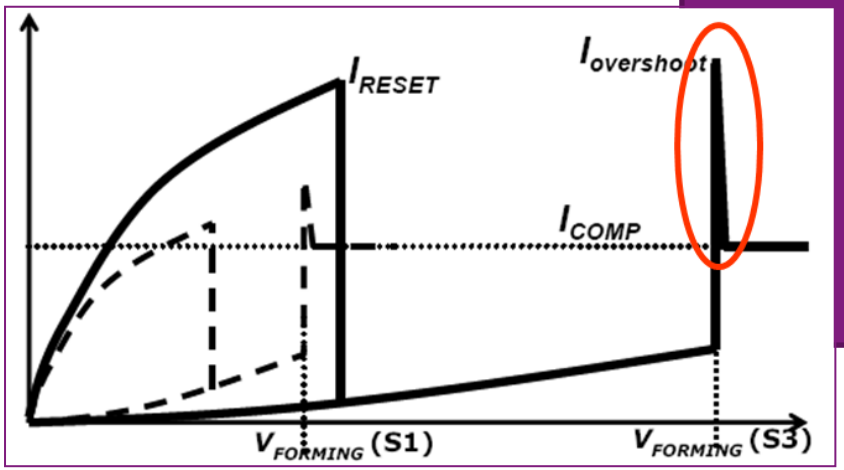
- 2D and 3D switching:
  - Current levels scale with area of the cell ~ F^2
- 1D switching:
  - Current levels **independent of cell area**
  - Current level determined by filament "diameter"
    - **Determined by operation conditions** (Forming/SET CC)
    - We can have small current even in large device
  - Limitations ?
    - Cell area ~ filament size..
    - Smallest filament size ?
      - ~ nm ??

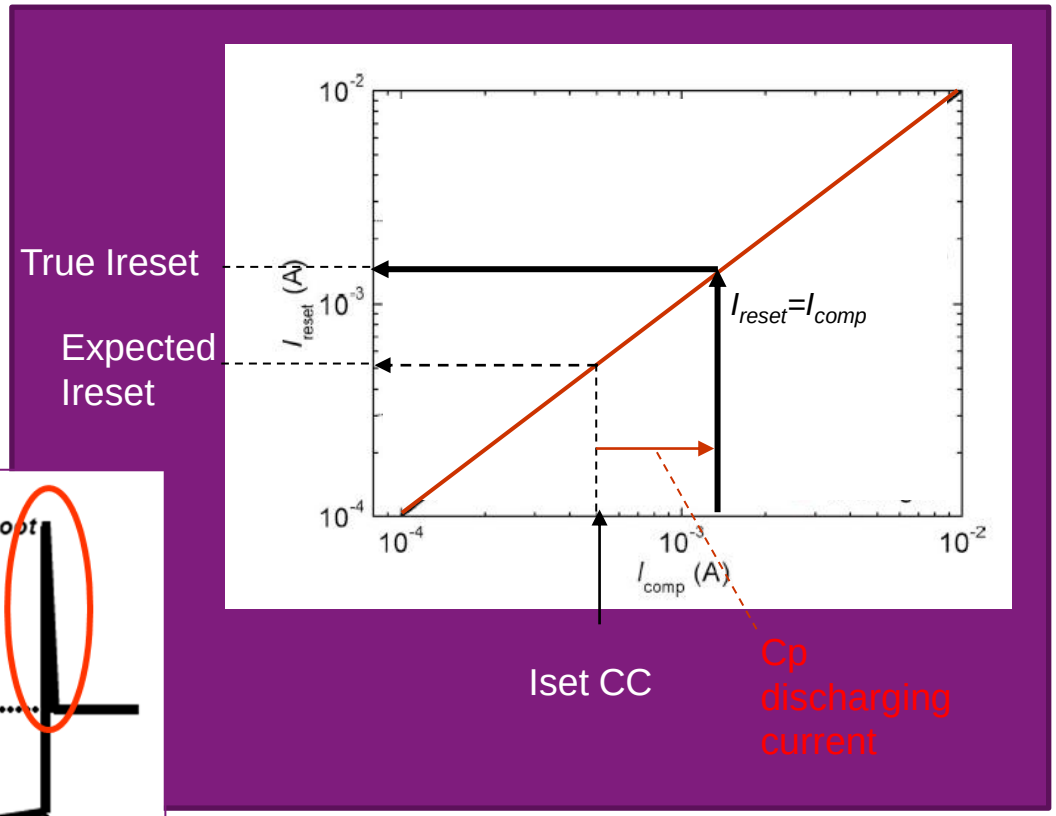


F.Nardi et al, Trans.El.Dev. 59(9), p.2461,2012

Influence of spike currents

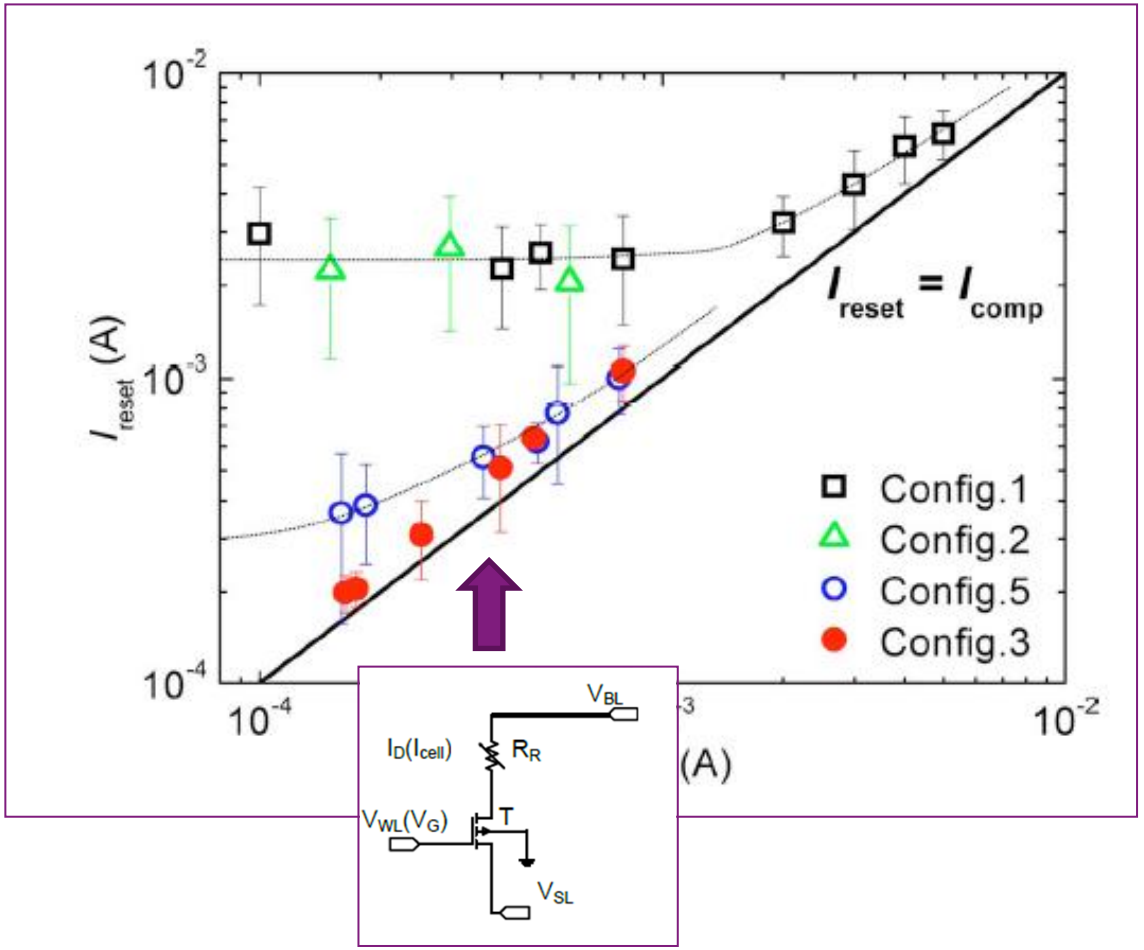






L.Goux et al, IEEE TED 2009 (sept 09)

1T1R integrated teststructure for stable current control



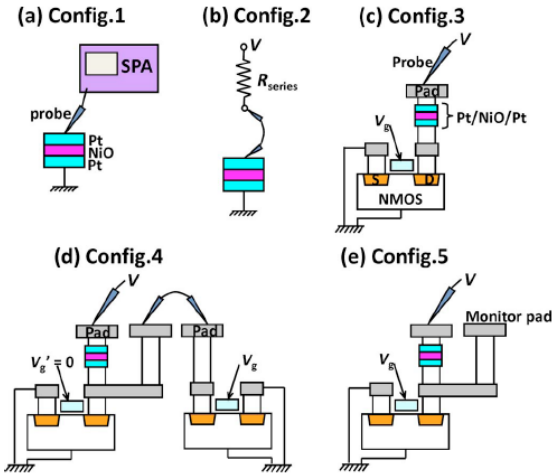
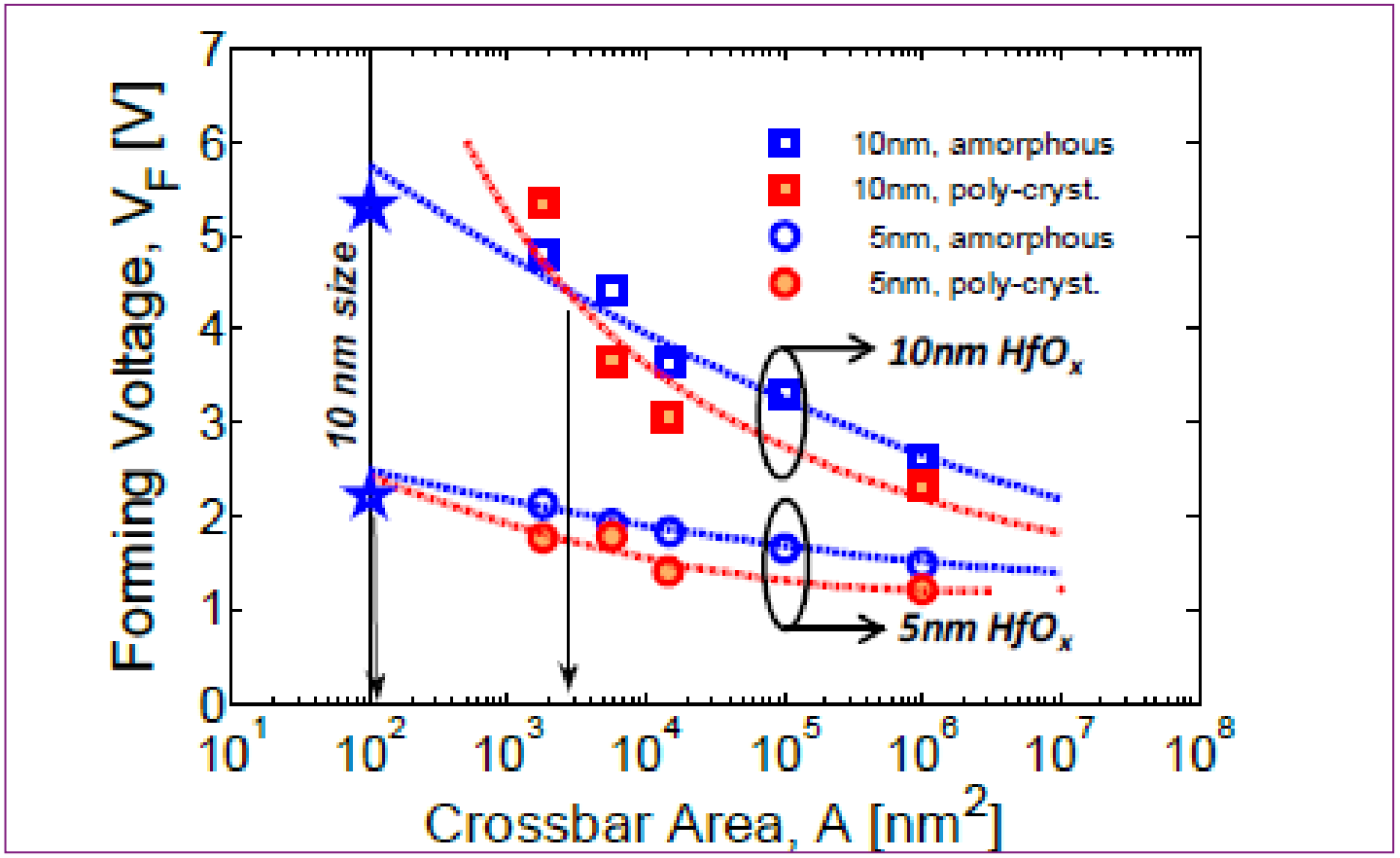


FIG. 1. (Color online) Five configurations used to measure I_{reset}-I_{comp} characteristics: The circuit composed by connecting (a) a current limiter built into the SPA and (b) a resistance, respectively, to the Pt/NiO_x/Pt structure. (c) The 1T1R cell consisting of the Pt/NiO_x/Pt structure and the cell transistor. (d) The circuit composed by connecting the drain of 1T to the Pt/NiO_x/Pt structure of the 1T1R cell with the monitor pad via probes and a coaxial line. (e) The 1T1R cell with the monitor pad.

Kinoshita et al, APL vol. 93

Intrinsic Forming voltage scaling

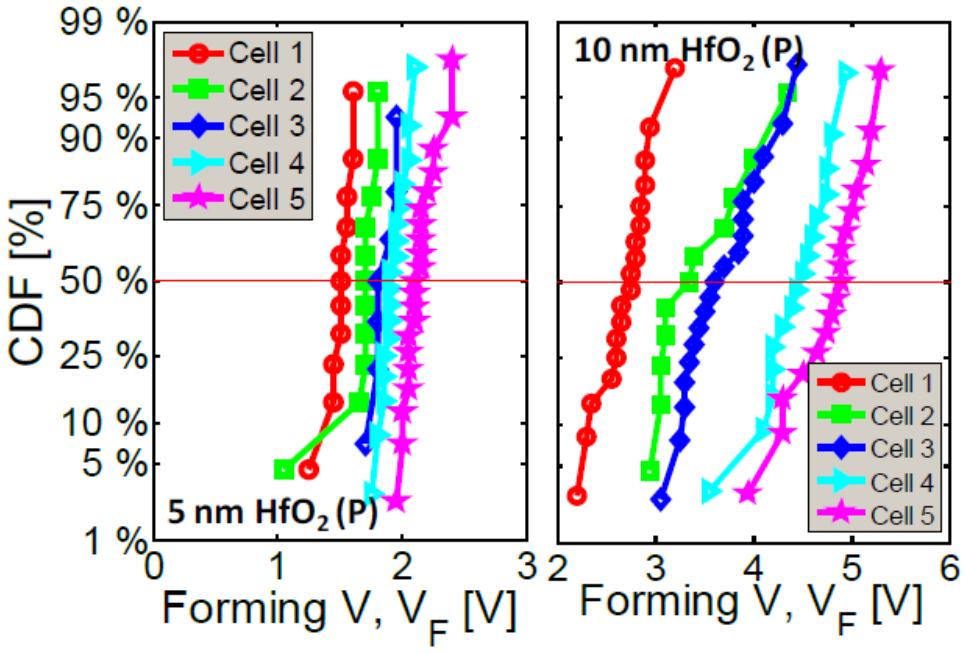


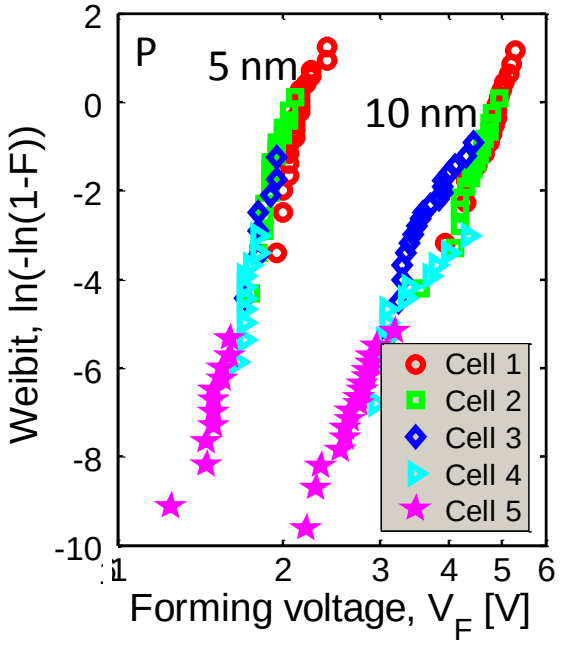
B.Govoreanu, IEDM 2011

Area dependence of Forming voltage

Due to defect distribution statistics

- Fitting single area-scaled Weibull plot



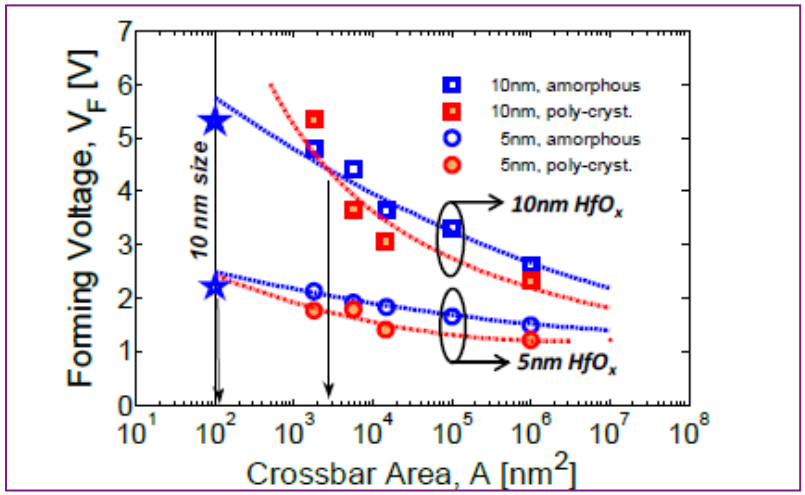


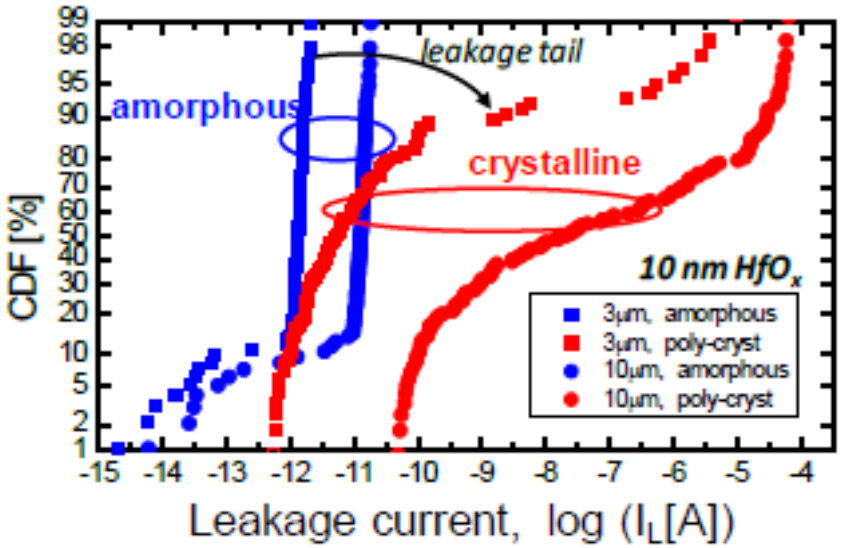
B.Govoreanu, SSDM 2011

Area dependence of Forming

Due to defect distribution statistics

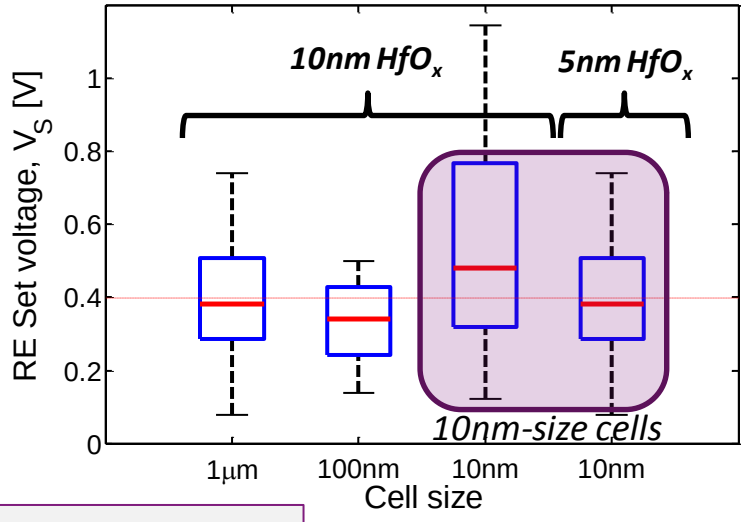
- Difference between **amorphous** and **crystalline** $V_{FORMING}$: linked to different leakage current tails



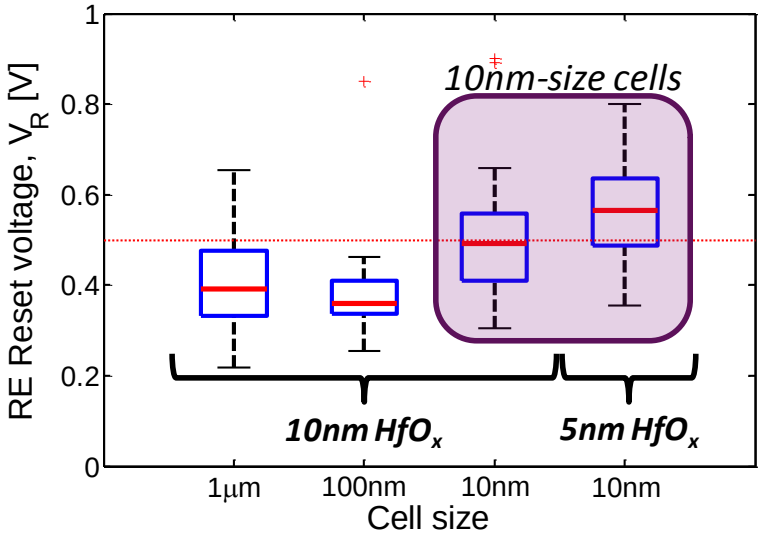


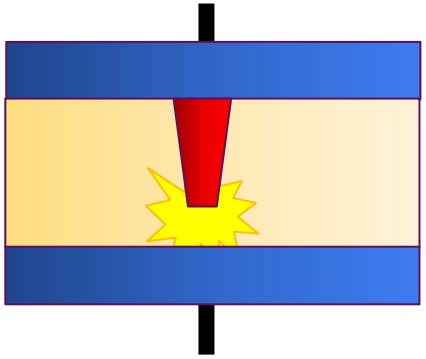
B.Govoreanu, IEDM 2011

Switching during SET/RESET: SET ≠ Forming



B.Govoreanu, IEDM2011

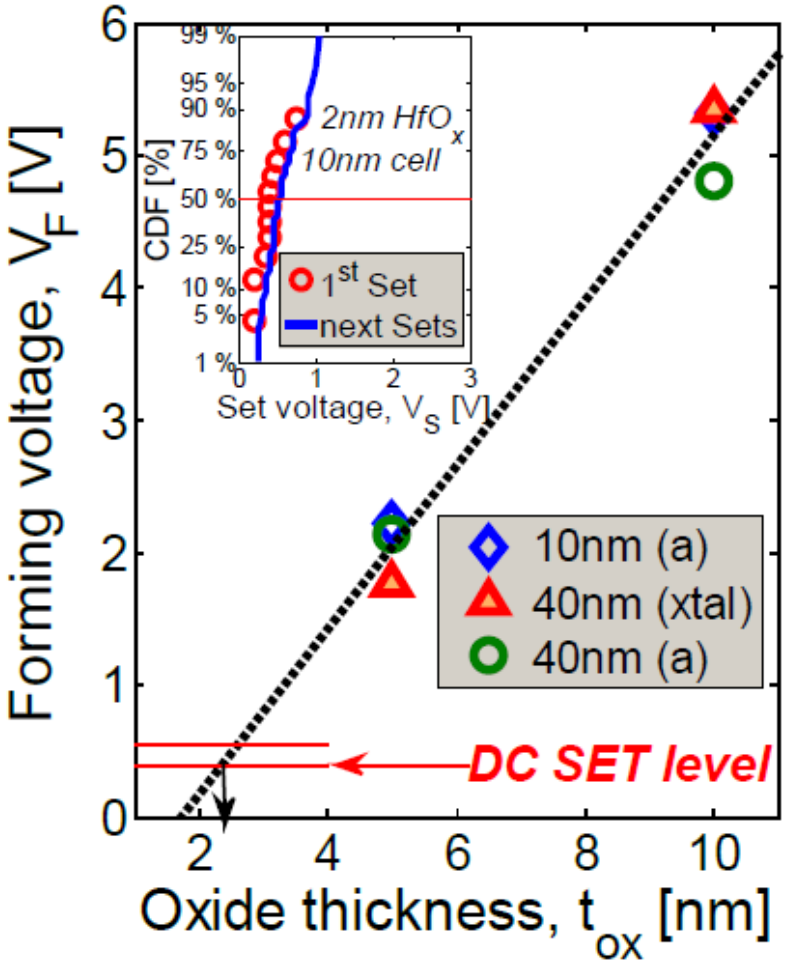




Absence of oxide thickness effect on $V_{SET/RESET}$ indicative of LOCAL filament switching

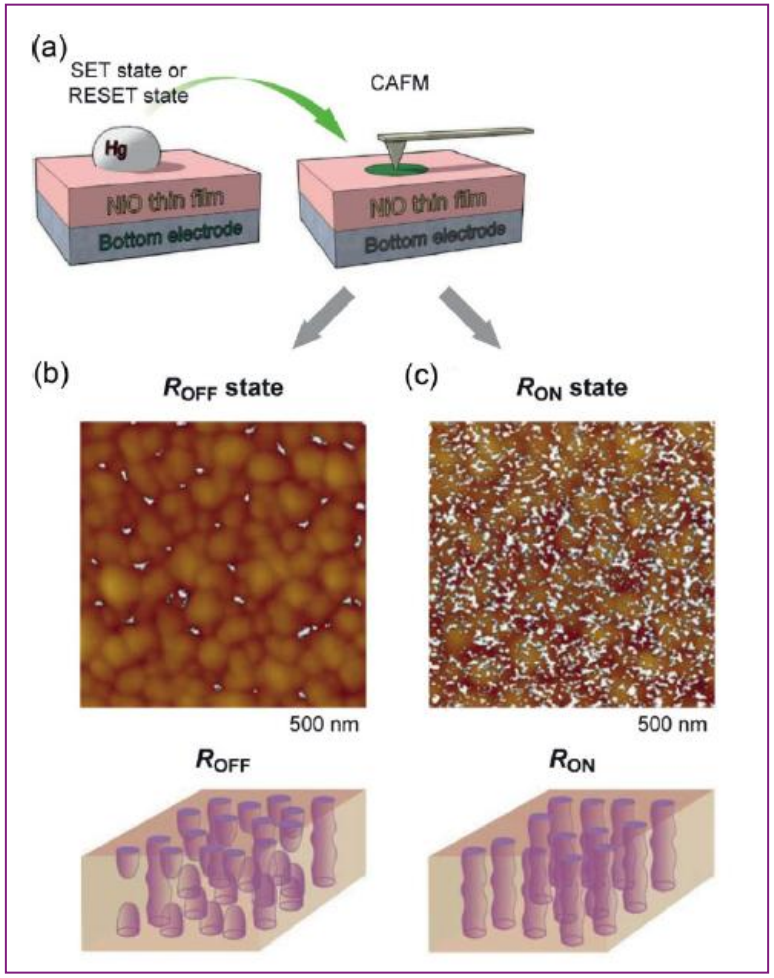
Forming free for thin films ?

- Linear scaling with oxide thickness:
  - Field driven
- Predicts "forming-free" behavior if t_{ox}<2.5 nm
  - limitation ?
    - new filament creation @ each Set ?

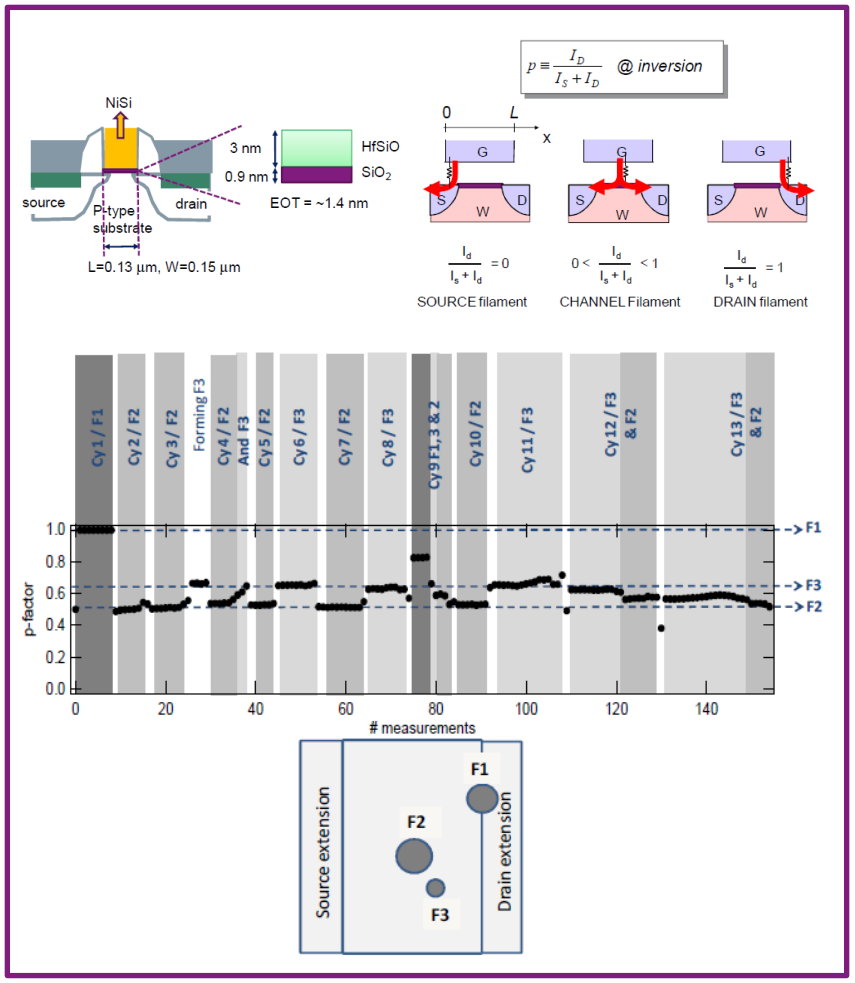


B.Govoreanu et al, IEDM 2011

Single or multiple filaments ?



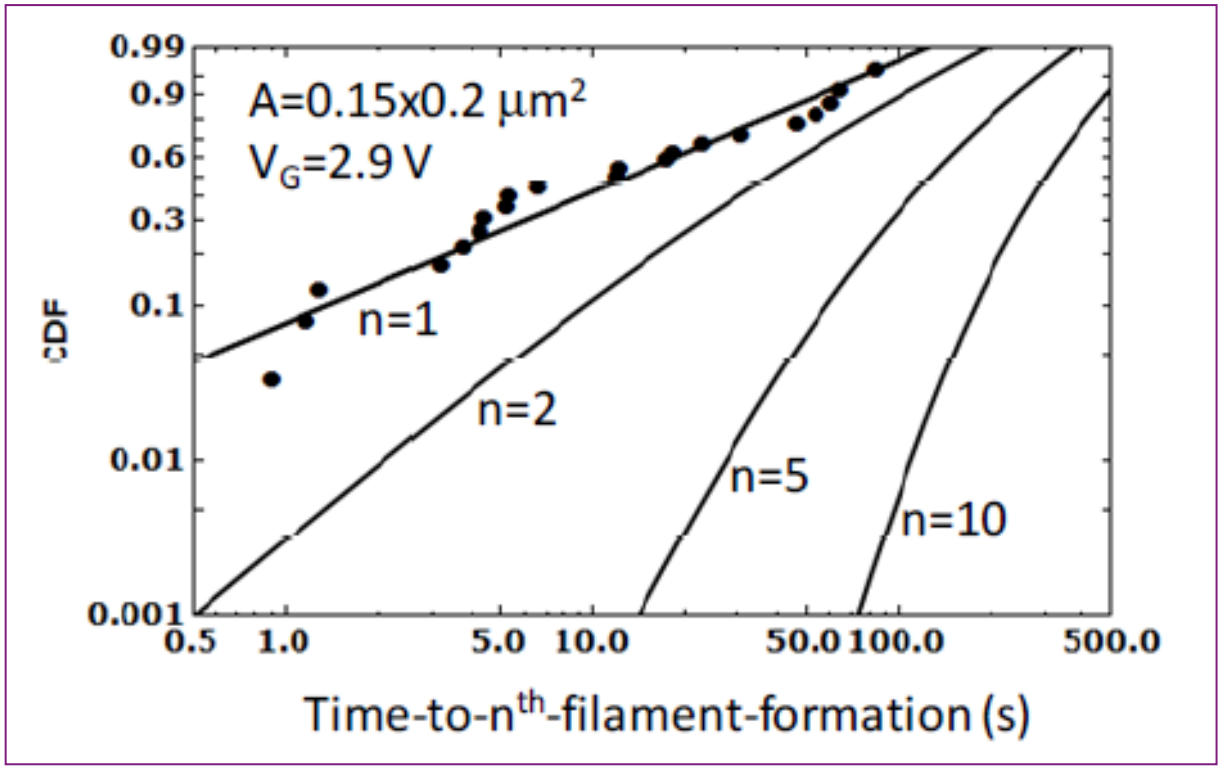
J.Y.Son, Y.-H.Shin, Appl.Phys.Lett. 2008,92,222106



R.Degraeve et al., IEDM 2010

Indications of multi-filaments?

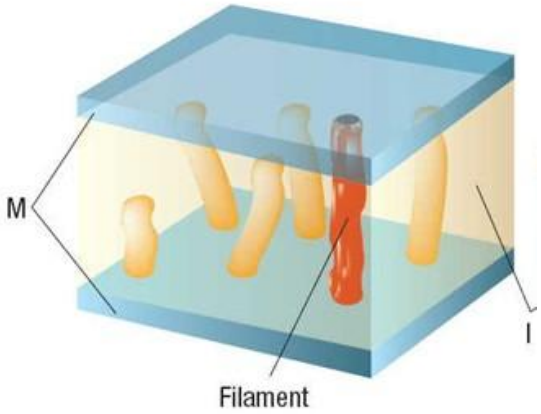
"Forming" at lower voltage...



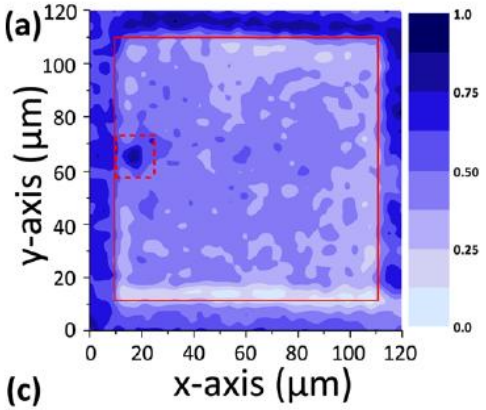
R.Degraeve et al., IEDM 2010

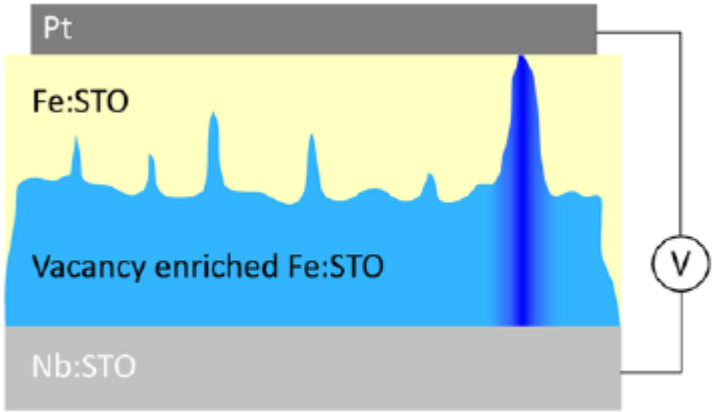
BD theory predicts possible activation of new filaments even at lower SET voltage..

The winner takes it all ?



Most models assume single filament





Ch. Lenser et al., J. Appl. Phys. 111, 076101 (2012);

RRAM : classification & materials

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  - **Thermo-chemical RRAM**
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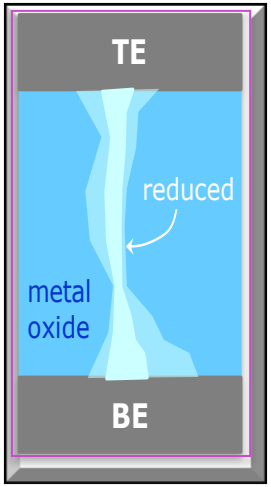
- Interfacial switching

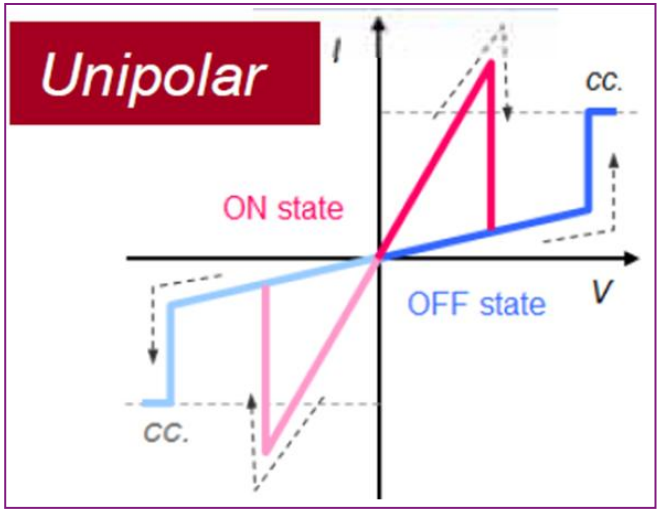
Unipolar Switching OxRRAM : "Thermo-Chemical Fuse/antifuse"

1D
Filamentary

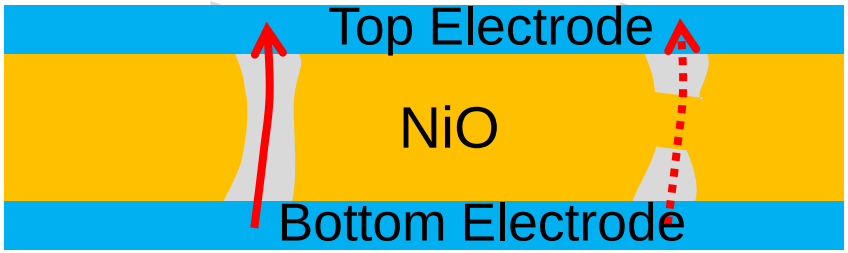
Thermo-Chemical Fuse/ antifuse



UNIPOLAR



Material : Transition Metal-Oxides, e.g. NiO, HfO,..



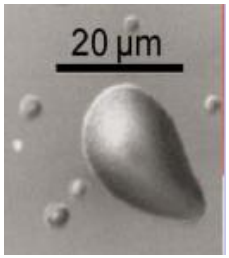
Conductive filament (CF)

Low R
Set state

High R
Reset state

Role of oxygen / oxygen vacancy defects in OxRRAM memories

- Filament switching involves oxygen transport

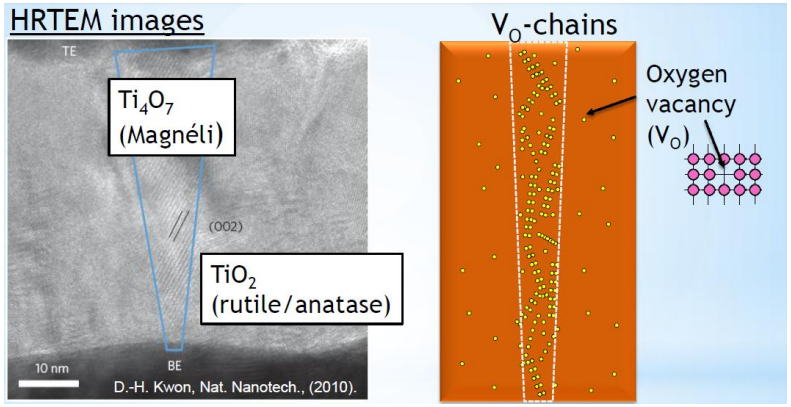


Bubbles < O2 released to the gas phase or adsorbed by the grainboundaries of the Pt electrode

Szot et al., Nature materials (2006)

- Filament observations indicate local lower O concent
  - Magnelli phase of Ti_4O_7 or Ti_5O_9 , essentially TiO_{2-x}

→ Oxygen vacancy defects

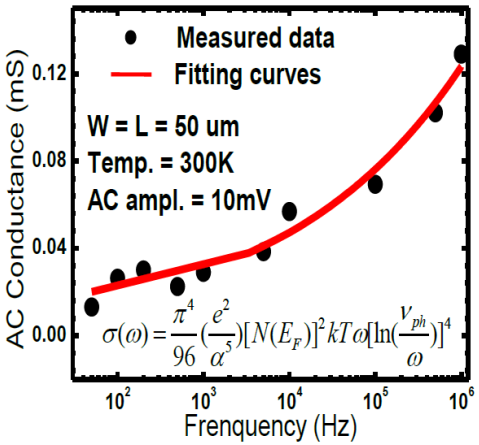


D. H. Kwon et al., Nature Nano technology(2010)

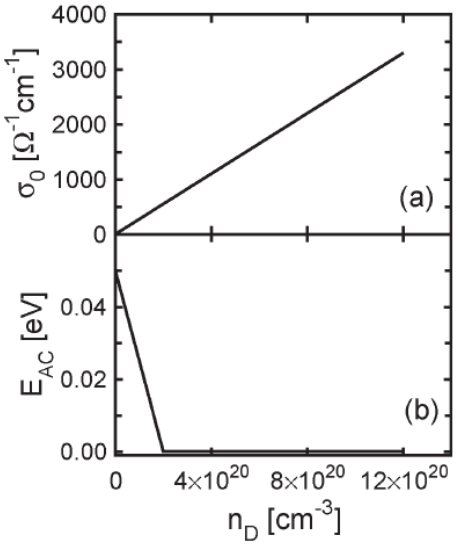
Oxygen vacancy filament conduction

- Oxygen vacancies influence conduction
  - Electron hopping from one vacancy to another
  - Act as local "doping" → thermally activated conduction
  - Create conductive defect band in Metal Oxide (e.g. at GB)

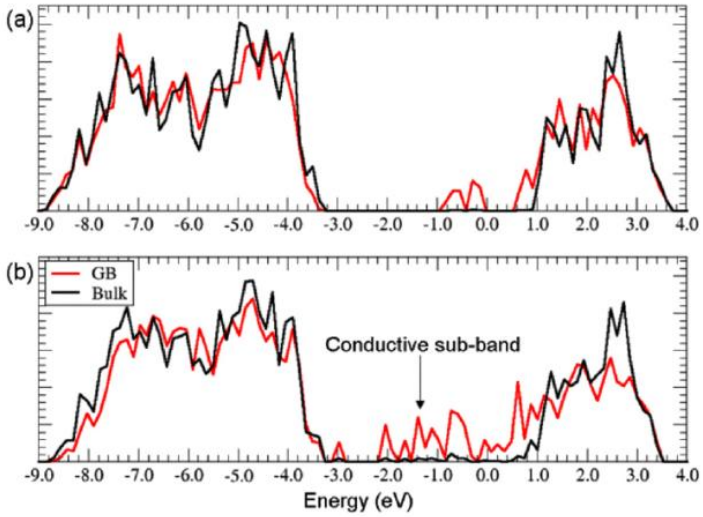
    → Metallic conduction



N.Xu et al,
VLSI Technology, 2008



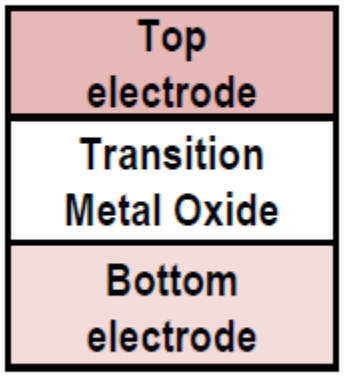
S.Larentis et al,
Trans. El.Dev. 59(9), 2012, p. 2468



G.Bersuker et al.,
J. Appl. Phys. 110, 124518 (2011)

Why Transition Metal Oxides?

- Transition metals, have 2 or multiple oxidation states
- Transition metal oxides are good ionic conductors. (Used in fuel cells for that reason)



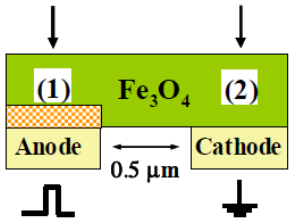


Figure 9 Cross-section of the lateral device with 2 bottom electrode to clarify the crystal structure detected from the surface of the switching film, using Raman microspectroscopy.

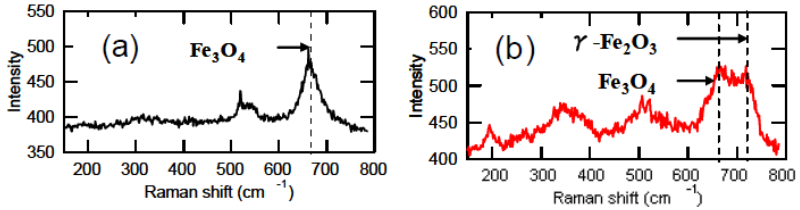
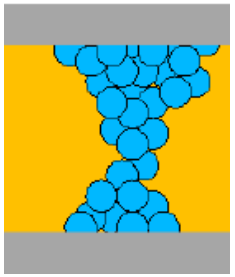


Figure 10 Raman spectra detected from the surface of the switching film. The (a) shows the spectrum for the region (1) before electroforming and (2) before and after electroforming. The (b) shows the spectrum for the region (1) after electroforming.

S.Muraoka et al., IEDM 2007

Switching Process

- Forming creates filament consisting of oxygen vacancies



= oxygen vacancy

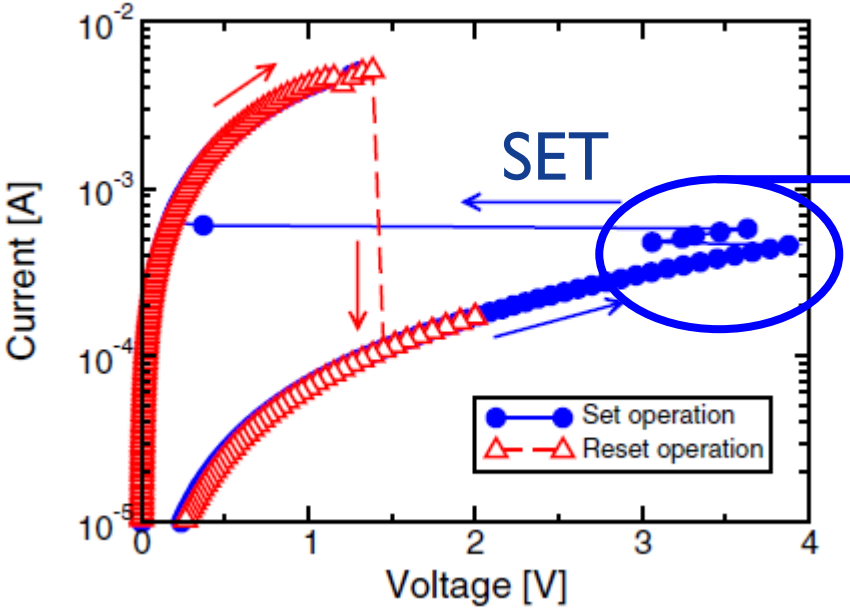
- RESET: local oxidation ; (Forming/)SET: local reduction

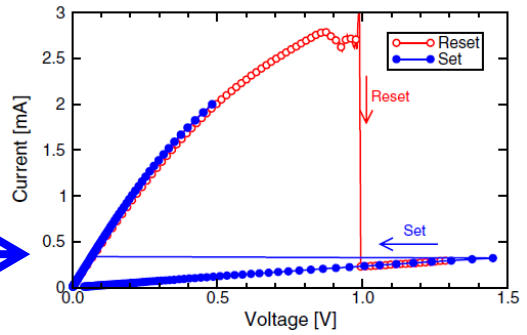
- How to explain process and unipolar character ?

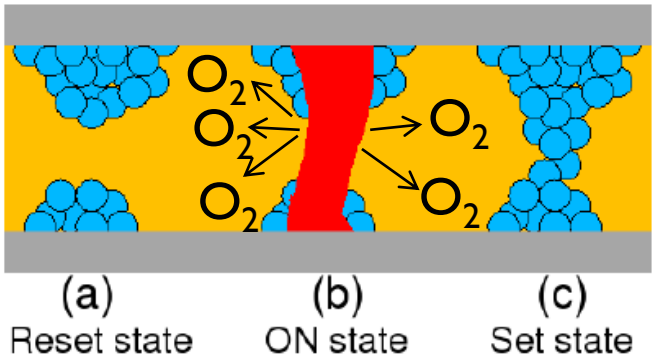
Unipolar SET process

Stage 1: high-field threshold switching → high current path
Stage 2: high current also induces Joule heating

High Field + high T: damage MOx (bond breaking/reduction)
→ permanent conductive path

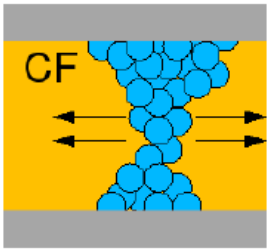




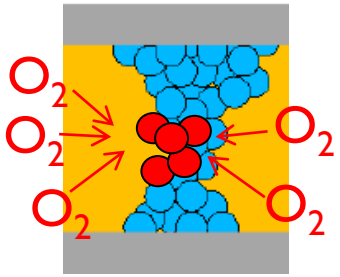


C.Cagli et al, IEDM 2008

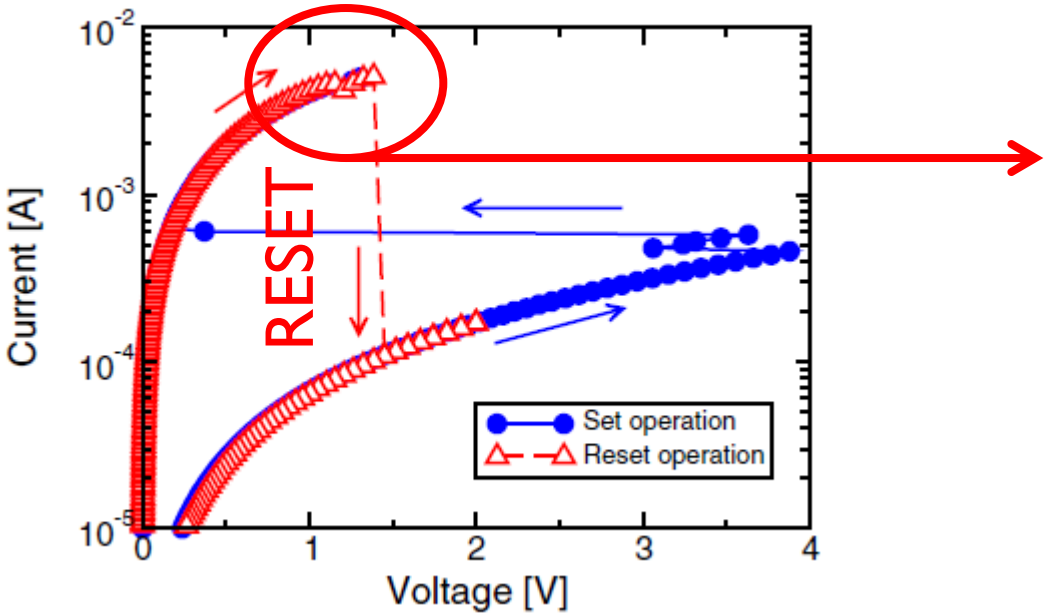
Unipolar RESET process

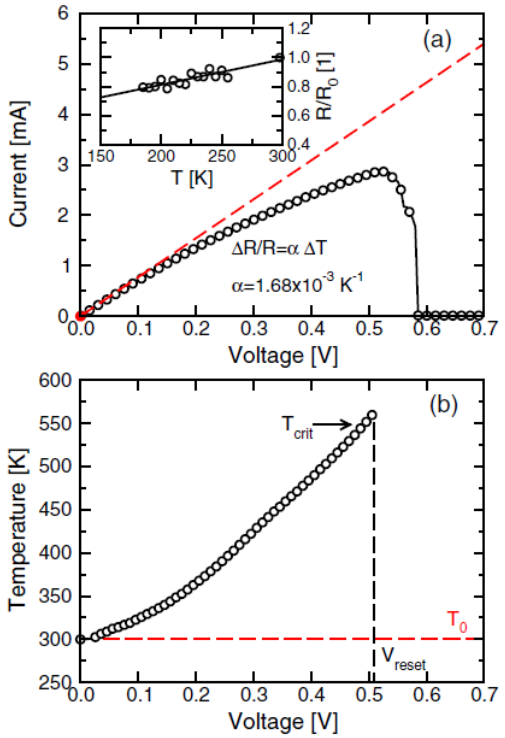


High (ON) current induces high T by Joule heating
Thermal oxidation "dissolves" of the filament



M (conducting)+O→ MO (insulating)





U.Russo et al, IEDM 2007

Why unipolar ?

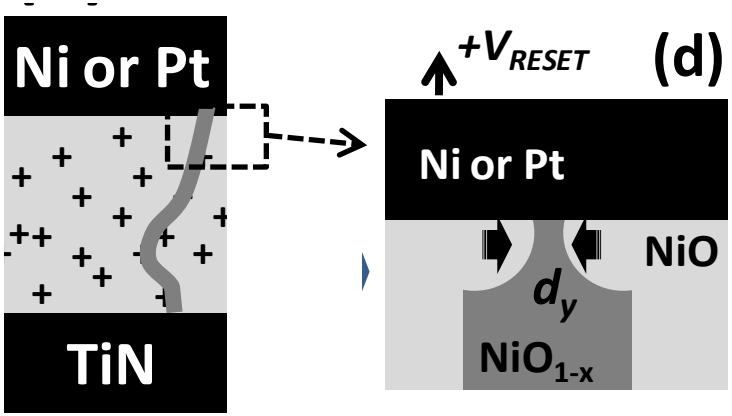
Non-directional mechanisms:

- temperature

- "BD" field

Anodic Oxidation @ "active" electrode

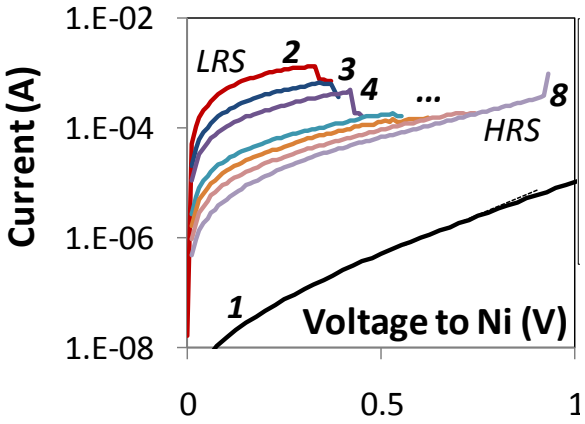
- Previous model does not take effect of electrodes into account
- **Actual switching requires "active" electrode**
  - Pt, Ni, ...
  - Active electrode catalyses anodic oxidation reaction during RESET
  - Filament "rupture" at active electrode interface and not at center as deduced from pure thermal simulations



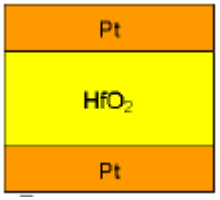
L.Goux et al,VLSI Technology 2011

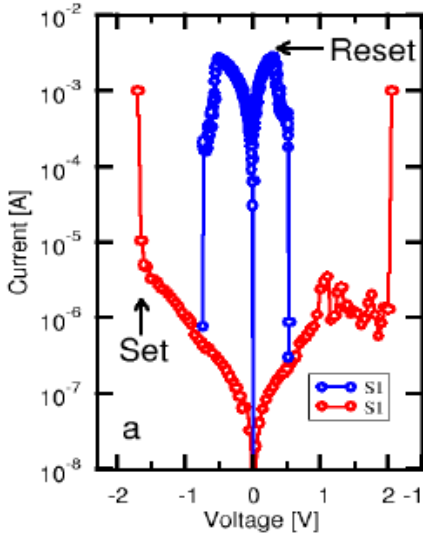
A-polar and Uni-polar switching

- Unipolar switching:
  - SET and RESET at SAME polarity
  - However, RESET needs specific polarity due to anodic oxidation
- Apolar switching:
  - Only in **symmetric structure** :
    - Active electrode as both bottom and top electrode



L.Goux et al,VLSI Technology 2011





A.Cagli et al, IEDM 2011

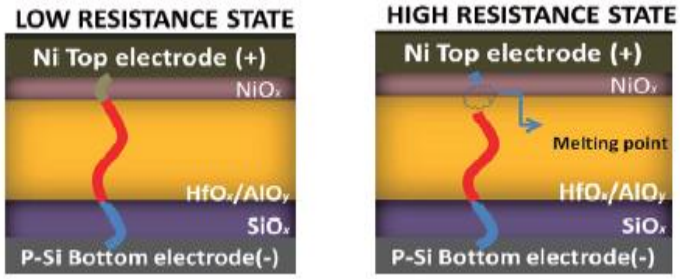
PRO/CON Unipolar switching

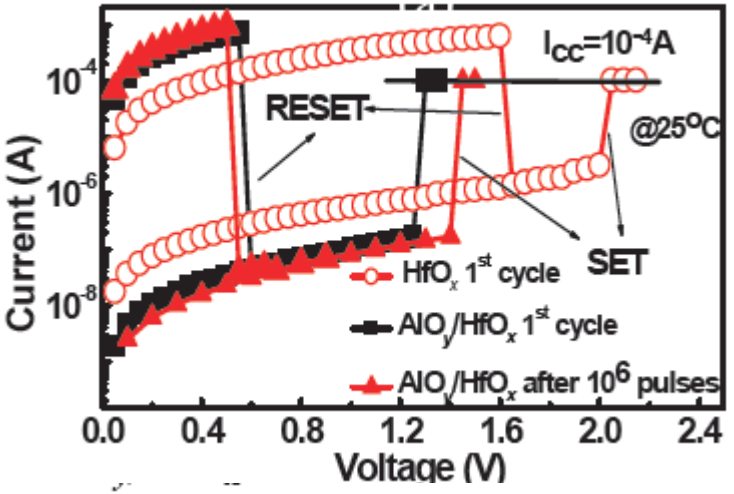
- Unipolar switching mechanism:
  - FORMING/SET : High Field activated reduction
  - RESET : High T induced local re-oxidation (Joule heating)
  - Oxygen diffuses "locally"

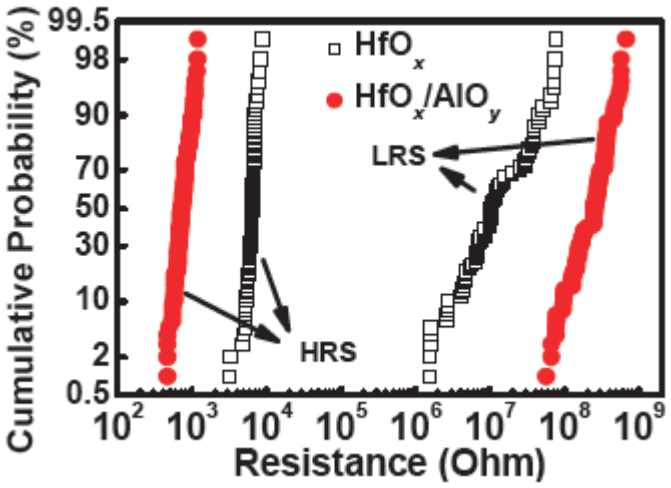
- High energy (thermal activated process, breakdown)
  - High V, I
  - Stronger filament "break" : higher R-window
- Loss of oxygen : diffusion is not very directional
  - Limited cyclability
- 1 voltage polarity :
  - use of simple DIODE as selector : 1D1R cell

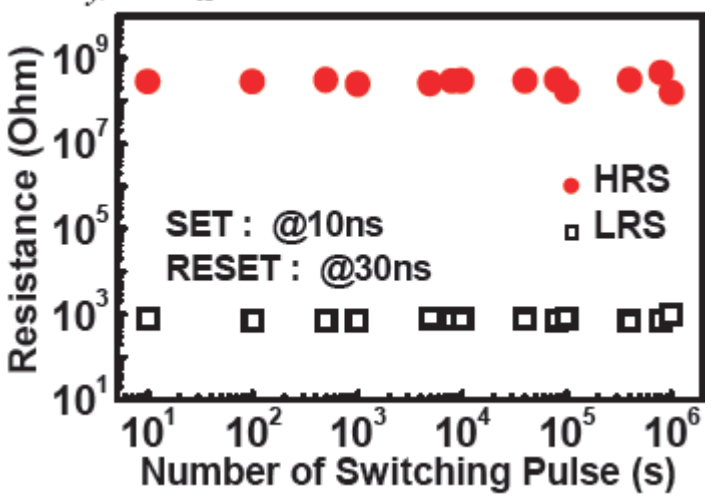
State of the art.../1 typical results

"High Performance Unipolar AlOy/HfOx/Ni based RRAM Compatible with Si Diodes for 3D Application", X.A. Tran, VLSI Technology 2011

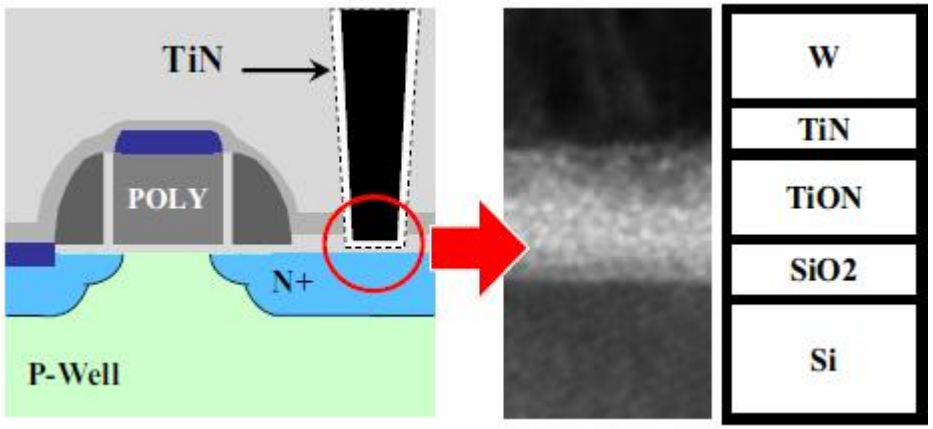








State of the art.../2. low current results



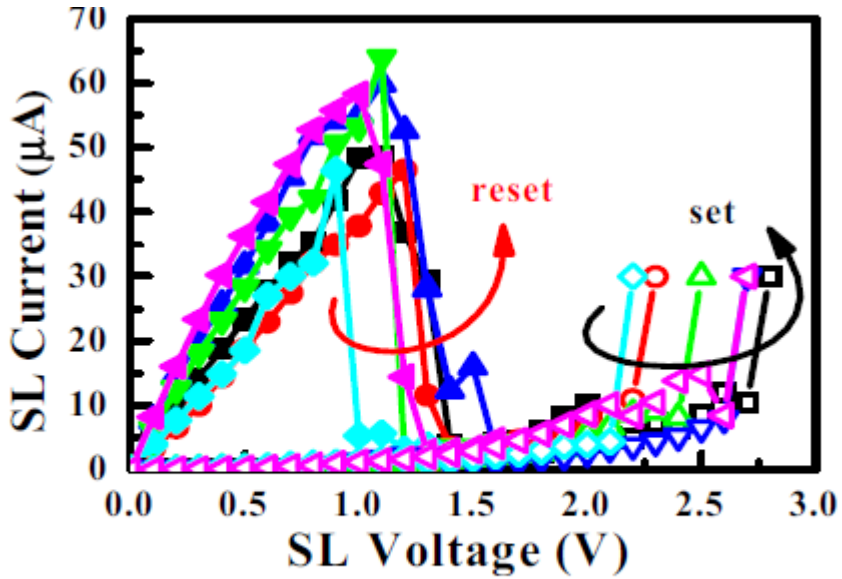
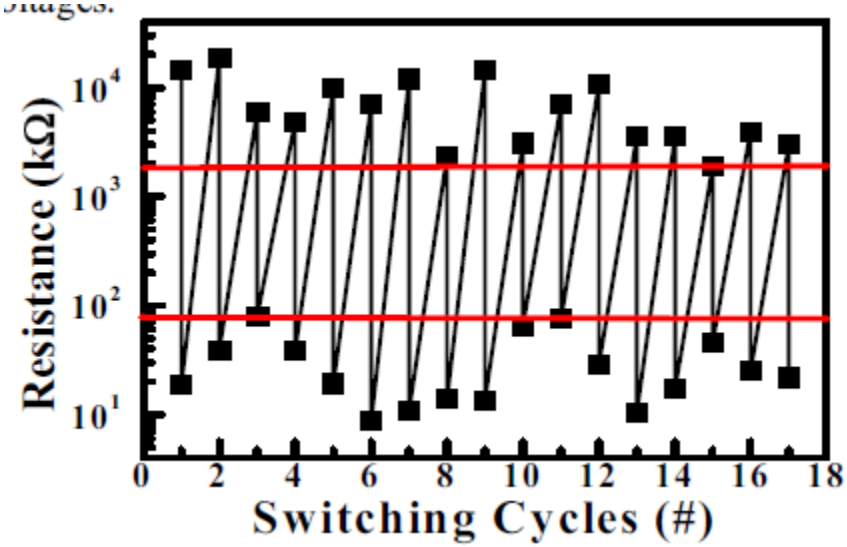


Figure 4 The DC-IV characteristics of two reproducible resistance states.

Y.-H.Tseng et al, IEDM 2009

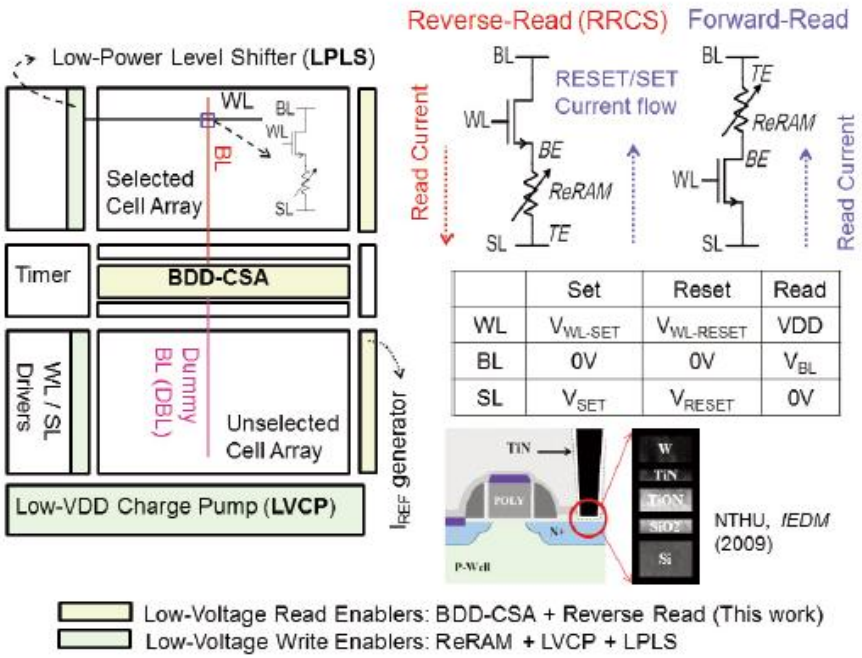


Low current but at expense of window and extreme poor cyclability

NTHU/TSMC ISSCC 2012 ITIR

A 0.5V 4Mb Logic-Process Compatible Embedded Resistive RAM (ReRAM) in 65nm CMOS Using Low-Voltage Current-Mode Sensing Scheme with 45ns Random Read Time

Unipolar



	Set	Reset	Read
WL	V_{WL-SET}	$V_{WL-RESET}$	VDD
BL	0V	0V	V_{BL}
SL	V_{SET}	V_{RESET}	0V

Figure 25.7.1: Block diagram and cell structure of the low-voltage ReRAM macro.

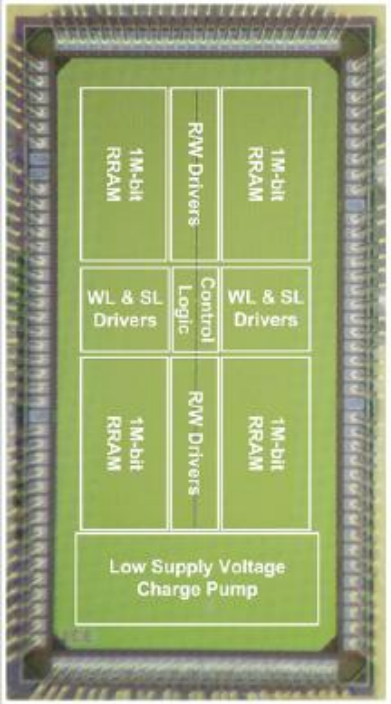


Figure 25.7.7: Measured results.

Technology	TSMC 65nm CMOS Logic Process
Capacity	4Mb (4 x 1Mb)
ReRAM Device	VSET= 2V VRRESET=1.5V
Sub-array	1024 columns x 512 rows
VDD	Write: 0.48V~1V Read: 0.32V~1V
Testchip Size	4.74mm^2
Testchip Read Power (include Testchip buffers)	0.5mA at VDD=0.5V
Low-Voltage Charge-Pump (LVCP)	Min. Vin = 0.45V at Vout=2V
Low-Power Level-Shifter (LPLS)	Min. Vin = 100mV at Vout=2V

NTHU/TSMC ISSCC 2012

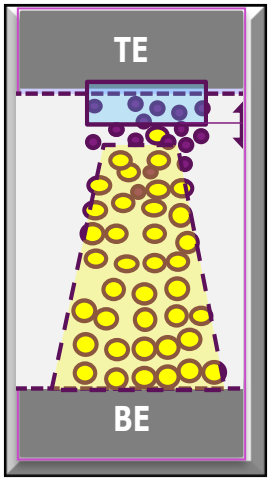
RRAM : classification & materials

- RRAM : general definitions & some history...
- Classification
- Filamentary switching
  - Properties of filamentary switching
  - Thermo-chemical RRAM
  - **Bipolar "oxygen vacancy drift" RRAM**
  - Electro-chemical CBRAM
- Interfacial switching

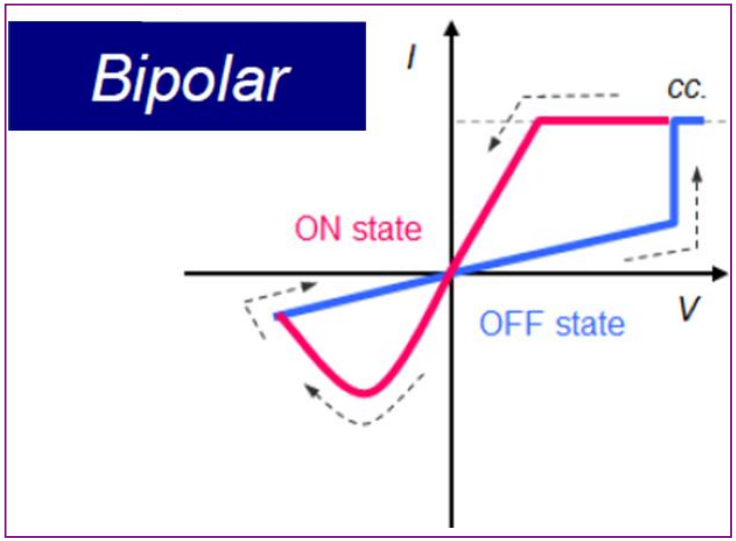
Bipolar Switching OxRRAM : "Oxygen Vacancy Migration"

1D
Filamentary

Oxygen vacancy migration

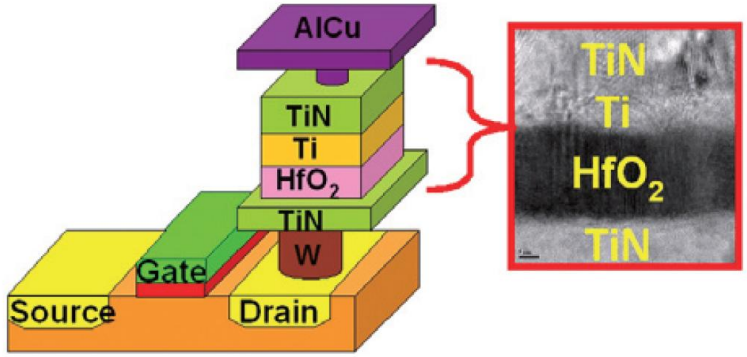


BIPOLAR



Material : TMO's , e.g. HfO, TiO, TaO..

H.Y.Lee et al, "Low Power and High Speed Bipolar Switching with A Thin Reactive Ti Buffer Layer in Robust HfO_2 Based RRAM", IEDM, Tech. Dig., pp. 297, 2008

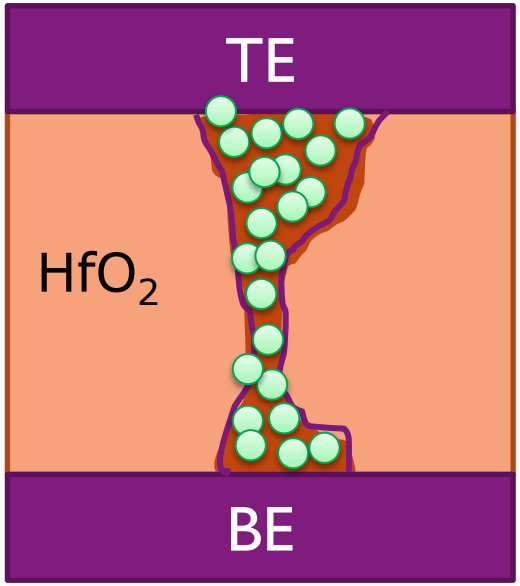


Bipolar vs unipolar switching OxRRAM

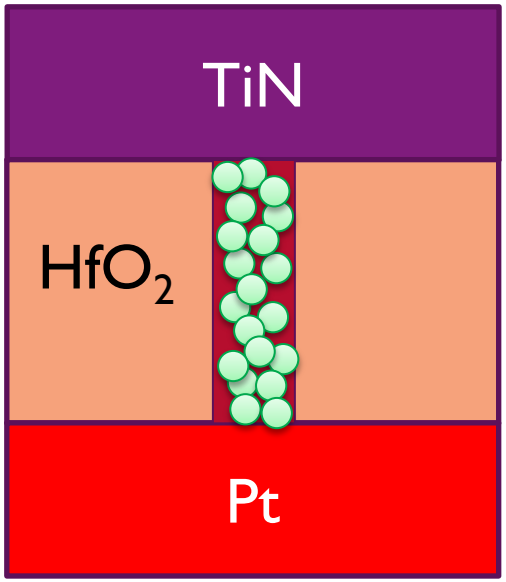
- Same TMO-based RRAM cells ?
  - Requirement for bipolar switching = asymmetric structure
- Type I : cells with one "active" electrode :
  - Show both unipolar and bipolar switching
- Type II: cells with asymmetrically built-in oxygen vacancies
  - Cells show bipolar switching

Mechanism ?

- Focus here on HfO_2 based RRAM



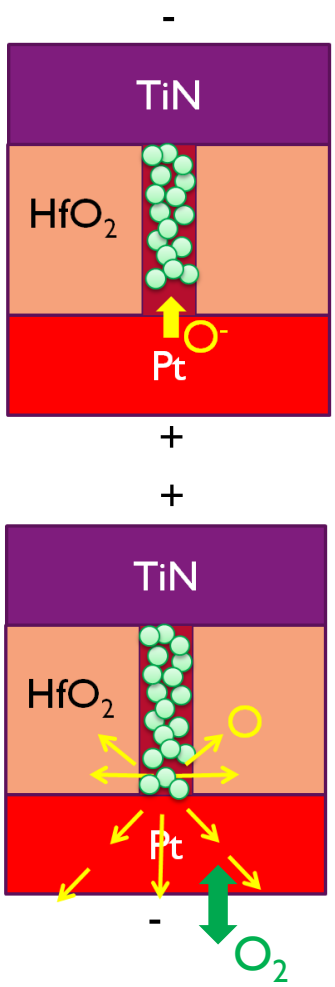
1. "Active electrode" based HfO_2 RRAM



- Structure:
  - Stoechiometric HfO_2 with one catalytic active electrode (e.g., Pt), and one neutral electrode (e.g., TiN)
- Forming:
  - BOTH generation of oxygen vacancies AND filament formation
  - High forming voltage (>3V, 5nm HfO2 films)

L.Goux et al., On the Gradual Unipolar and Bipolar Resistive Switching of TiN\HfO2\Pt Memory Systems, Electrochemical and Solid-State Letters, 13 6 G54-G56 2010

1."Active electrode" based HfO_2 RRAM

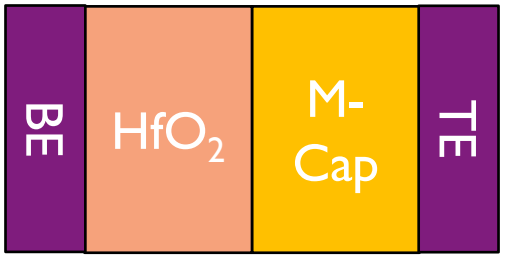


- Reset : anodic oxidation
  - Requires positive voltage at active electrode
    - re-oxidation of filament at Pt anode interface [1]
    - Oxygen supply from active electrode
- Set :
  - Vacancy creation + thermal assisted outdiffusion & drift of oxygen
- No closed system:
  - Generation/recombination of oxygen vacancies
    - Main mechanism = transport of Oxygen
    - atmosphere effects [2]
- **Main difference with unipolar operation**
  - Drift-assisted motion of charged oxygen species results in improved cyclability

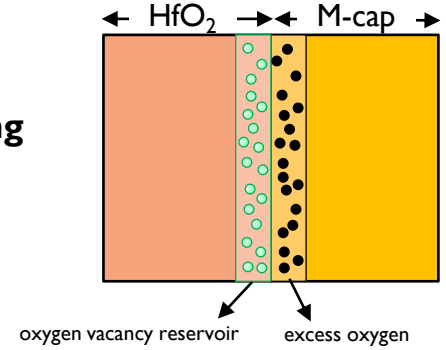
[1] L.Goux et al., *Electrochemical and Solid-State Letters, 13 6 G54-G56 2010*
[2] L.Goux et alAPPLIED PHYSICS LETTERS 97, 243509 2010

2. "Oxygen vacancy drift" based RRAM

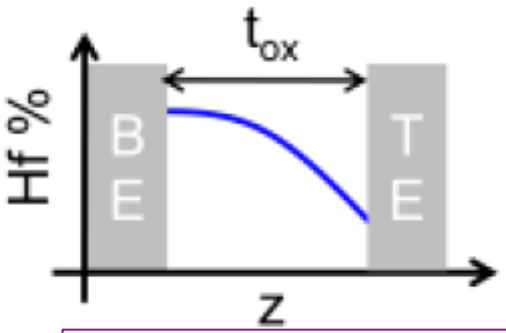
Stack



After processing



- **Controlled** introduction of oxygen vacancy by **process**
  - Oxygen scavenging metal cap layer on top of stoechiometric HfO_2 (ALD)
    - Ti, Hf, Ta,....
    - Local formation of $HfO_{2-\delta}$
  - Deposition of substoichiometric HfO_x (PVD)



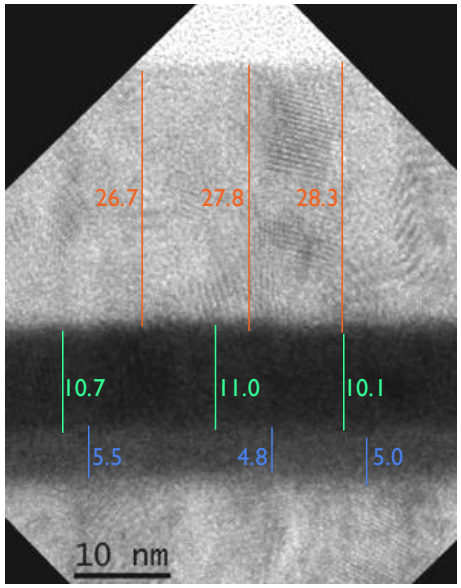
- Need for **asymmetric** profile of oxygen vacancies
  - Otherwise competing switching layers [1]

F.Nardi et al, "Complementary switching in metal oxides: toward diode-less Xbad RRAMs", IEDM 2011

Evidence of O migration in Hf CAP

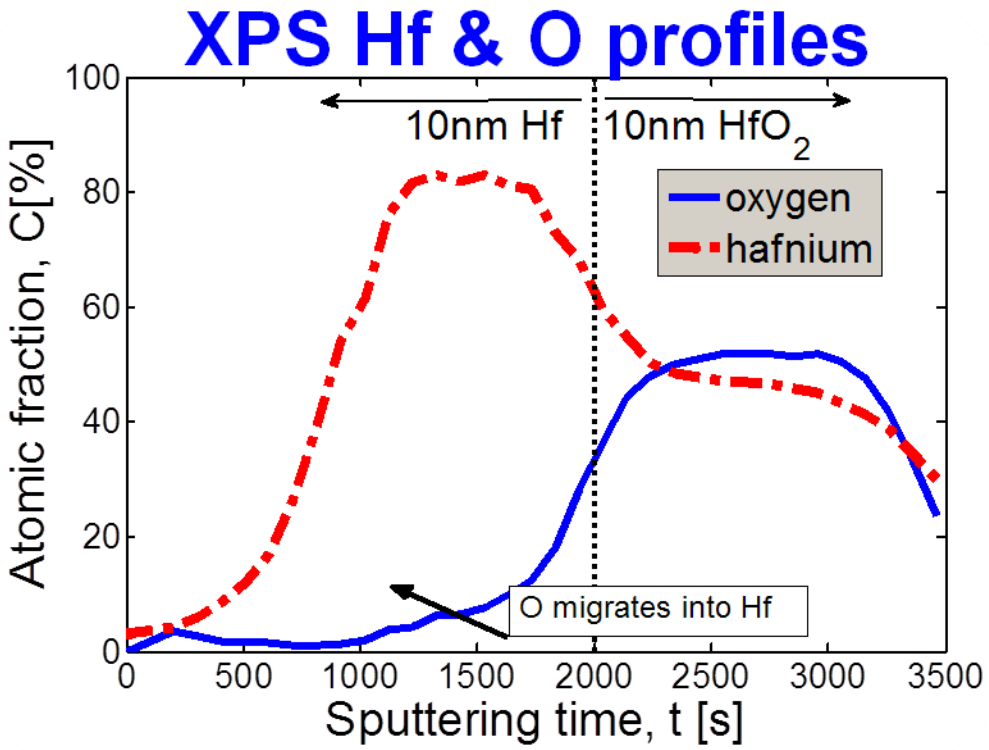
(10nm) Hf

(5nm) HfO_x



[*Govoreanu et al, SSDM2011*]

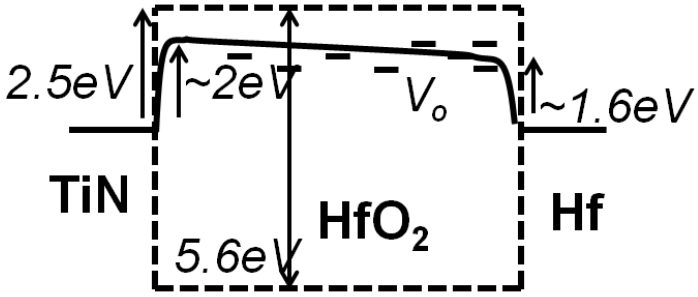
Amorphous Hafnia



B.Govoreanu et al, IEDM 2011

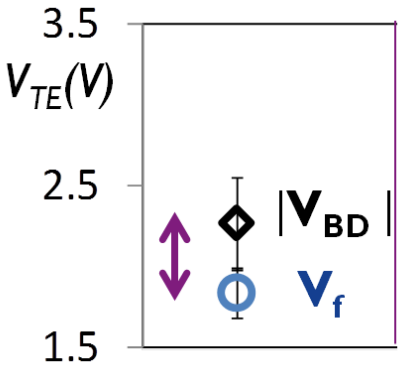
Evidence for asymmetric V_O profile

- Difference in TE/BE barrier height depending on local [V_O]



Internal Photoemission measurements – L. Pantisano et al., Microel. Eng. 88(2011)

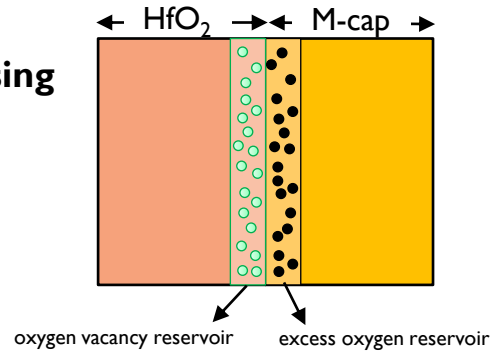
- Difference in positive Forming voltage and negative Breakdown voltage



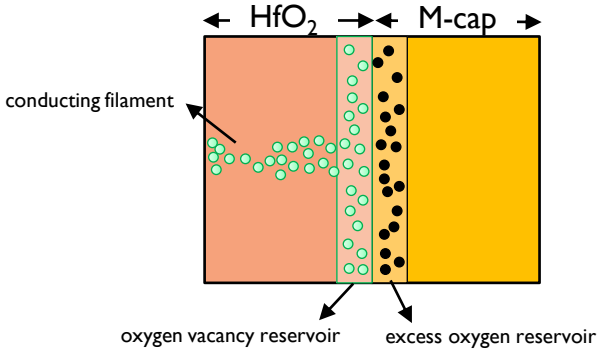
L.Goux et al,VLSI 2012

2. "Oxygen vacancy drift" based RRAM

After processing

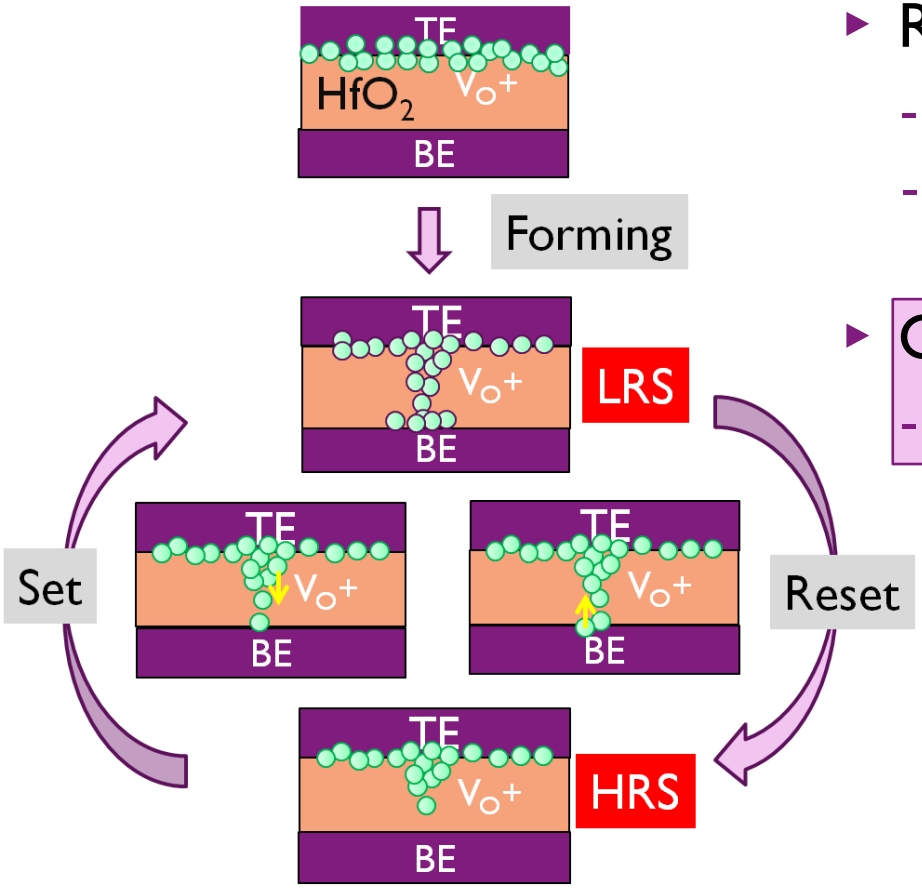


After forming



- Forming:
  - Main effect = filament formation ONLY
    - (limited creation of additional V_O)
  - Reduced forming conditions (<2V for 5nm HfO_2 films)
  - Polarity effect

2. "Oxygen vacancy drift" based RRAM



- Reset/Set :
  - Transport = drift of oxygen vacancies
  - Filament constriction shrinks/expands with drift of oxygen vacancies up/down
- Closed system:
  - NO Generation/Recombination of V_O

Above is "intuitive model"
→ more detailed discussion of operation mechanisms follows later !

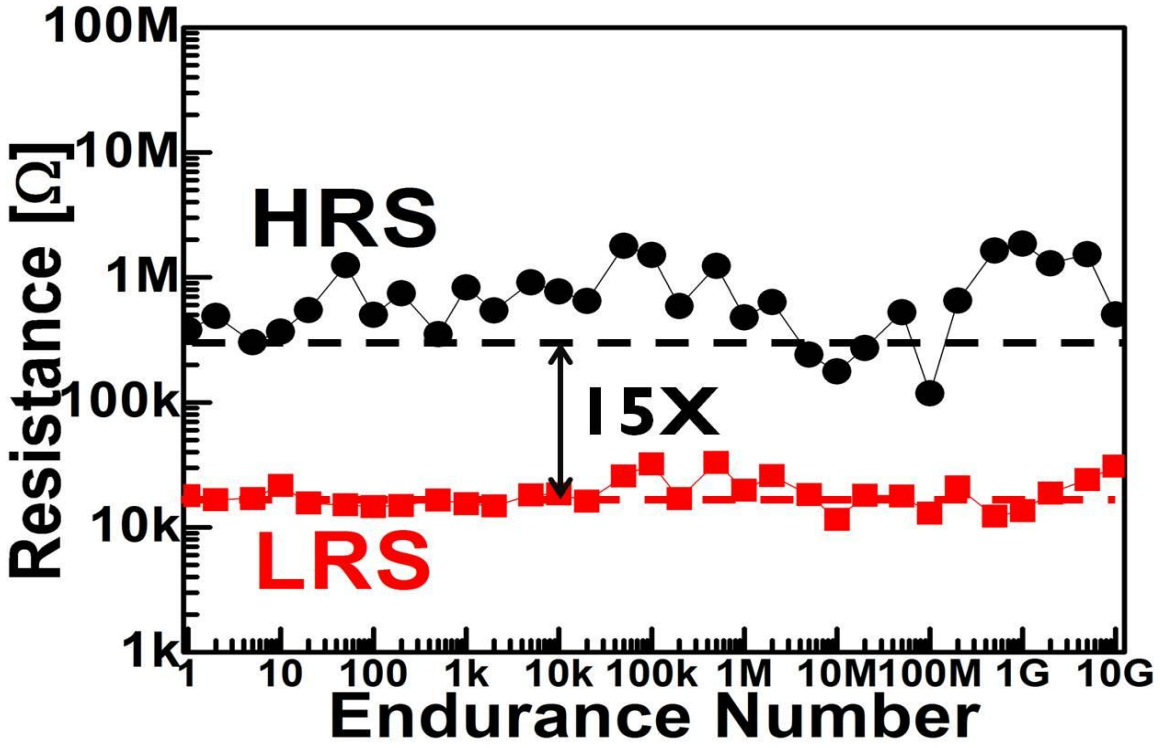
Comparison

	Active Electrode	V_O Drift
Filament	Oxygen Vacancies	Oxygen Vacancies
Generation of V_O	Forming	Process
Forming (5nm HfO_2)	High V (>3V)	Low V (<3V), tunable
Reset	Catalytic oxidation of filament	Filament narrowing
Defect model	Oxygen diffusion & drift Generation/ Recombination of V_O	Drift of V_O
System	Open (loss of O)	Closed (no V_O G/R)
Cyclability	Limited	High

Only "V_O drift" RRAM further discussed

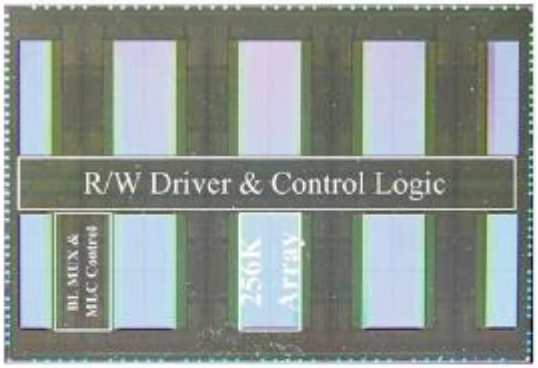
>10^{10} Cyclability of HfO_2 RRAM

Y.Y.Chen, (imec) accepted for TED 2012



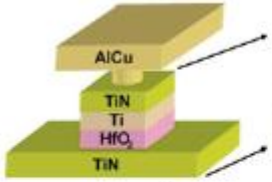
By balancing the SET pulse WL=1V, BL=1.8V, 5ns and RESET pulse WL =3V, SL=1.8V, 10ns, 10^{10} pulse endurance could be achieved on 40nm Hf/HfO_2 1T1R devices.

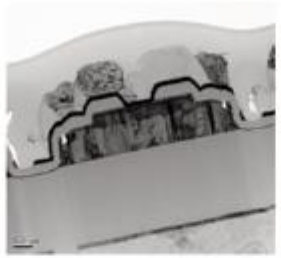
HfO_2 RRAM demonstrator

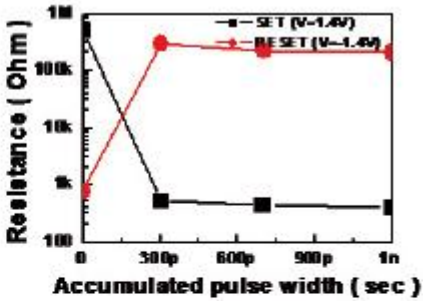


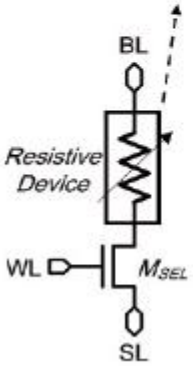
Process	CMOS: 0.18um 1P4M RRAM: 0.64um x0.48um
Memory Capacity	4Mb (32 x 128Kb sub-blocks)
Chip size	11310um x 16595um (with test-mode circuits)
Device	HV path: 3.3V device Cell array: 3.3V device Peripheral: 1.8V device
VDD	HV path: 3.3V Core: 1.8V
Read-Write Access Time (SLC-mode)	Random access: 7.2ns Burst-mode: 3.6ns

A 4Mb Embedded SLC Resistive-RAM Macro with 7.2ns Read-Write Random-Access Time and 160ns MLC-Access Capability

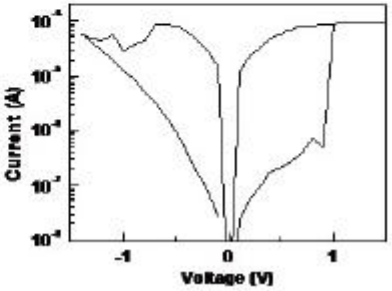








	SET	RESET	Read
WL	V_{G_SET}	VDD	VDD
BL	V_{SET}	0	V_{BLR}
SL	0	V_{RESET}	0
State	LRS (R_L)	HRS (R_H)	'1' / '0'



NTHU/ITRI ISSCC 2011 1T1R

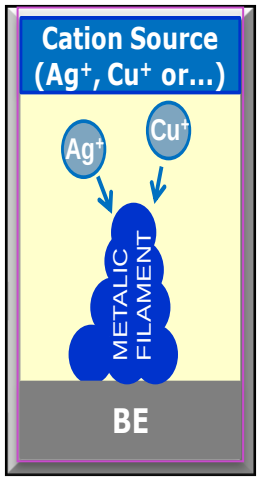
RRAM : classification & materials

- RRAM : general definitions & some history...
- Classification
- Filamentary switching
  - Properties of filamentary switching
  - Thermo-chemical RRAM
  - Bipolar "oxygen vacancy drift" RRAM
  - **Electro-chemical CBRAM**
- Interfacial switching

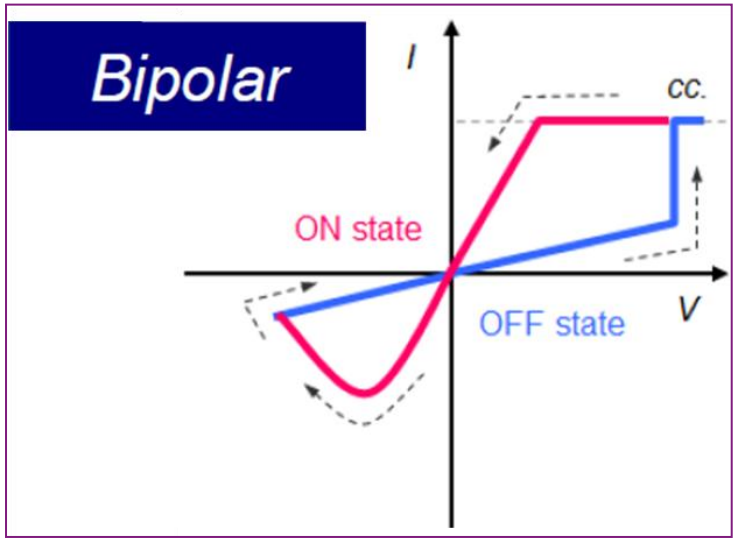
Conductive Bridge RRAM : "Programmable Metallization Cell"

1D
Filamentary

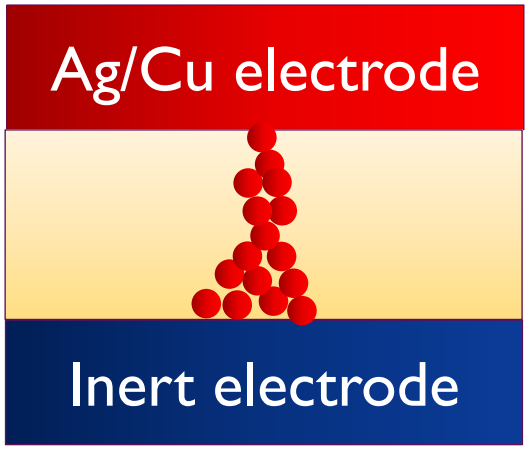
Electro-chemical



BIPOLAR

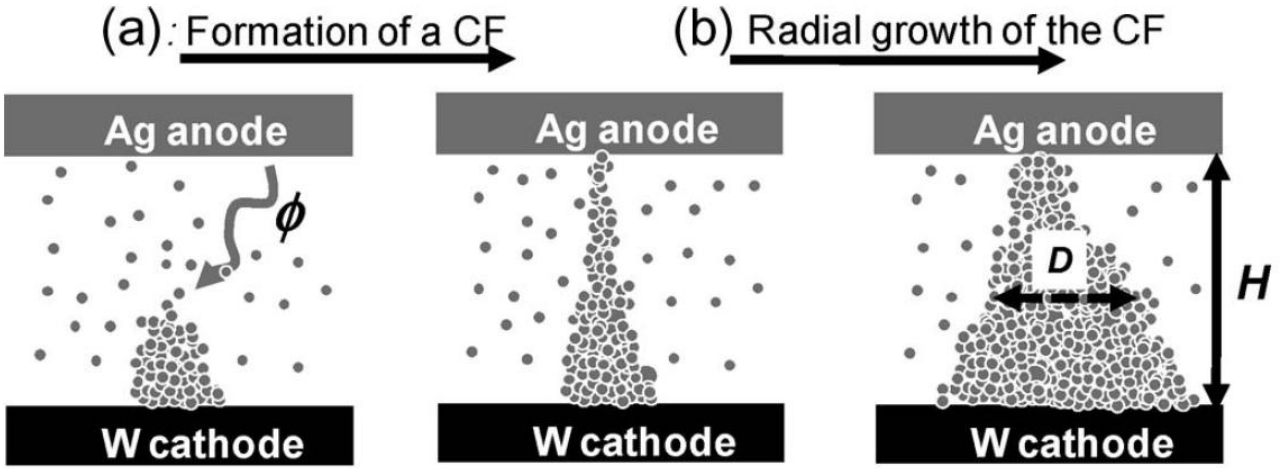


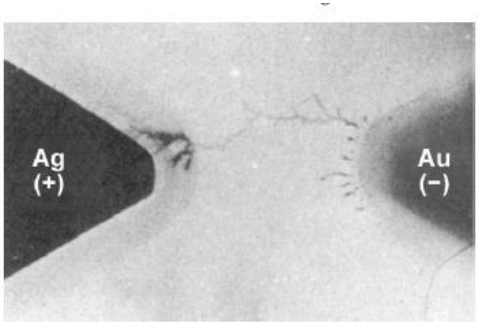
Material :
Ag or Cu based



Electrochemical filament formation

- Oxidation at anode: forming of metal ions ($Ag \rightarrow Ag^+ + e^-$)
- Drift of metal ions through insulating switching layer
- Reduction at cathode: plating out of metal ions ($Ag^+ + e^- \rightarrow Ag$)
  - Growing filament forms "virtual cathode"

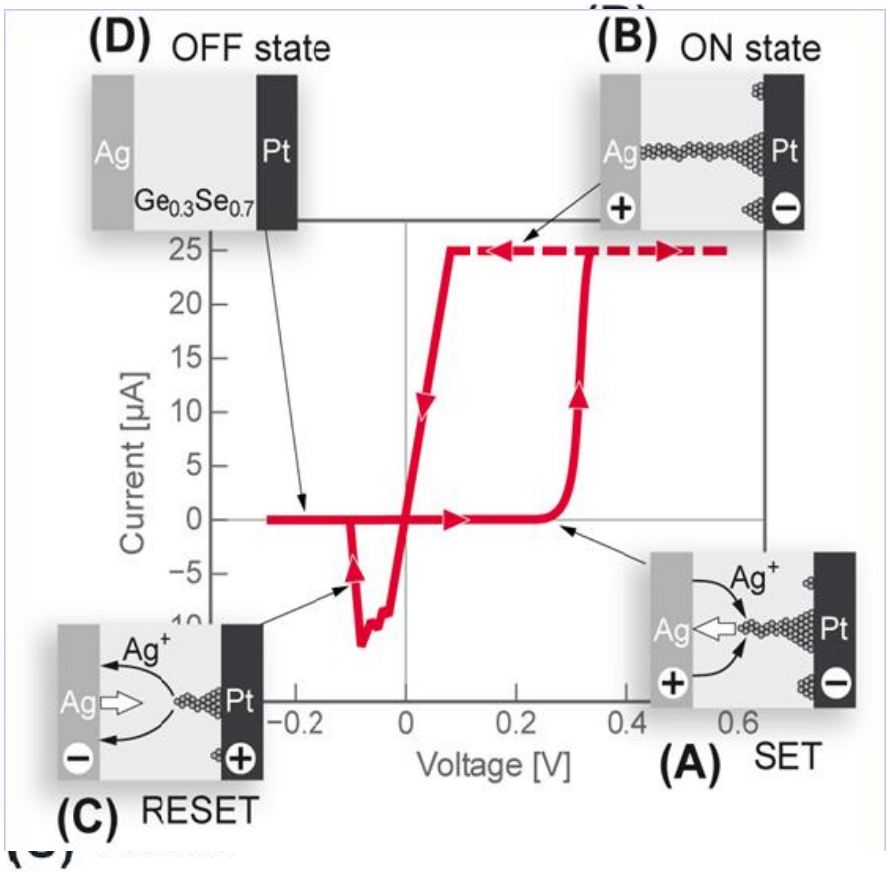




Rainer Waser et al., Adv. Mater. 2009, 21, 2632–2663

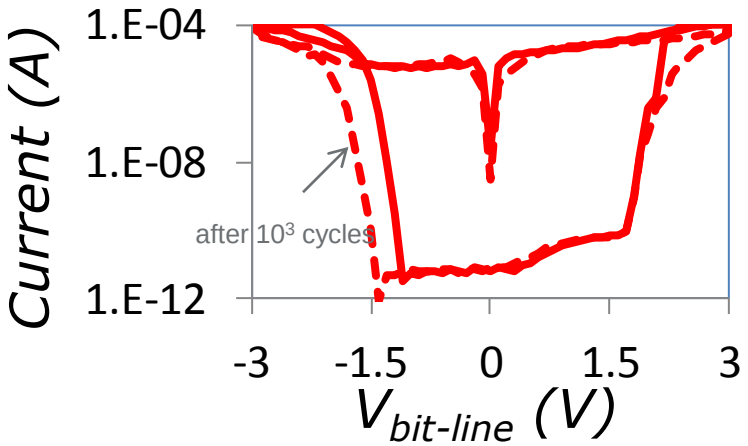
U. Russo et al., IEEE TRANSACTIONS ON ELECTRON DEVICES, 56(5), p. 1040, 2009

Bipolar Switching



Asymmetric switching
→VRESET < VSET

Deep RESET
~ complete filament annihilation?



C. Schindler et al., IEEE T-ED, 54 (2007) 2762

L.Goux et al., VLSI Technology 2012

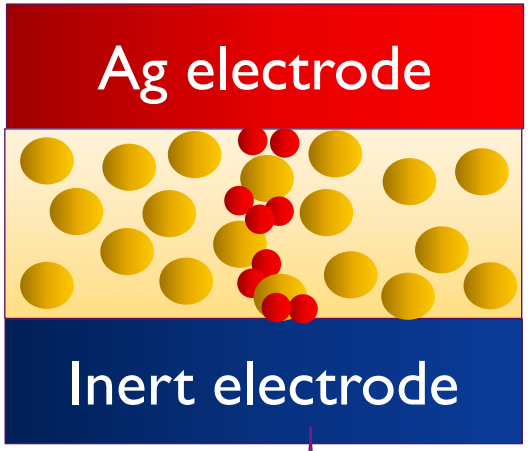
Materials and Structures

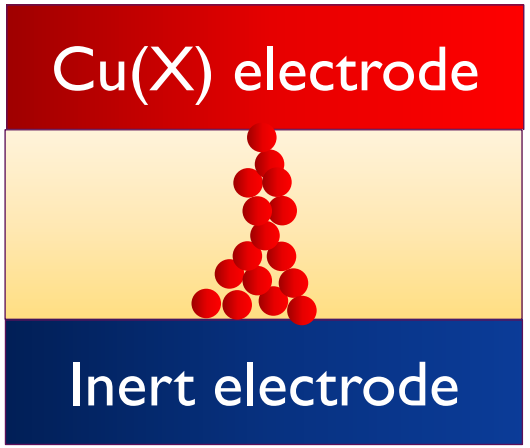
1st generation : **Ag-doped chalcogenide**
All-in-one, non-homogeneous material

2nd generation: **Metal-Oxide**
Cu source separated from switching layer

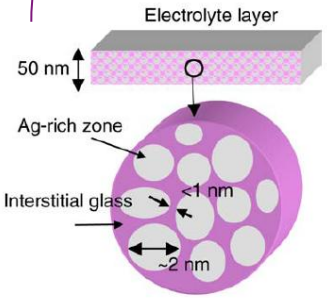
Ge_xSe matrix

Ag_2Se nanoparticles

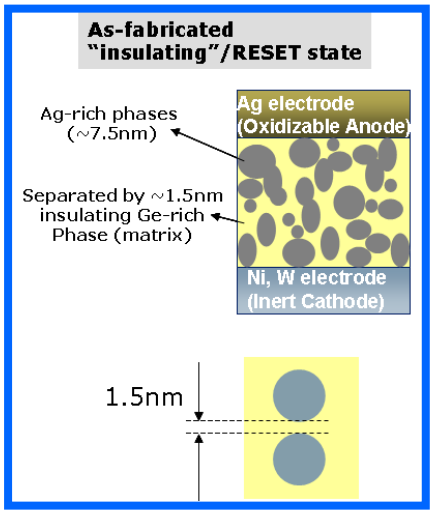


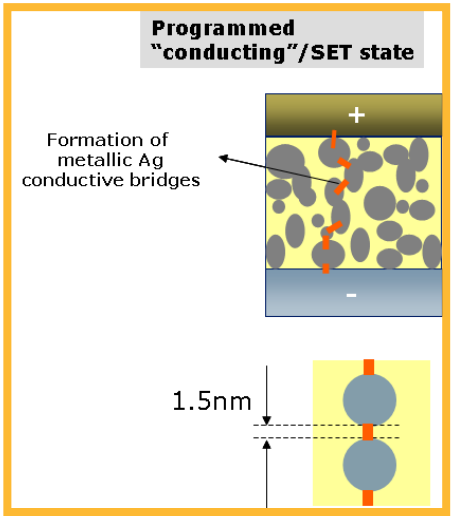


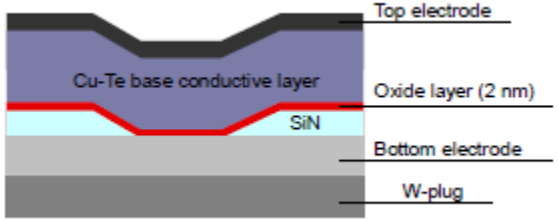
Metal-oxide matrix



[1] M.Kozicki, IEEE Trans. On Nanotechnology 4(3), 331 (2005)



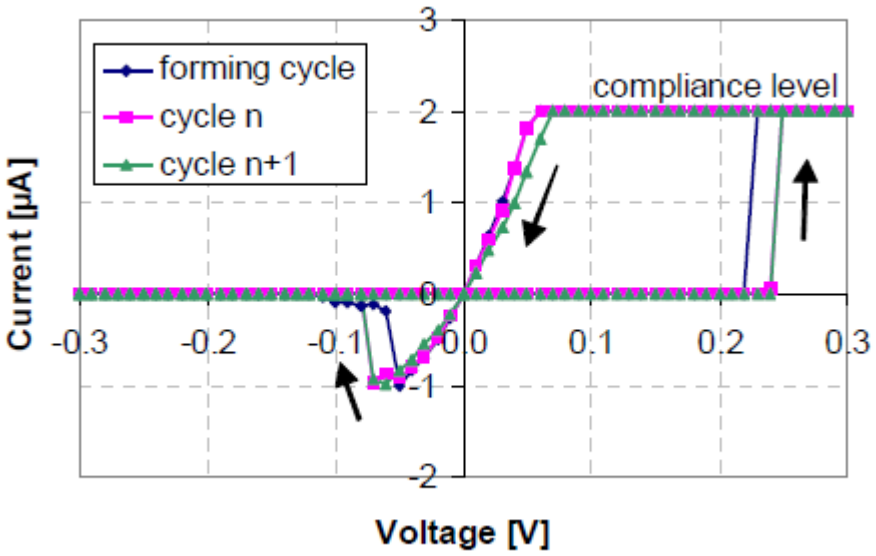




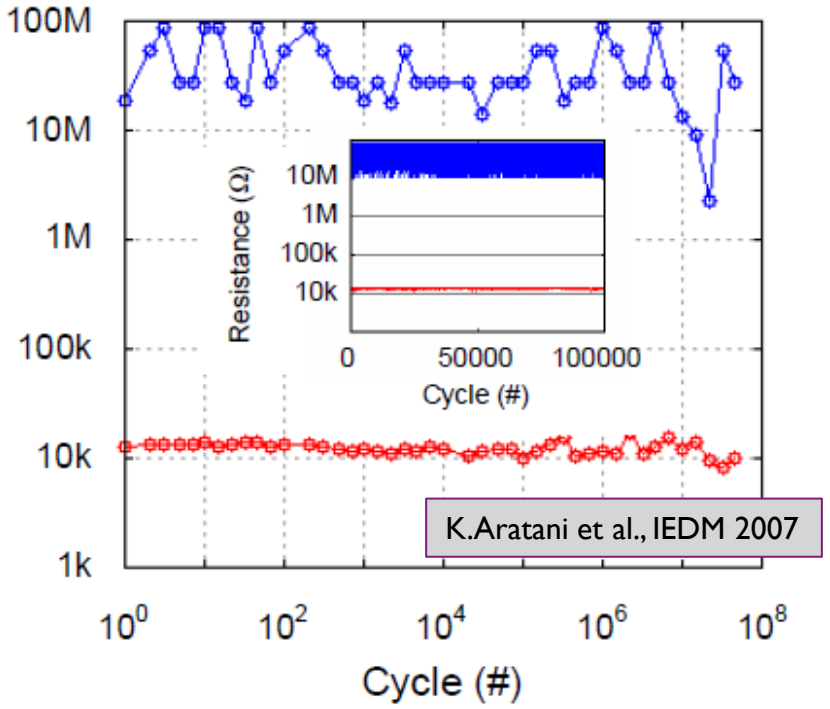
K.Aratani et al., IEDM 2007

PRO/COM OF CBRAM

- Combines high resistance window with low current operation
- Good cyclability (>10^8 cycles)
- Limited thermal stability of material and control of Cu diffusion
  - Process T and High-T retention issue
- Low RESET voltage (disturb)



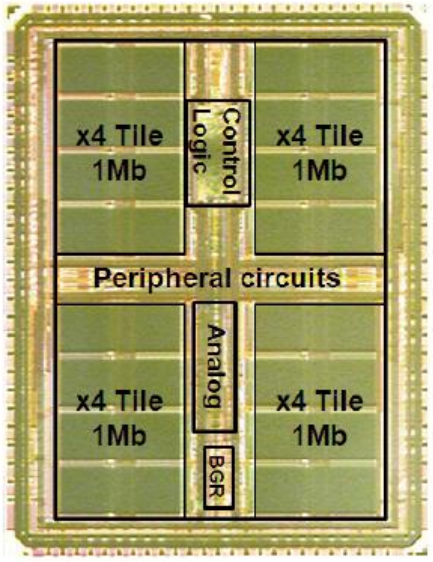
M.Kund et al., IEDM 2005



K.Aratani et al., IEDM 2007

SONY ISSCC 2011 CBRAM 1T1R

A 4Mb Conductive-Bridge Resistive Memory with 2.3GB/s Read-Throughput and 216MB/s Program-Throughput



Capacity	4 Mb
Tile	256Kb
Process	180nm CMOS
Chip size	6.8x5.26mm 35.8 mm²
Cell architecture	1T-1R
Cell size	2.24 μm²
Power Supply	3.3 V,1.8 V
Memory / IF clock	125MHz
Read Size, Throughput	128Byte 2.3GB/s
Program Size, Throughput	16Byte 216MB/s

Figure 11.7.1: Die micrograph and features.

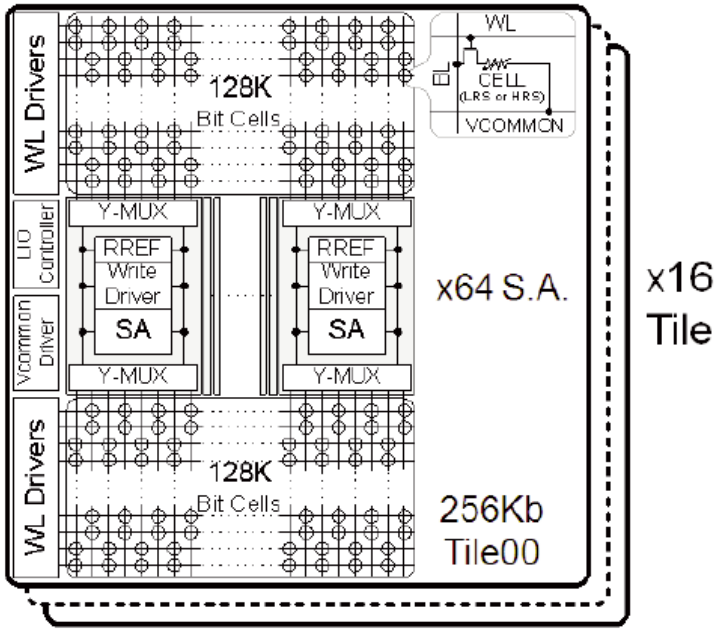
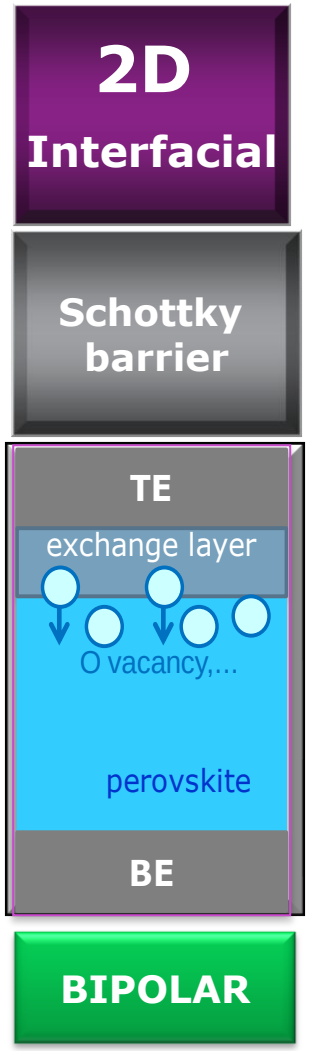


Figure 11.7.2: Array organization.

RRAM : classification & materials

- RRAM : general definitions & some history...
- Classification
- Filamentary switching
  - Properties of filamentary switching
  - Thermo-chemical RRAM
  - Bipolar "oxygen vacancy drift" RRAM
  - Electro-chemical CBRAM
- **Interfacial switching**

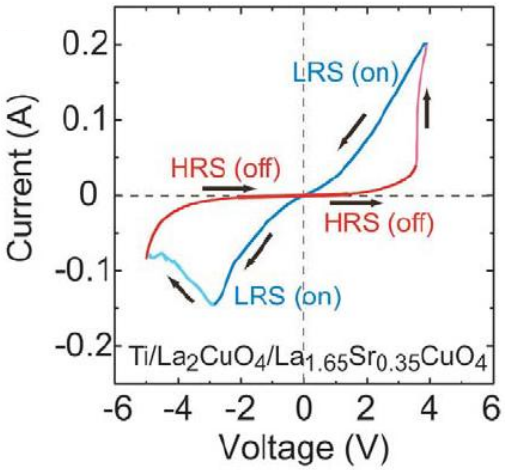
2D switching RRAM

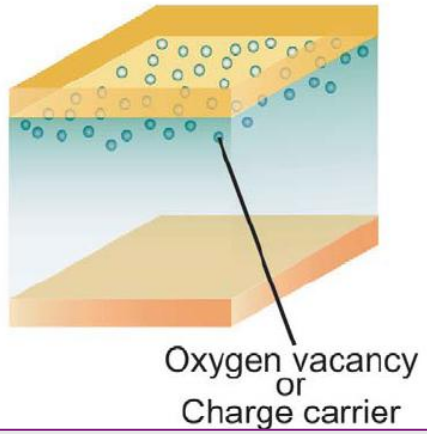


Material :

complex oxides
(doped perovskites)

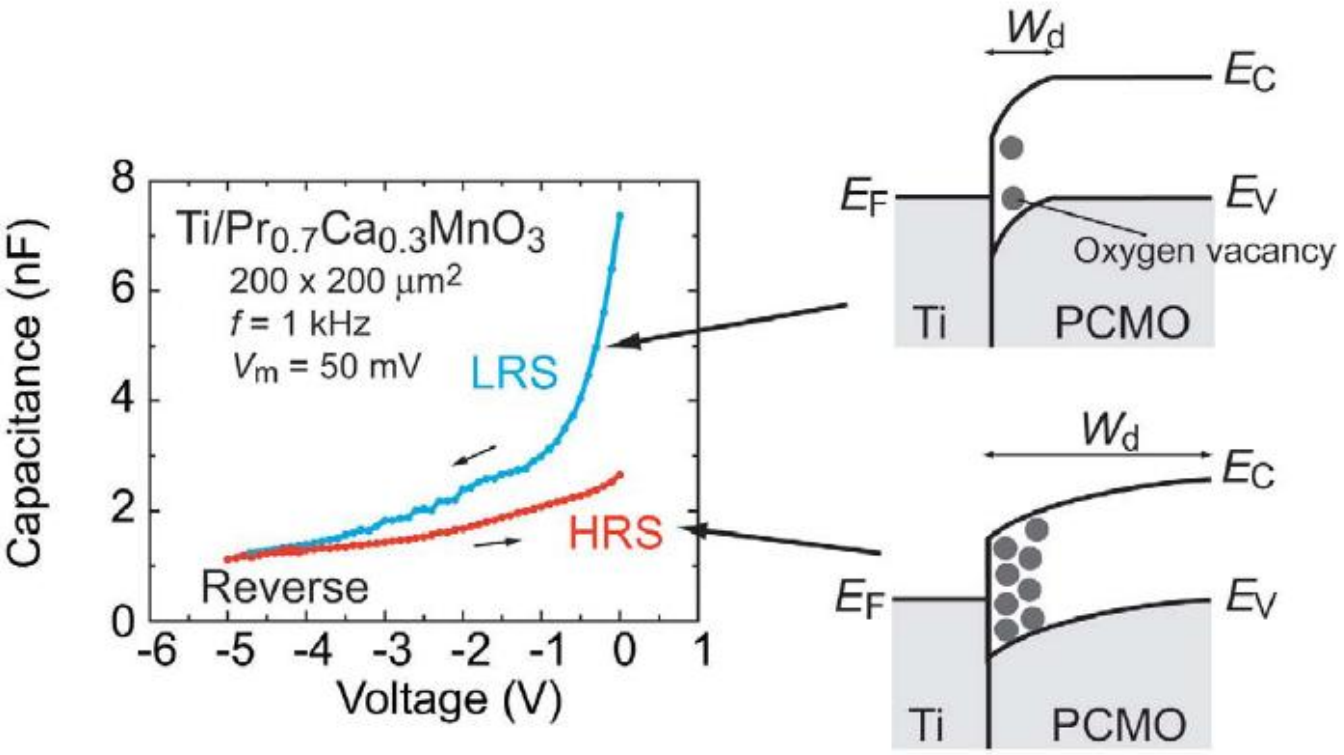
noble (Pt) electrode





Akihito Sawa, Materials Today 11(6) p.28 2008

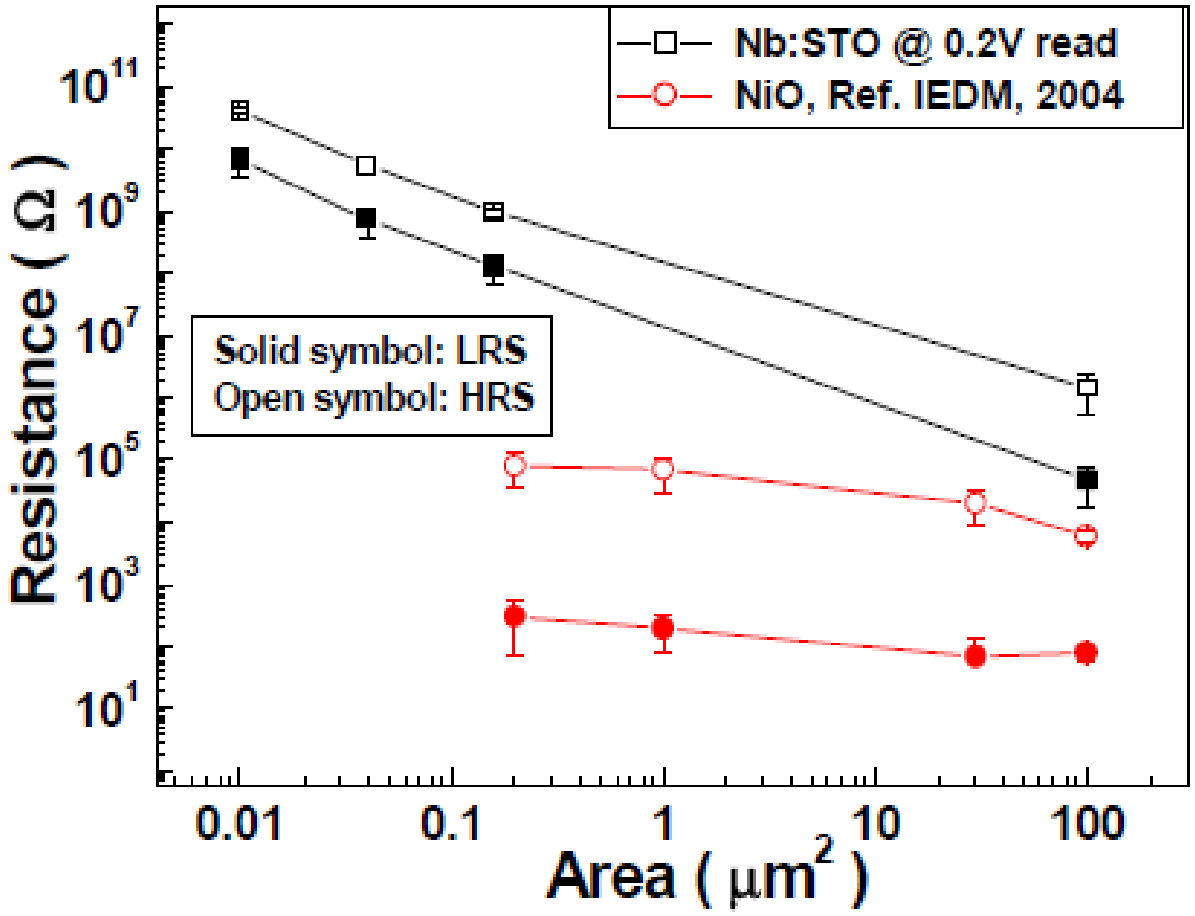
Mechanism: modulation of Schottky barrier



Akihito Sawa, MaterialsToday 11(6) p.28 2008

by moving oxygen vacancies to or from the interface

Area scaling as fingerprint of 2D switch



H.Sim et al., IEDM 2005

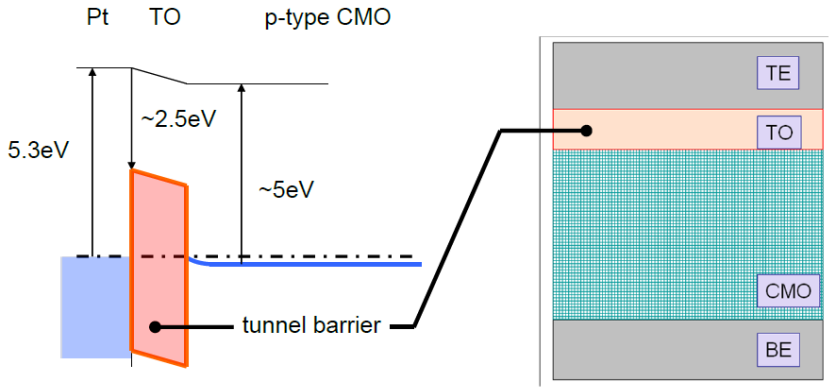
PRO/CON 2D Interfacial Switching

- Materials :
  - Complex perovskite oxides : process (in) compatibility ?
  - Pt electrode required for good Schottky barriers
- Thick films :

  - may compromise scaling
- Asymmetry and Non-linearity of LRS I-V behavior:
  - Suitable for Self Rectifying Cell

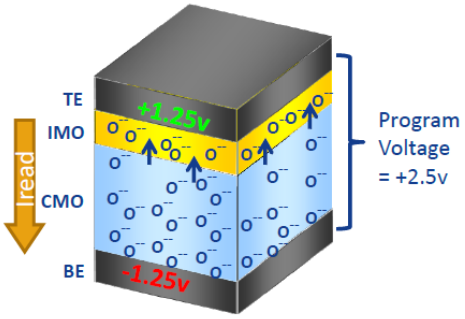
Interfacial switching key for Self Rectifying Cell...

Current limited by QM tunneling through tunneling layer
Barrier height influenced by oxygen vacancies driven in our out the TO



TE:	Top Electrode (Pt)
TO:	Tunnel Oxide 20-30A
CMO:	Conductive Metal Oxide
BE:	Bottom Electrode (Pt)

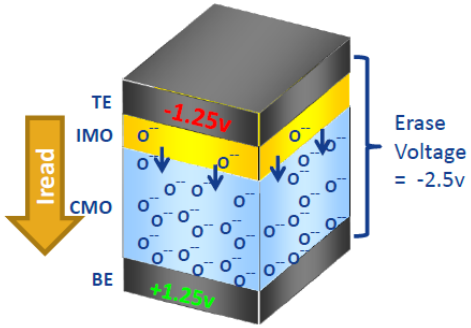
Program



Cell current is *low*.

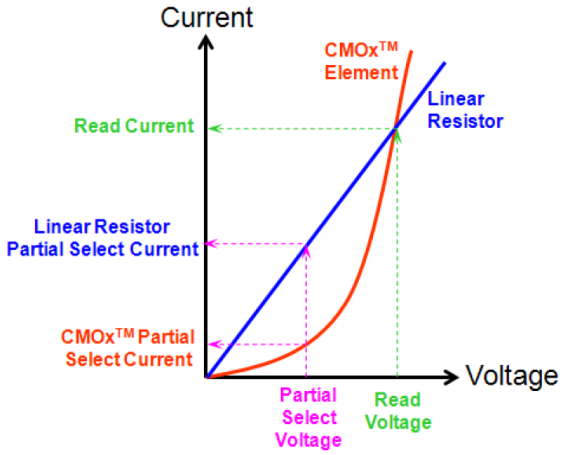
Programmed State: some Oxygen ions are distributed in the IMO layer.

Erase



Cell current is *high*.

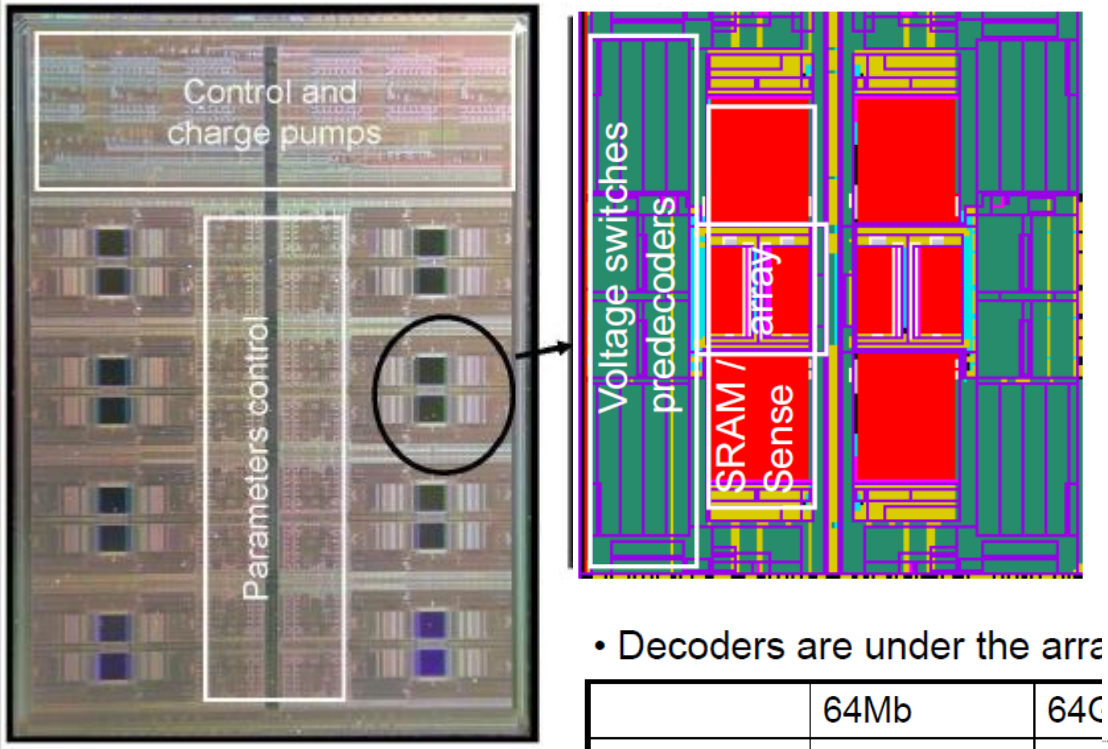
Erased State: Oxygen ions are distributed in the CMO layer.

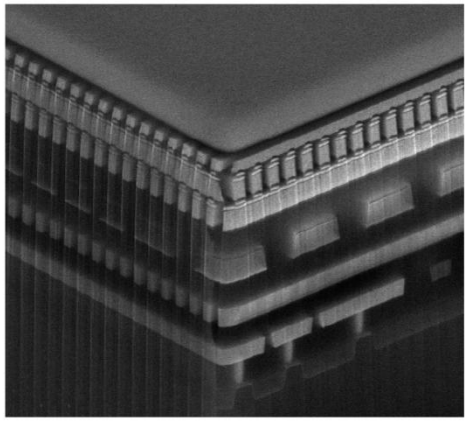


J.Sanchez, NCCAVS Thin Film User Group Meeting, 10/14/09

UNITY SC ISSCC2010 SRC

A 0.13µm 64Mb Multi-Layered Conductive Metal-Oxide Memory





• CMOS / Interconnect / BL / WL / BL with cells

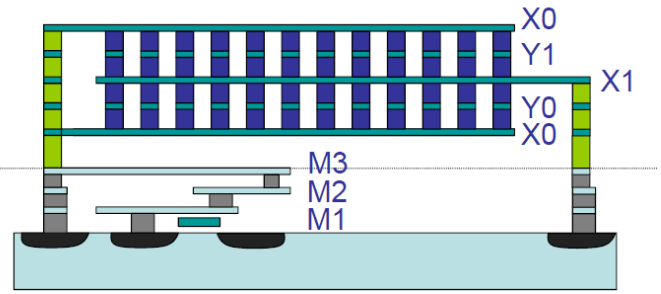


Figure 14.3.5: Test chip micrograph and a

• Decoders are under the arra

	64Mb	64C
technology	130 nm	45n 90n
Die size	Test Chip, 3.27 mm^2 array size	123 mm
Cell size	0.168 µm^2	0.081 µm^2

Outline

Need for new Non Volatile Memory?

Materials → RRAM : Classification

RRAM : Memory Structure

Device → Resistive Switching Behavior

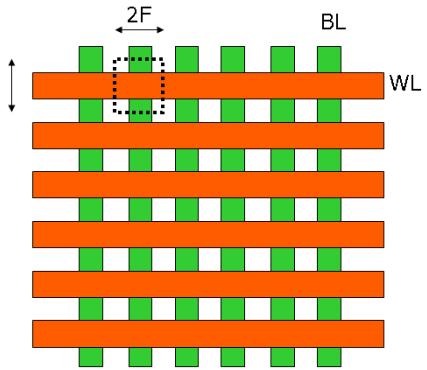
RRAM: Status

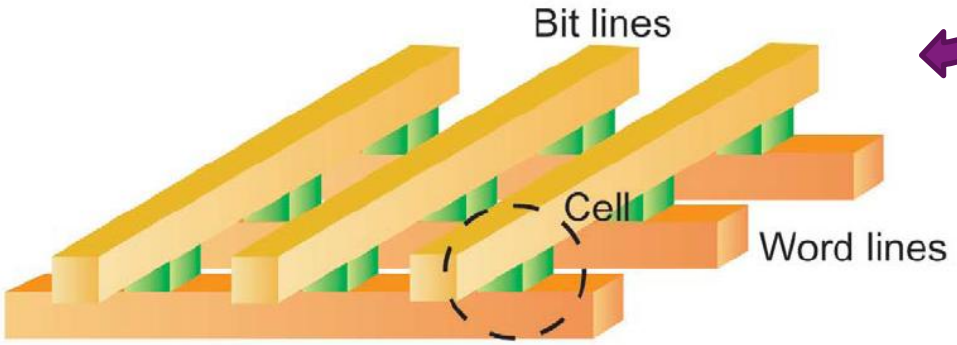
RRAM Memory Structure

- Memory Cell > RRAM element
- Different RRAM Cell configurations
- 3D RRAM architectures

RRAM Cell and Array configurations

- RRAM element = RRAM cell ?
  - Raw Cross Point array = highest density configuration
  - Cell size = $4F^2$

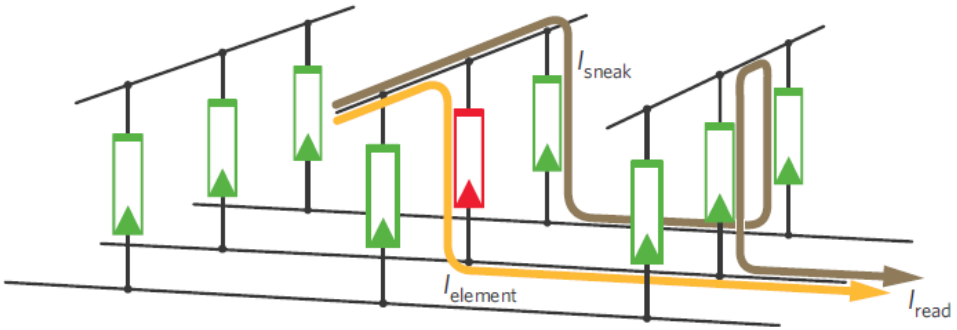


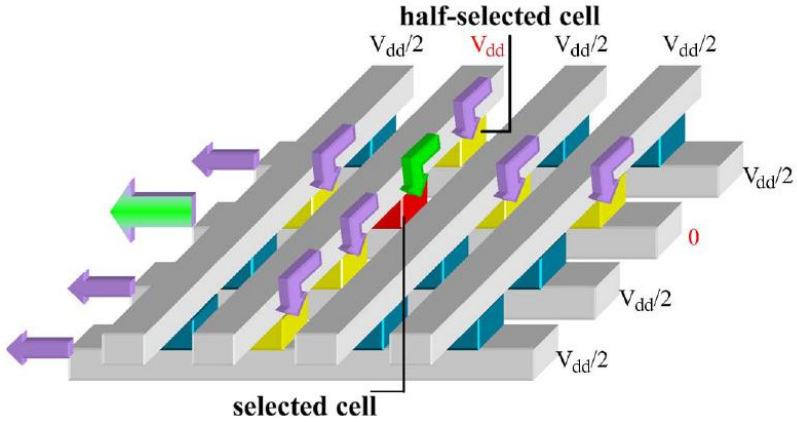


Akihito Sawa,
MaterialsTodayJUNE 2008 |
VOLUME 11 | NUMBER 6 p. 28

RAW XP LIMITATIONS

- Read errors due to sneak current paths
- Program disturbs on half-select cells (1/2 or 1/3 V scheme)
- Power dissipation due to current through half-selected cells

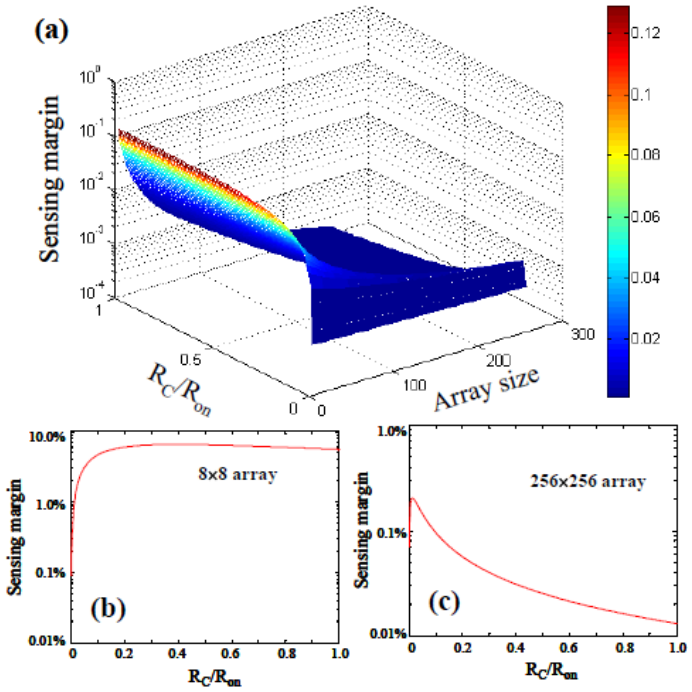




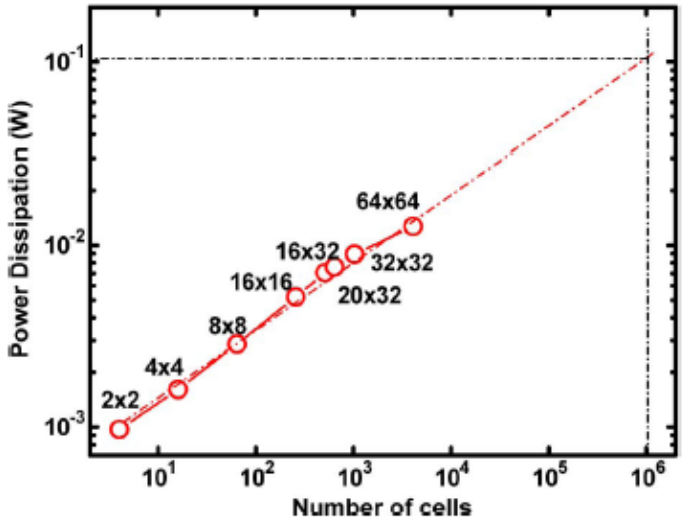
E.Linn en al, NATURE MATERIALS VOL 9 p. 403 MAY 2010

J.Liang et al., IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 57, NO. 10, p.2532 OCTOBER 2010

RAW XP ARRAY EXPLORATION



An Chen, Nanotechnology (IEEE-NANO), pp.1767-1771, 15-18 Aug. 2011



J.Liang et al., IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 57, NO. 10, p.2532 OCTOBER 2010

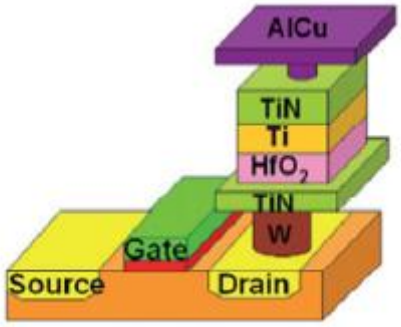
Very limited array sizes, dependent on Ron/Roff ratio, Ron value, non-linearity, etc.

Solution ? Need for selector element in RRAM cell

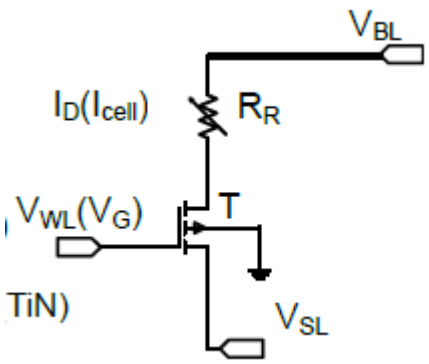
1T1R cell

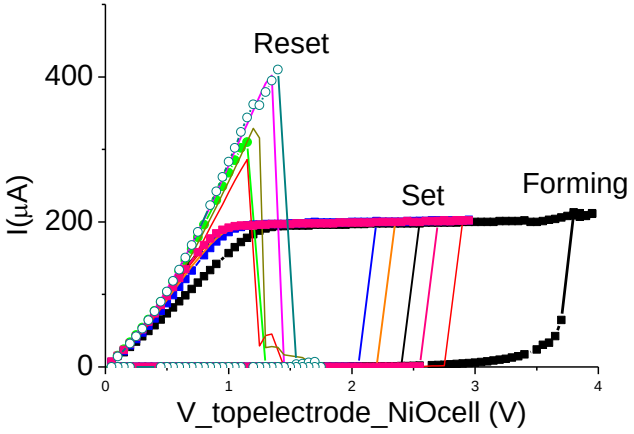
Transistor is ideal selector

- Both isolation switch and current limiter (during SET)
- 3-terminal device : large cell
- Best suited for embedded RRAM



F,Chen ITRI



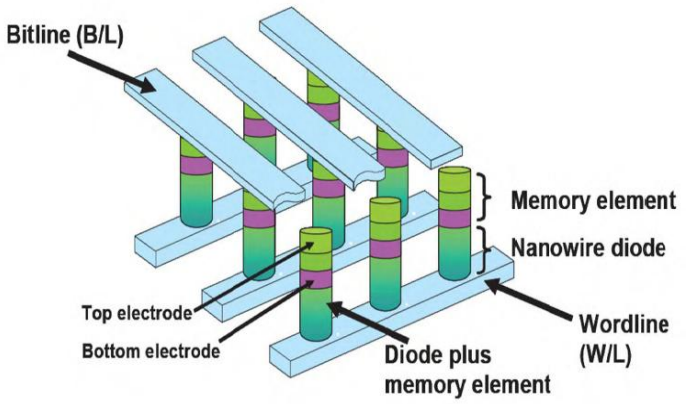


F.Nardi et al, IMW 2010

IDIR-ISIR cell

- Diode selector
  - Good selector : strong asymmetry (rectification) combined with strong (exponential) non-linearity
  - 2 terminal selector on top of RRAM
    - Small cell size possible
  - Only for unipolar switching RRAM
  - Voltage drop over diode
  - Large aspect ratio

P.Wong (Stanford)



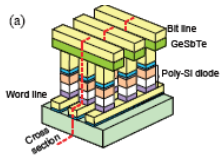
- For bipolar RRAM
  - New 2 terminal selectors :
    - "Symmetric" diode type and Volatile Switching types

2- Terminal SELECTOR concepts

unipolar

Diode types

-p(i)n diode
-Schottky diode



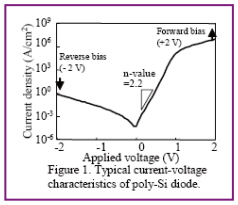


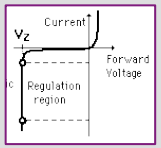
Figure 1. Typical current-voltage characteristics of poly-Si diode.

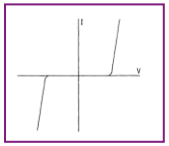
Y.Sasago et al, VLSI Tech.Symp. 2009

bipolar

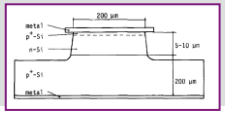
Symmetric diode type

-Zener





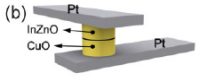
-Punch Through Diode

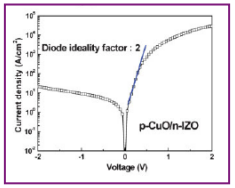


Using semiconducting material

Diode types

MOx pn/Schottky diode

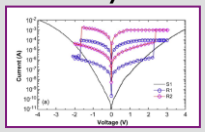




M-J. Lee, Advanced Functional Materials, 2008, 18, p.1

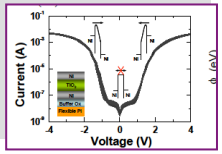
Symmetric diode type MO_x

- Schottky Diode



J-J. Huang, EDL 11(10) 2011

-Tunnel Diode

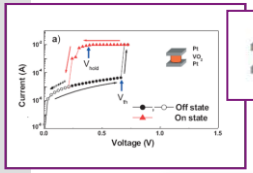


J-J. Huang, IEDM 2011

Volatile switching type

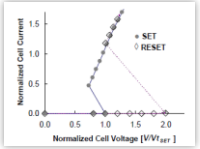
-MOTT VO2

M-J. Lee, Advanced Materials, 2007, 19, p.3919

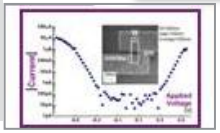


D.Kau et al, IEDM 2009

-OTS Chalcogenide



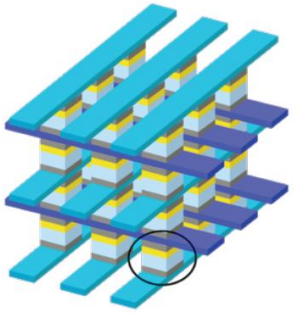
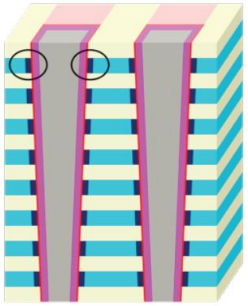
-MIEC Ion Conductor



K.Gopalankhrisnan et al. VLSI 2010

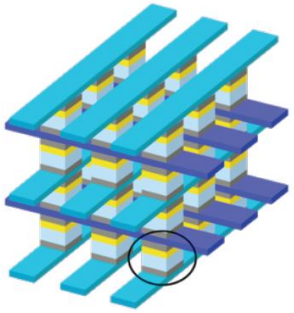
novel materials

3D RRAM ARRAY OPTIONS

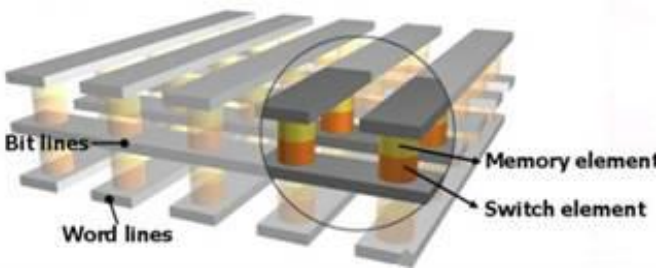
3D Stackable RRAM	3D VRRAM
	

3D RRAM ARRAY OPTIONS

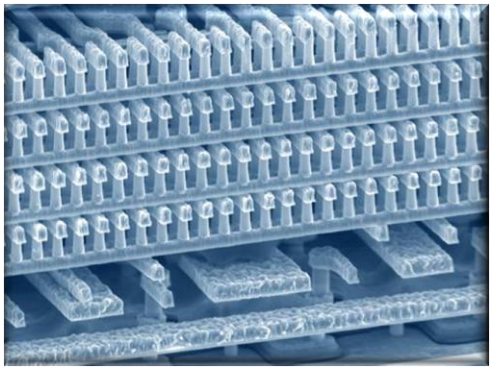
3D Stackable RRAM



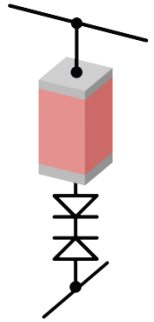
"pseudo 3D" = 2D stacking



M. Lee, et al., IEDM Tech. Dig. 2007



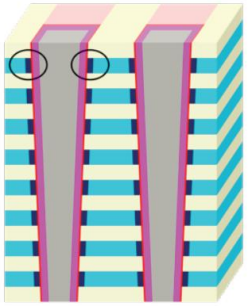
3D Matrix, Semiconductor International , 7 Jan. 2005



ISIR

3D RRAM ARRAY OPTIONS

3D Stackable RRAM	3D VRRAM



"true" 3D

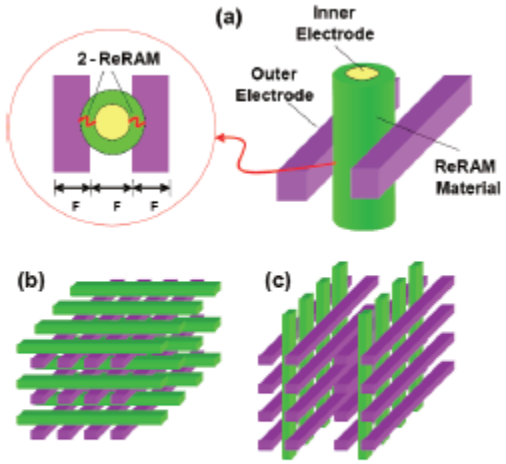


Fig. 1 Schematic diagram of (a) an unit vertically-defined ReRAM cell, (b) horizontal cross-point architecture (HCPA), and (c) vertical cross-point architecture (VCPA).

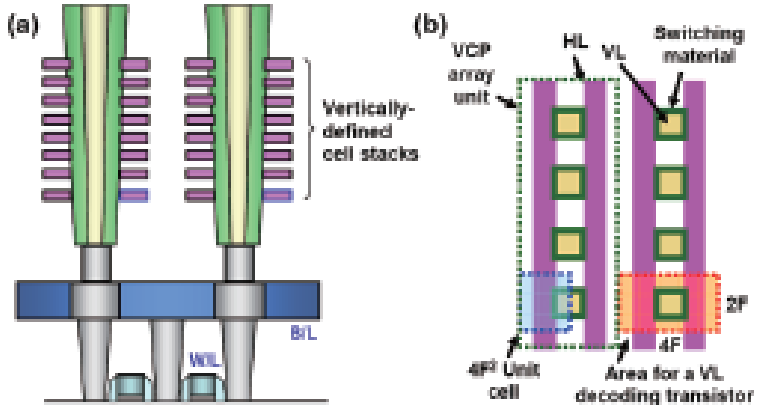
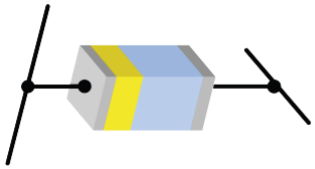


Fig. 10 (a) Vertical view and (b) top view of VCPA ReRAM with $4F^2$ memory cell densities.

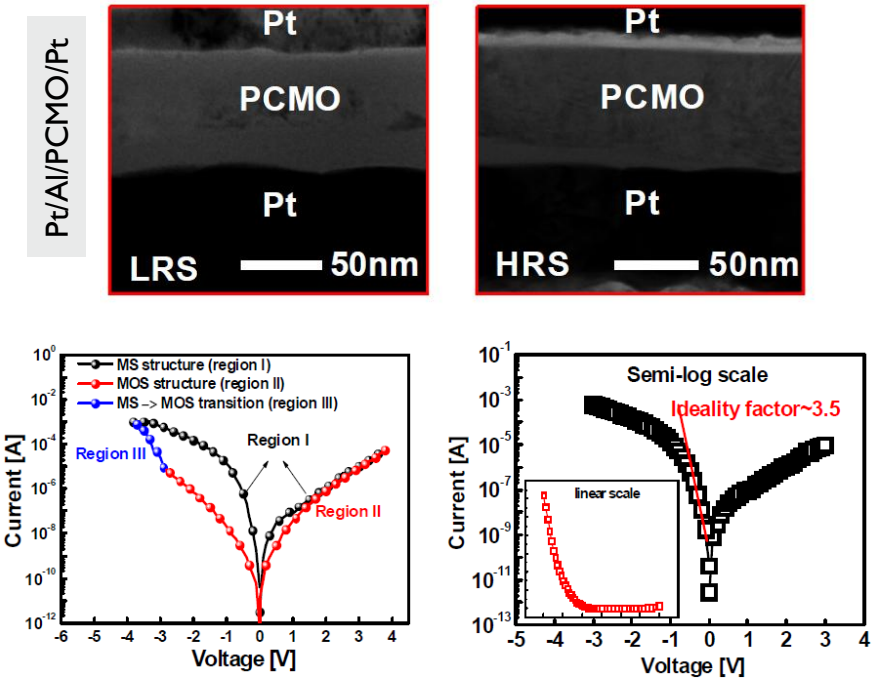


No place for selector !
→ **SRC**

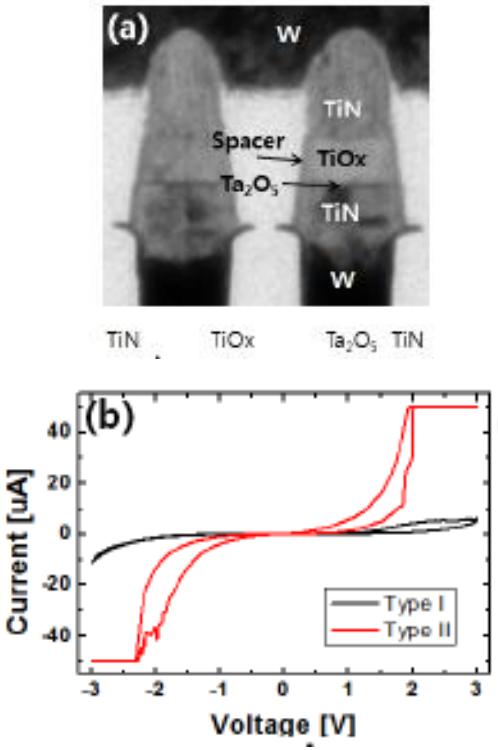
H.Yoon, et al., VLSI Tech. 2009

Self Rectifying Cell

- Cell with strong nonlinearity (in ON state)
- Some proposals, but still limited nonlinearity

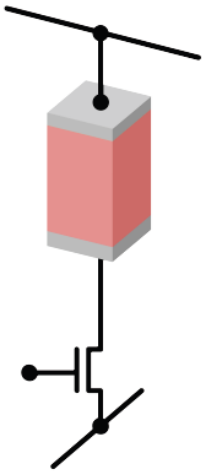


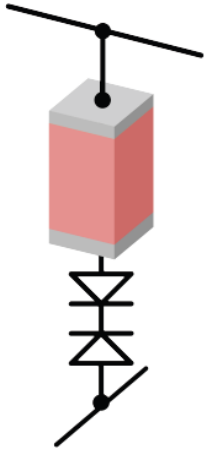
M.Jo et al, VLSI Tech. 2010

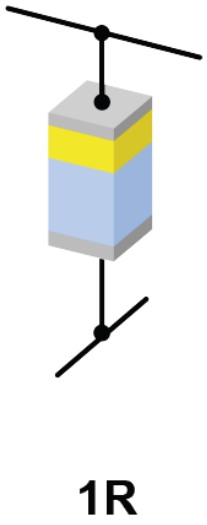


Hynix VLSI Tech. 2012

BIT CELL SELECTION







	Embedded	2D stackable array	3D vertical RRAM
PROS	Easy to optimize high ON/OFF ratio Easy to integrate in CMOS BEOL (3 extra masks vs 8 for Flash)	4F2	4F2 thin
CONS	Big cell, not stackable	Stackable?	No real solution yet

Outline

Need for new Non Volatile Memory?

Materials → RRAM : Classification

RRAM : Memory Structure

Device → Resistive Switching Behavior

RRAM: Status

RRAM switching behavior

Detailed understanding of RRAM device behavior required for :

- Tuning memory operation conditions
- Predicting reliability
- Optimizing material stack

Not just process, but detailed kinetics of device behavior

Focus on oxygen-drift HfO_2 RRAM

- More generally applicable to bipolar filamentary switching (Ox)RRAM

Understanding RRAM switching

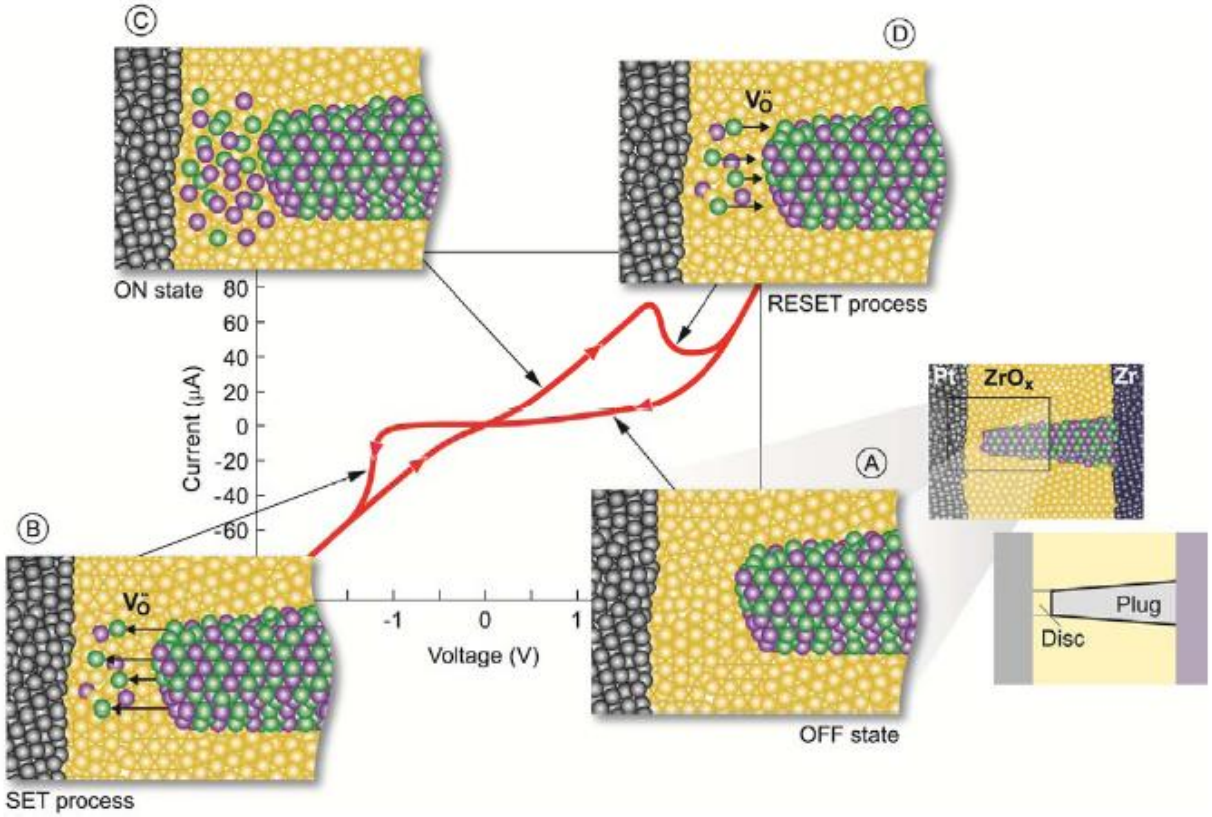
1. **Modeling approaches**
2. Intrinsic RRAM switching
3. QPC filament conduction model
4. Hourglass switching model

Modeling approaches

How to understand filamentary switching ?

(i) **use your imagination**

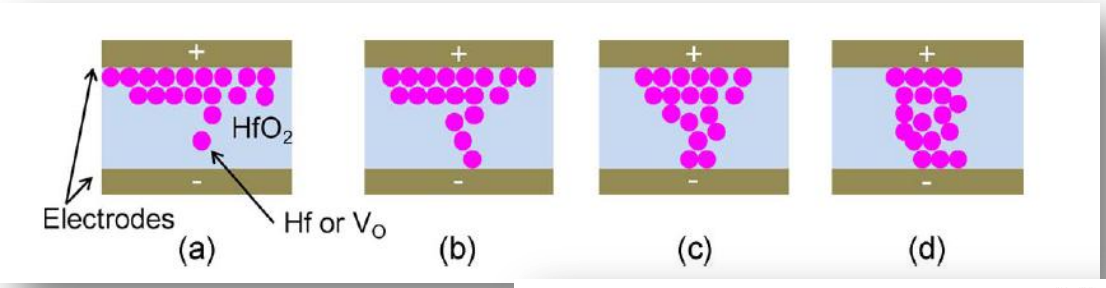
The *Artist* approach to RRAM



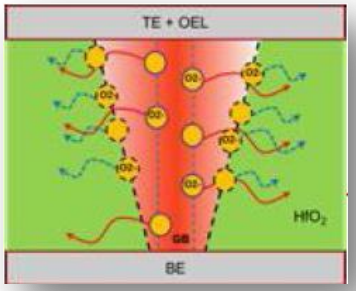
R. Waser et al. in: Nanoelectronics and Information Technology (3rd ed.), Wiley-VCH 2012

JARA FIT
Fundamentals of Future Information Technology

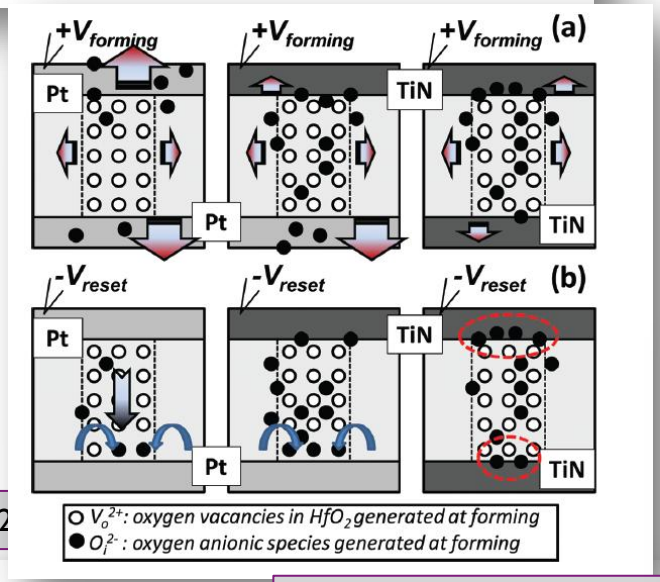
(too) many RRAM artist styles ?

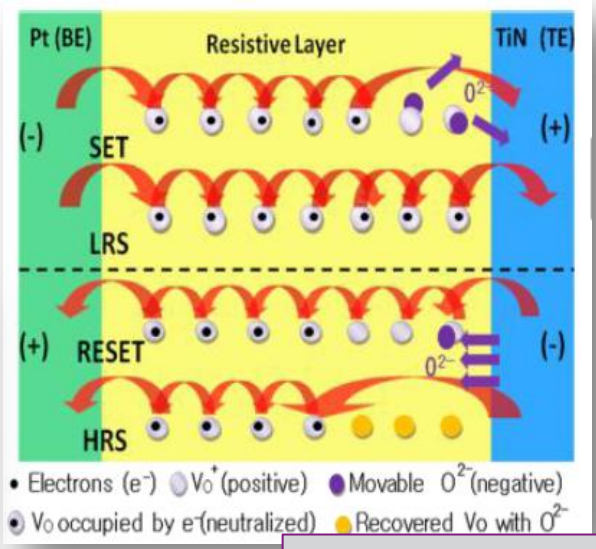


D. IELMINI TED 2011

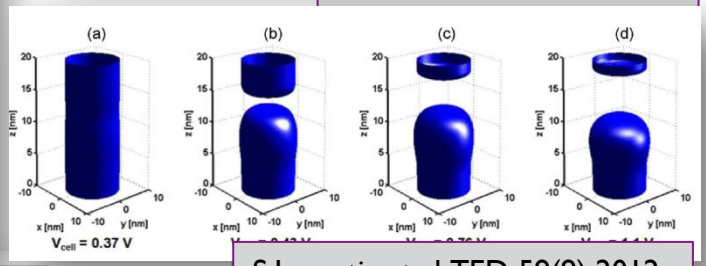


G.Bersuker, 2nd RRAM workshop 2012



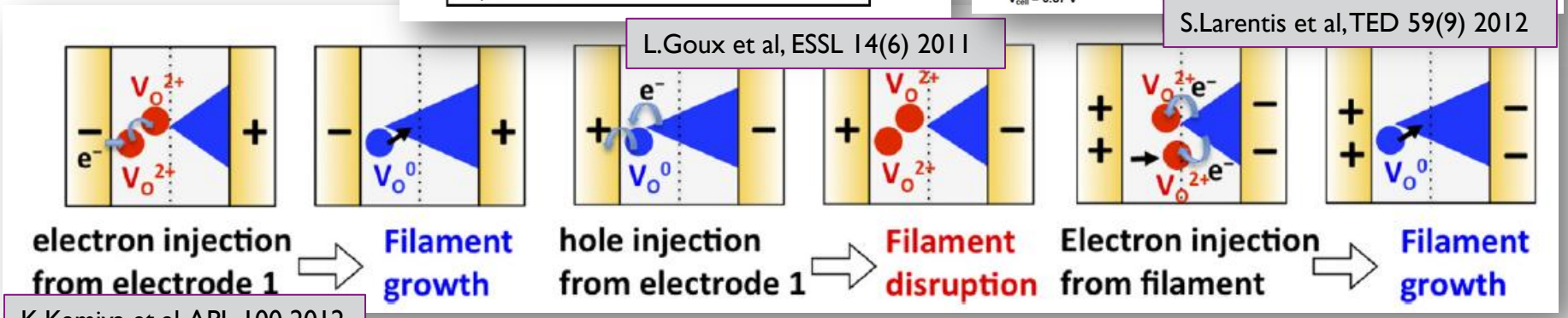


N.Xu et al, VLSI Tech 2008



S.Larentis et al, TED 59(9) 2012

L.Goux et al, ESSL 14(6) 2011



K.Kamiya et al, APL 100 2012

Relevance of Science Art ?

- Visualize possible processes
  - Generation of new insights
  - May hint to possible flaws in the assumed model
  - Explaining RRAM to your management
- Not a proof on its own but a good add-on of theoretical models
- Limitations :
  - Limited to classical "particle" models : problem to visualize Quantum-Mechanical processes...

Modeling approaches

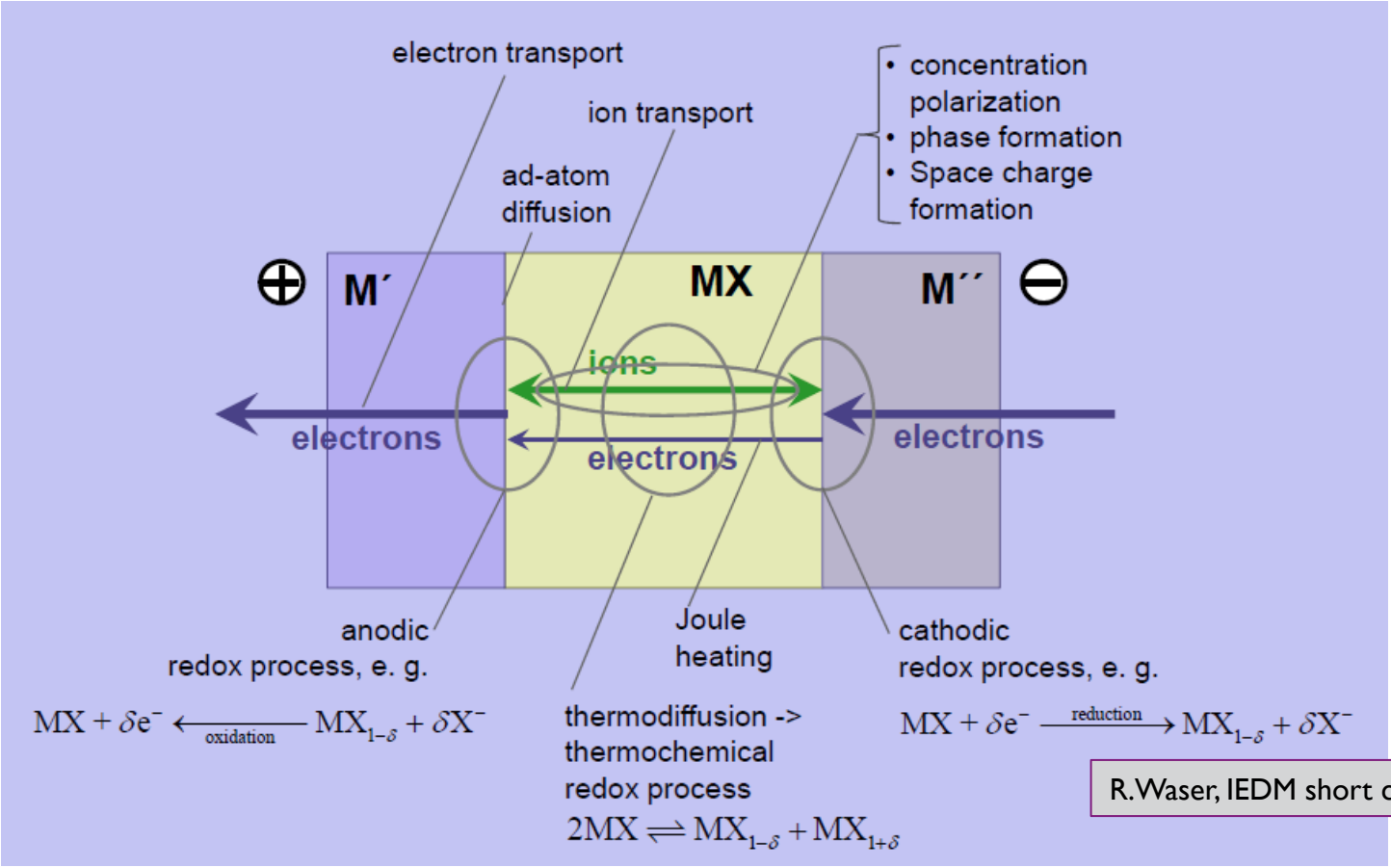
How to understand filamentary switching ?

(i) use your imagination : the "artist" approach

(ii) **bottom up: material scientist approach**

BOTTOM-UP approach

- List up all possible physical processes potentially involved in the resistive switching...



R.Waser, IEDM short course 2011

BOTTOM-UP approach critique

Too many possible equations to cope with.

- How to select relevant/dominating processes?
- A lot of different processes described by similar "exponential" math....

You only get out what you put in

- unexpected processes may play a role

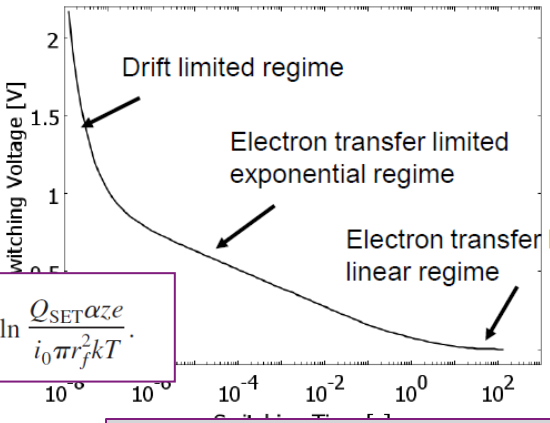
Classical "continuum" approach

- Finite element modeling of current & temperature based on local conductivity and Joule heating
- Cannot account for Quantum-Mechanical effects!

Example : V-t dilemma in CBRAM

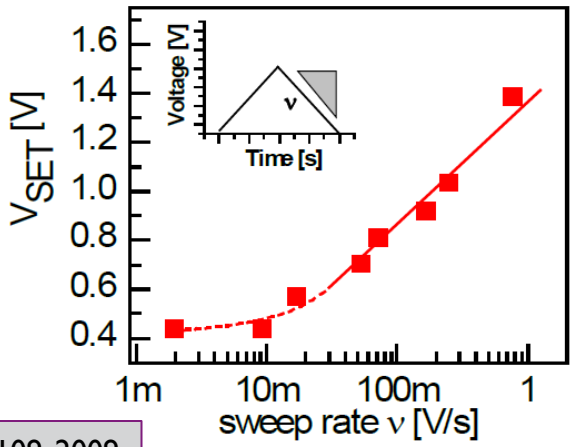
- Which is the rate limiting process in CBRAM?
  - (i) anodic dissolution of Cu according to $Cu \Rightarrow Cu^{z+} + ze^-$
  - (ii) drift of the Cu^{z+} cations across *the* SiO_2
  - (iii) cathodic deposition at the Pt electrode by $Cu^{z+} + ze^- \Rightarrow Cu$.
- All 3 give exponential !
- Argued that (iii) dominates through the charge transfer rate at the Cu/SiO_2 interface described by the Butler–Volmer equation

Simulation



$$V_{SET} = \frac{kT}{\alpha z e} \ln \nu + \frac{kT}{\alpha z e} \ln \frac{Q_{SET} \alpha z e}{i_0 \pi r_f^2 kT}.$$

Experiment $Cu/SiO_2/Ir$ cells



C.Schindler et al., Appl.Phys. Lett, 94, 072109, 2009

How deep at the bottom to start?

- The "ultimate" bottom : Ab Initio
  - Obtained A.I. results have been revealing on the behavior of oxygen defects (charge states, formation energy, diffusion constants) and their coalescence into filaments
  - But limited to study specific effects

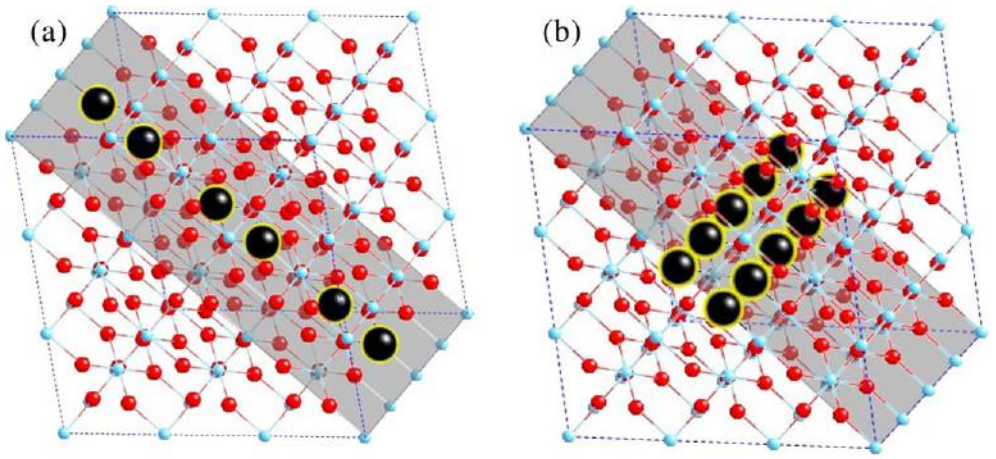
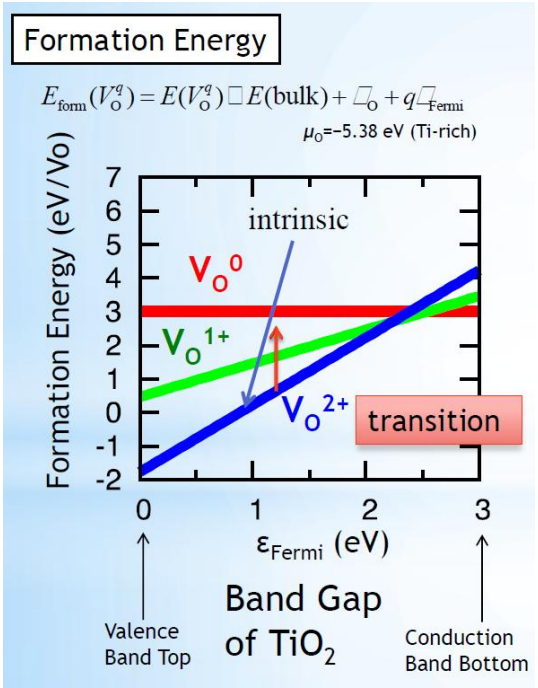


Fig. 1. Schematic picture of the oxygen vacancy chain system in 3 × 3 × 4 supercell of rutile TiO_2. The red represents oxygen, the blue represents Ti, and the black represents the oxygen vacancy. All oxygen vacancies are on the same (110) plane. (a) [110] vacancy chain. (b) [001] vacancy chain.

S. Park, et al.,IEEE Electron Device Letters, 32, 197, 2011.



Katsumasa Kamiya et al, Appl. Phys. Lett. 100, 073502 (2012);

Modeling approaches

How to understand filamentary switching ?

(i) use your imagination : the "artist" approach

(ii) bottom up: the material scientist approach

(iii) **top-down: the EE approach**

The EE approach

- Start from device behavior: electrical characterization
  - Conduction in different R states
  - Intrinsic versus extrinsic switching curves
  - Try to analyze the important effects (AC vs DC, temperature)
  - Effect of sample geometry (e.g. device area)
  - Others: RTN...
- Come up with a model
  - Filament model for conduction in HRS and LRS
  - Kinetic model for switching
- Check if we can simulate all electrical data with consistent and physically "sound" set of parameters

TOP-DOWN approach critique

- **Behavioral** model...
  ... but preferentially ***physics based***

link to actual material processes

= "MEET IN THE MIDDLE"

- Device behavior can be influenced by
  - Material
  - Device structure
  - Process effects

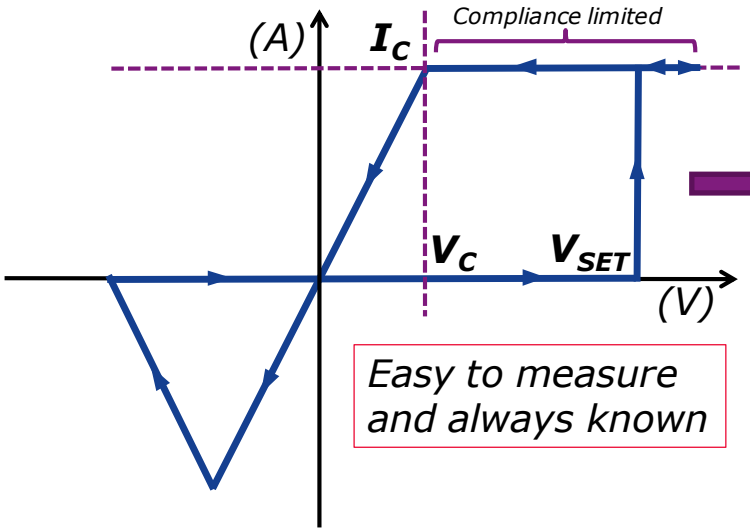
  May limit a more general value..

Understanding RRAM switching

1. Modeling approaches
2. **Intrinsic RRAM switching**
3. QPC filament conduction model
4. Hourglass switching model

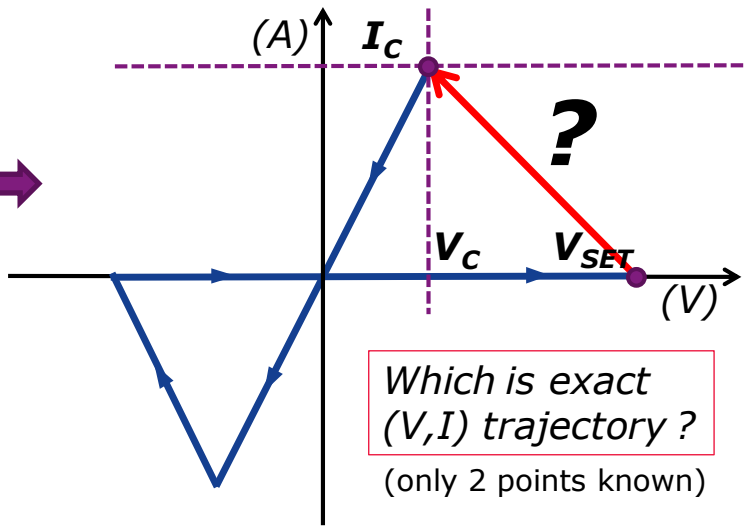
DC switching measurements : 0T1R

Current compliance hides (SET) switching



Easy to measure and always known

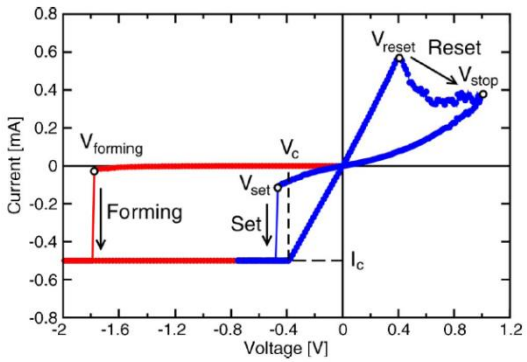
*Measured I-V (= **extrinsic**)*



Which is exact (V,I) trajectory ?

(only 2 points known)

*I-V of TMO (= **intrinsic**)*

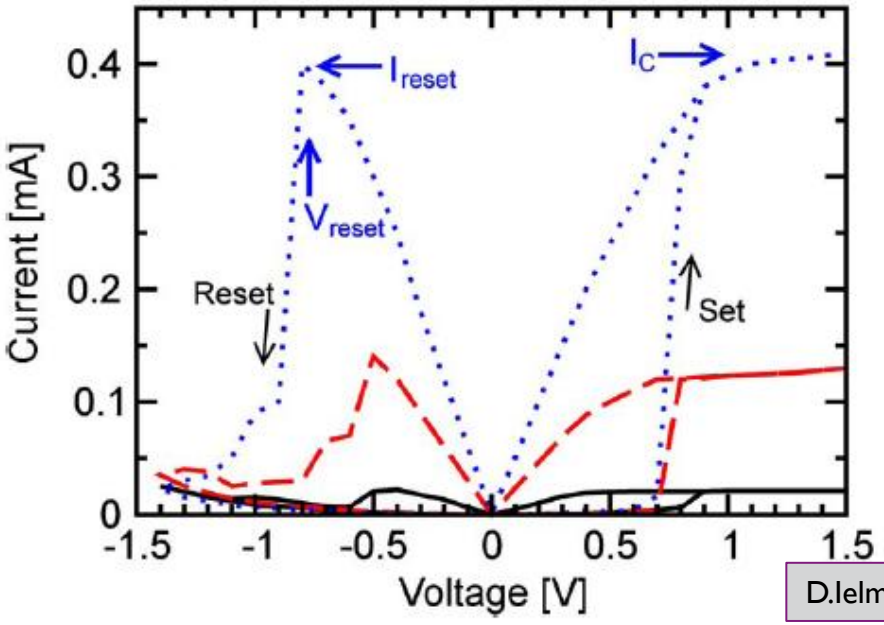


HfO_2 RRAM cell

F.Nardi et al, Trans.El.Dev. 59(9), p.2461, 2012

DC switching measurements : 1T1R

- Total cell voltage during SET switching known
- But high non-linearity of Transistor current $I_{DS}=f(V_G,V_{DS})$ prohibit calculation of voltage over RRAM



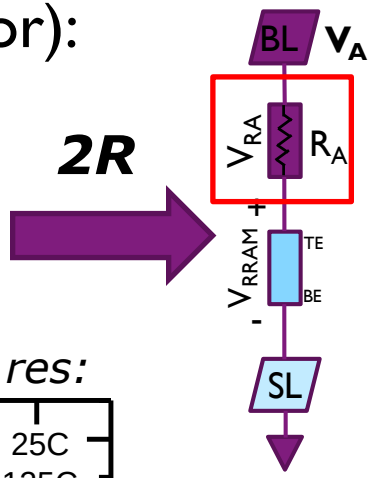
D.Ielmini , Trans.El.Dev. 58(12), p.4310 (2011)

DC switching measurements : 2R

Using a linear integrated component (resistor):

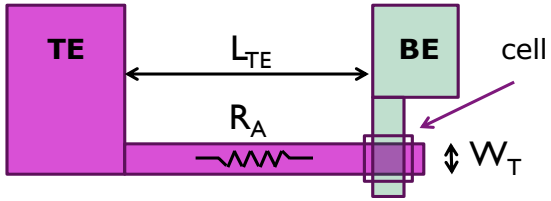
- we can limit current
- We can recover the SET trajectory:

$$V_{RRAM} = V_{applied} - I.R_A$$

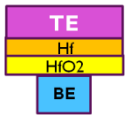


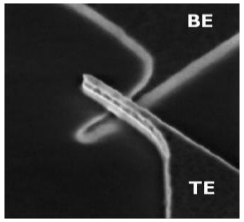
A. Fantini et al, IMW 2012

2R test structures:

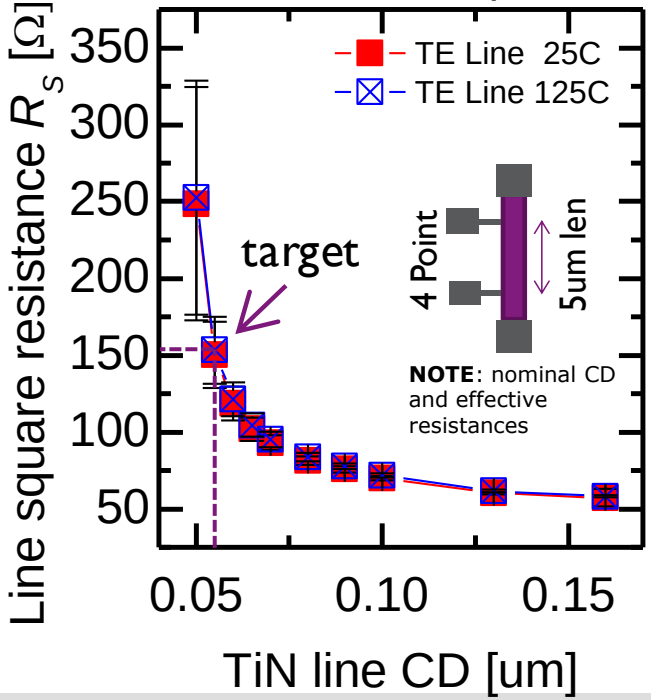


Imec crossbar RRAM

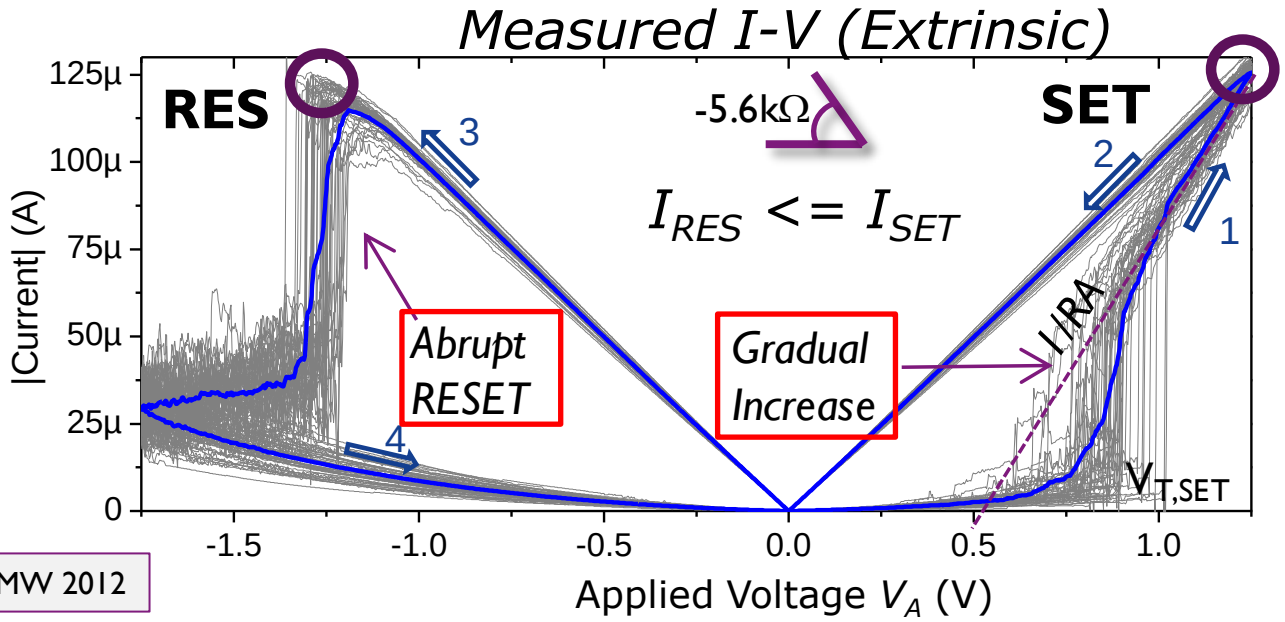




Calibration of sqr res:



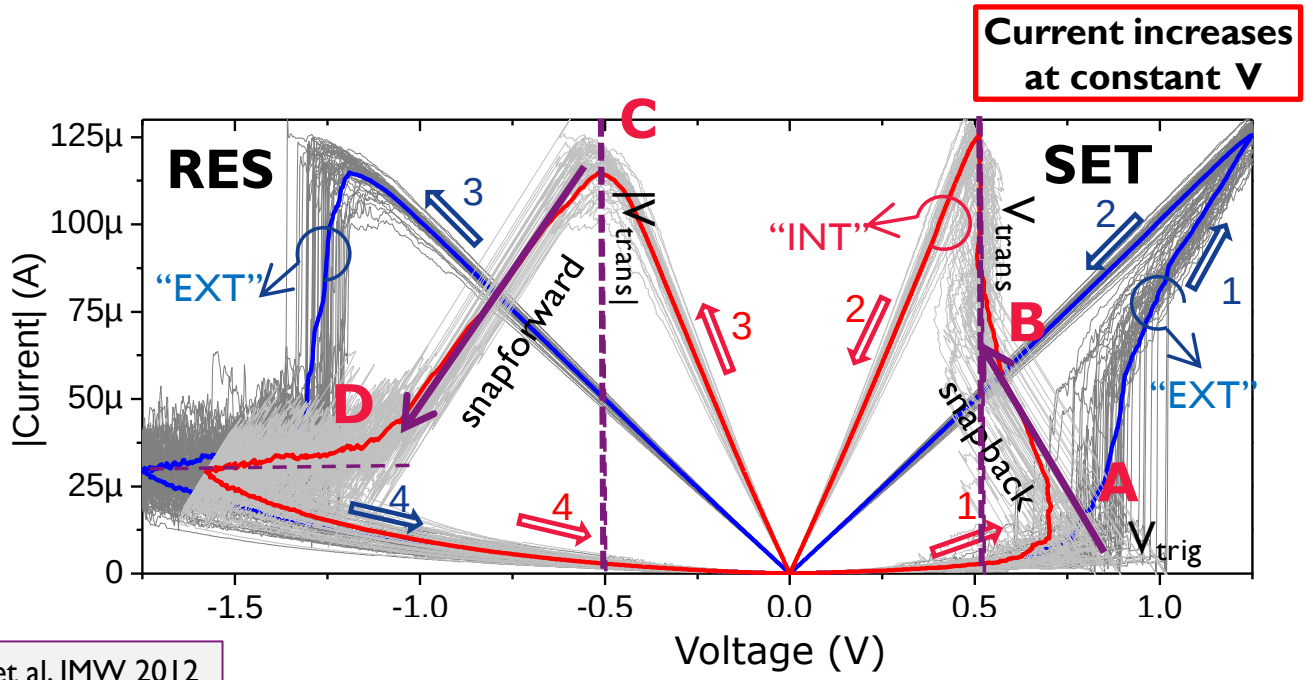
Extrinsic Switching in 2R



A. Fantini et al, IMW 2012

- ***RESET is very abrupt***. In clear contrast to "analog" reset.
- ***Gradual (linear) SET*** after first "jump"
- SET Linearly returns to origin with a different (lower) slope
- Onset of RESET symmetrically occurs at the same end point of SET sweep.

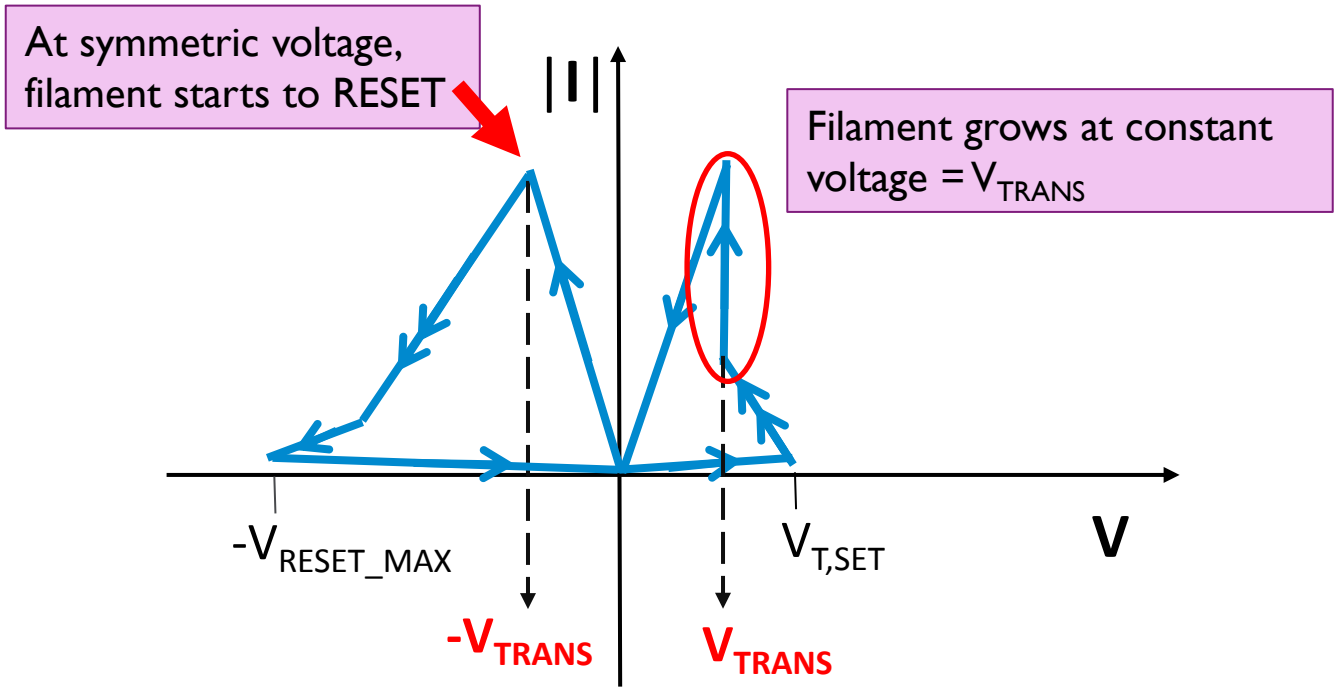
Extrinsic ➔ Intrinsic switching in 2R



A. Fantini et al, IMW 2012

A. SET triggering followed by rapid "snapback": with slope (-1/RA)
B. "Filament" then grows (i.e. current increases) at **constant** voltage ("**transition voltage**") V_{trans}
C. RESET transition triggers at symmetrical ($-V_{trans}$) voltage with fast voltage increase ("snapforward") with slope (-1/RA)
D. "Filament" then shrinks at approx constant saturation current IR,sat

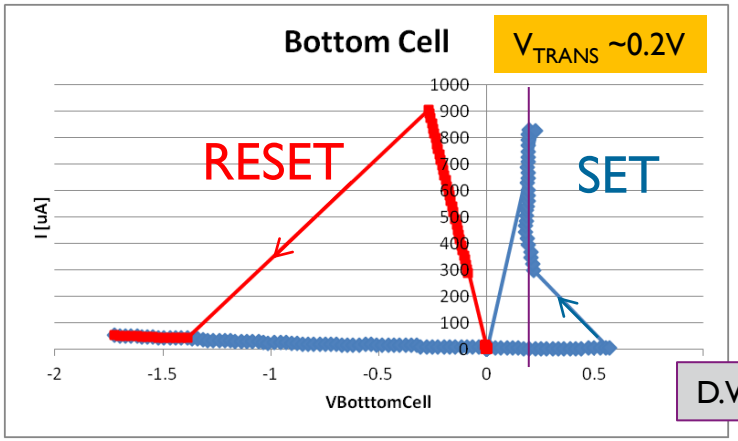
Voltage controlled switching : definition of Transition Voltage



V_{TRANS} is the **minimum voltage required for switching**

Fingerprint of filamentary switching?

- Analysis of different RRAM material systems show **similar intrinsic switching characteristics**



Pt\SiO2\GeSe\Cu
CBRAM cell

D.Wouters, EDL 33(8), p. 1186 (2012)

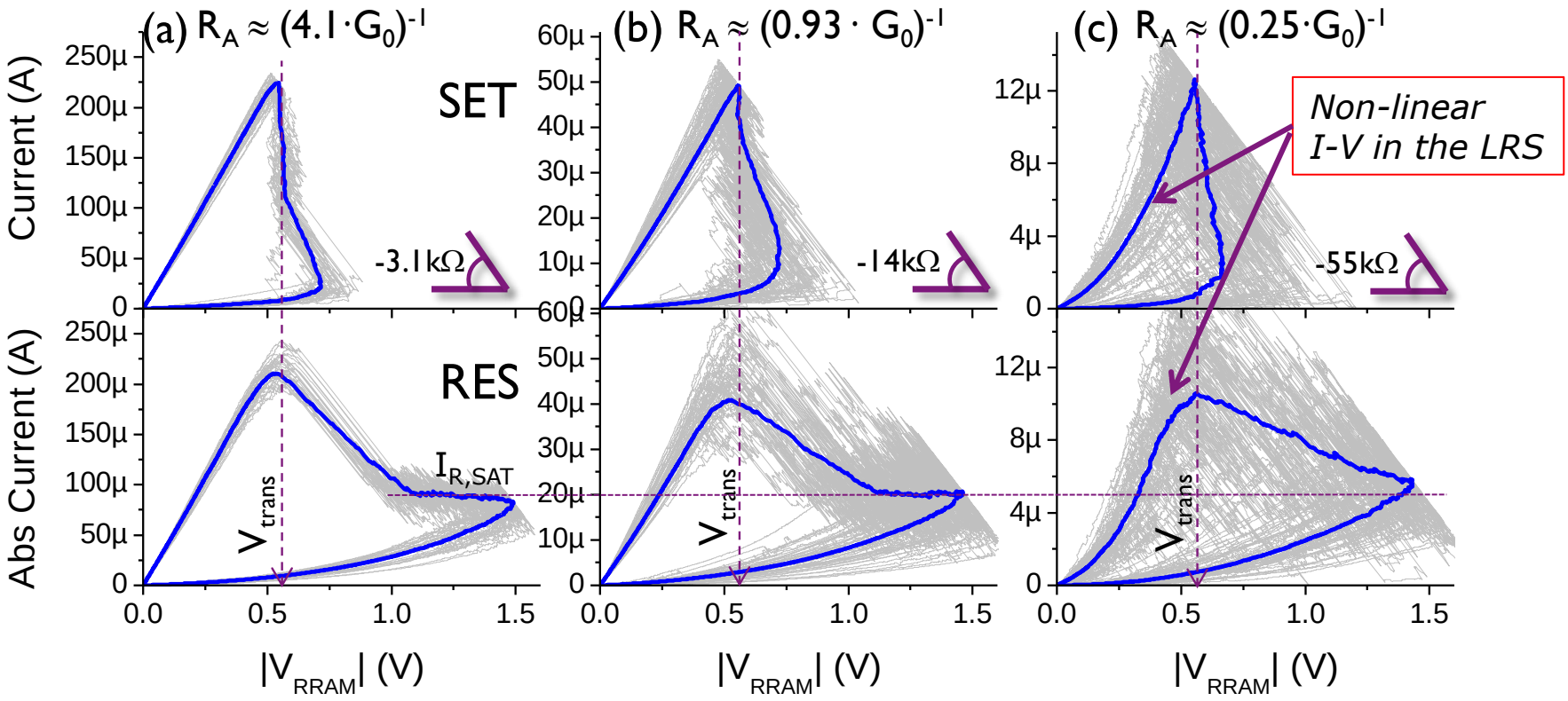
- Transition Voltage = material dependent parameter?

TABLE I
PARAMETERS FOR DIFFERENT ANALYZED CRS CELLS

RRAM element	I_{max}	R_{LRS}[a]	R_{SERIES}	V_{TRANS}[b]
TiN\HfO_2\Hf\TiN	3 mA	~140 Ω	180 Ω	~0.36 V
Pt\SiO_2\GeSe\Cu	0.9 mA	~264 Ω	1050 Ω	~0.18 V
Pt\SiO_2\Cu	15 mA	~27 Ω	220 Ω	~0.26 V
Pt\$Ta_2O_{5-x}$\$TaO_{2-x}$\Pt	40 µA	~10 kΩ	44 kΩ	~0.40 V
Au\CNT\a-C\Au	80 µA	~24 kΩ	70 kΩ	~1.85 V

[a]Average for Top and Bottom RE; [b]Average of + and - V_{TRANS}

Current scaling in 2R

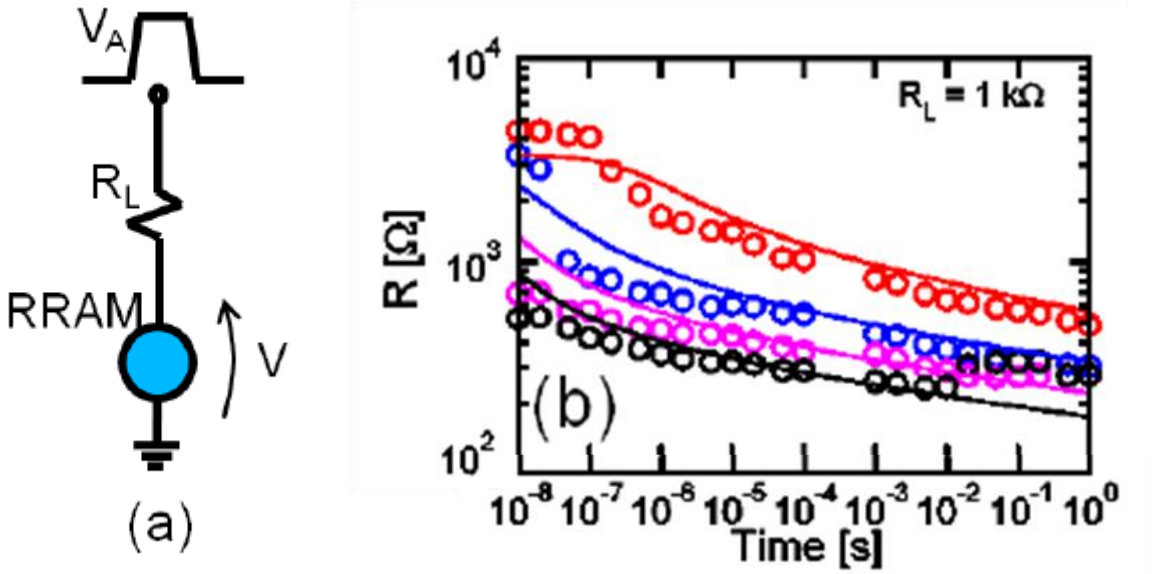


Important observations (mean values):

- Transition voltage not depending on current level
- Evidence of deviation from ohmic behavior for LRS in the lowest current range

AC characterization

- Typically done using voltage pulses
  - Pulse ***effect*** measured by probing R after applying pulse
  - No information of what happens during the pulse

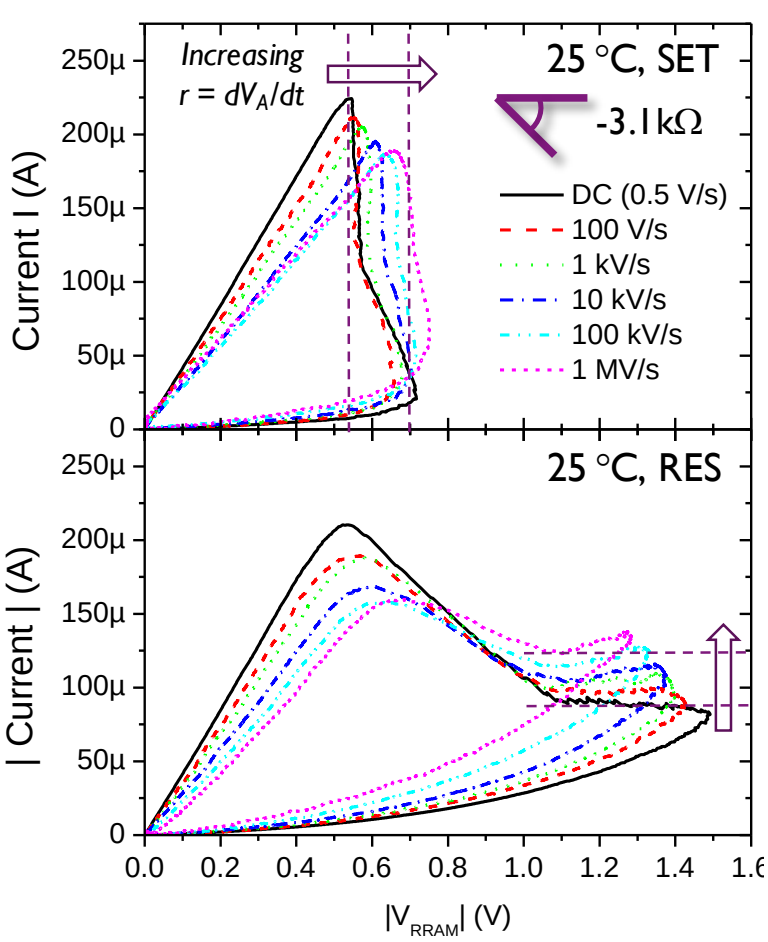


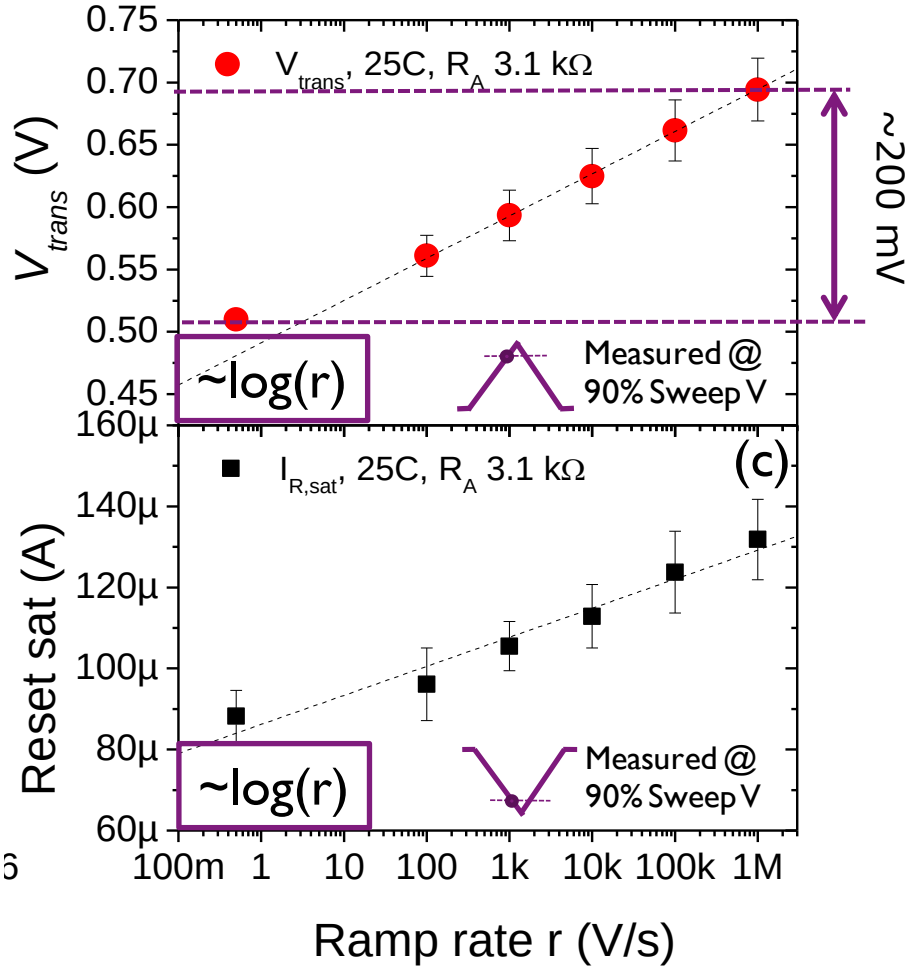
D.Ielmini , IEDM 2011

AC characterization in 2R

A. Fantini , IMW 2012

Transition voltage is log. depending in ramp rate



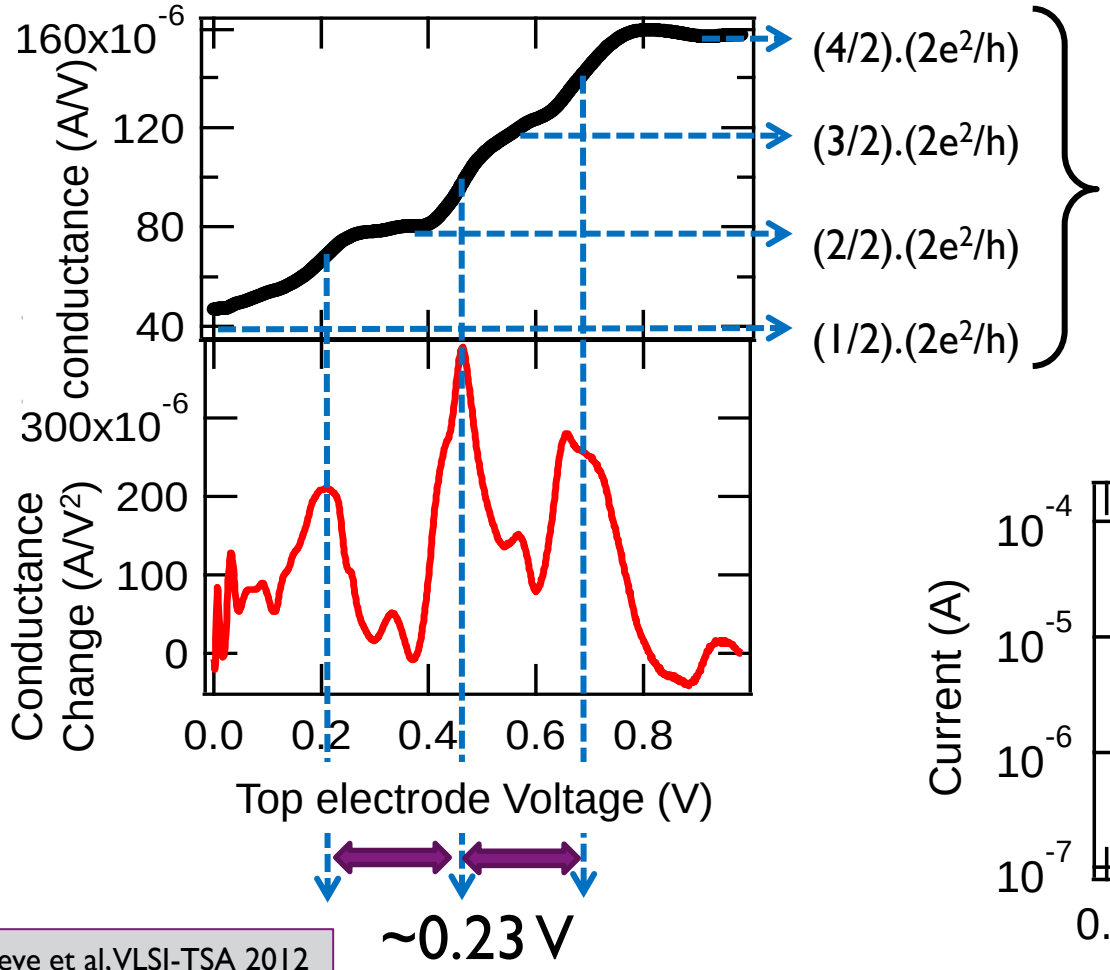


Understanding RRAM switching

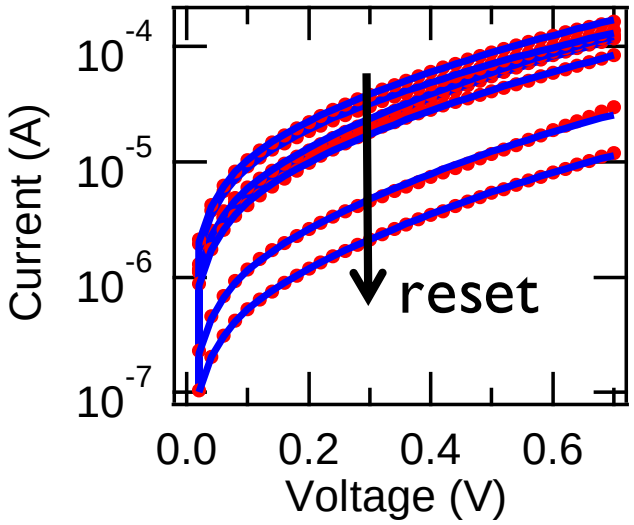
1. Modeling approaches
2. Intrinsic RRAM switching
3. **QPC filament conduction model**
4. Hourglass switching model

Non-linear & Quantized conduction

Room-T measurements

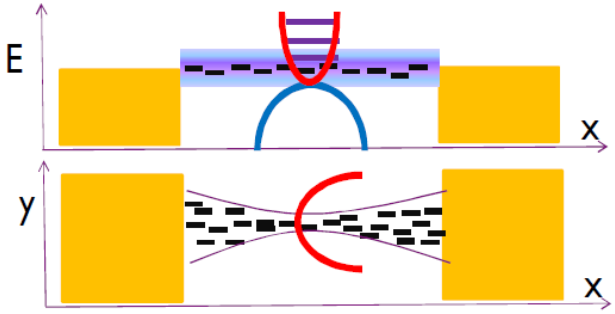


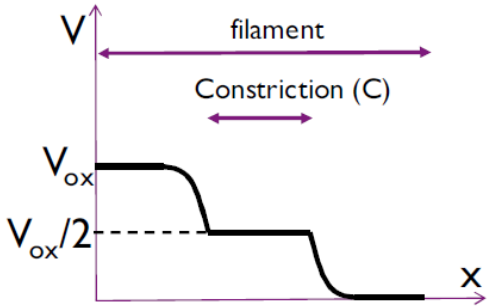
R.Degraeve et al,VLSI-TSA 2012

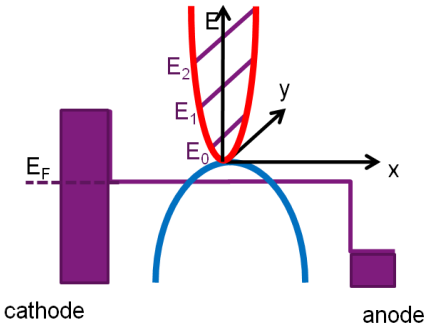


R.Degraeve et al,VLSI 2011

Quantum Point Contact model



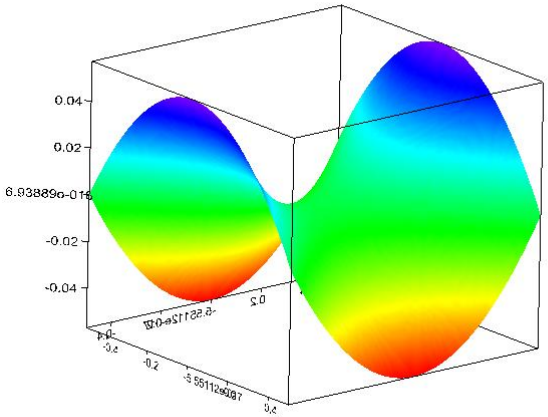




R.Degraeve et al, IEDM 2010

- Inside filament : interacting defects (oxygen vacancies) create conductive band
- **Geometric confinement** of current flow causes bottleneck with discrete levels
- Quantum point contact (QPC) model for conduction

$$E(x,y) = eV_0 - \frac{1}{2}m\omega_x^2 x^2 + \frac{1}{2}m\omega_y^2 y^2$$



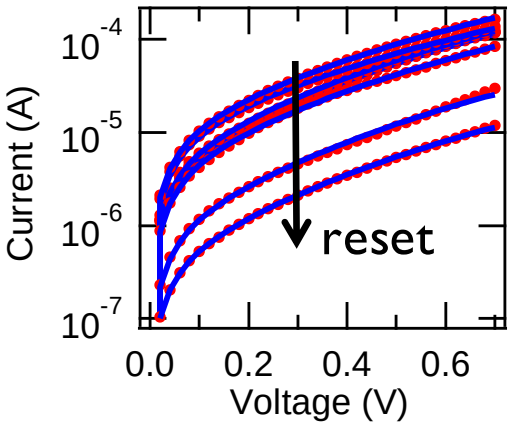
ω_y determines constriction ***width***
- low ω_y → wide constriction
- high ω_y → narrow constriction

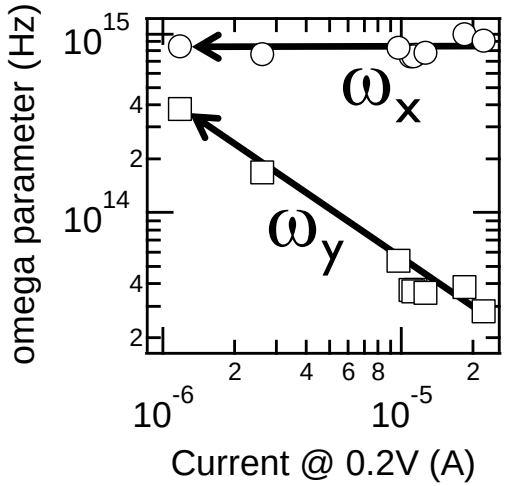
ω_x determines constriction ***length***
- low ω_x → long tunneling path
- high ω_x → no tunnel barrier

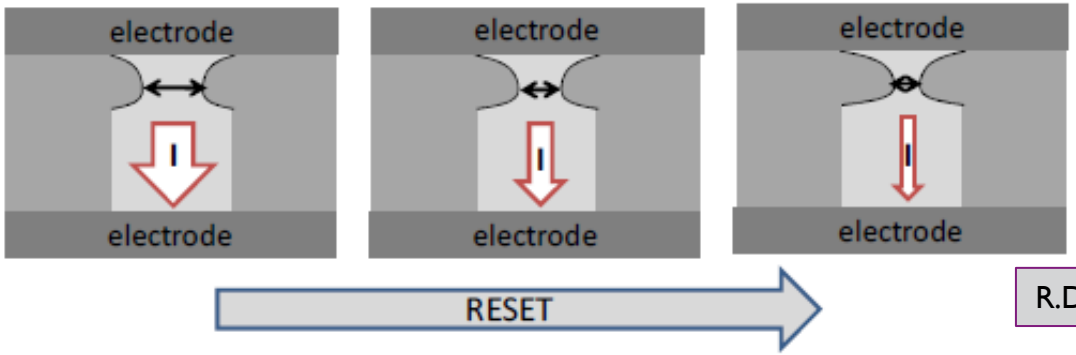
V_0 determines ***nature*** of the constriction
- $V_0 < E_F$ → metallic
- $V_0 > E_F$ → still insulating barrier

Fitting I-V with QPC

- Only ω_y parameter changes → indicating RESET occurs by local filament NARROWING

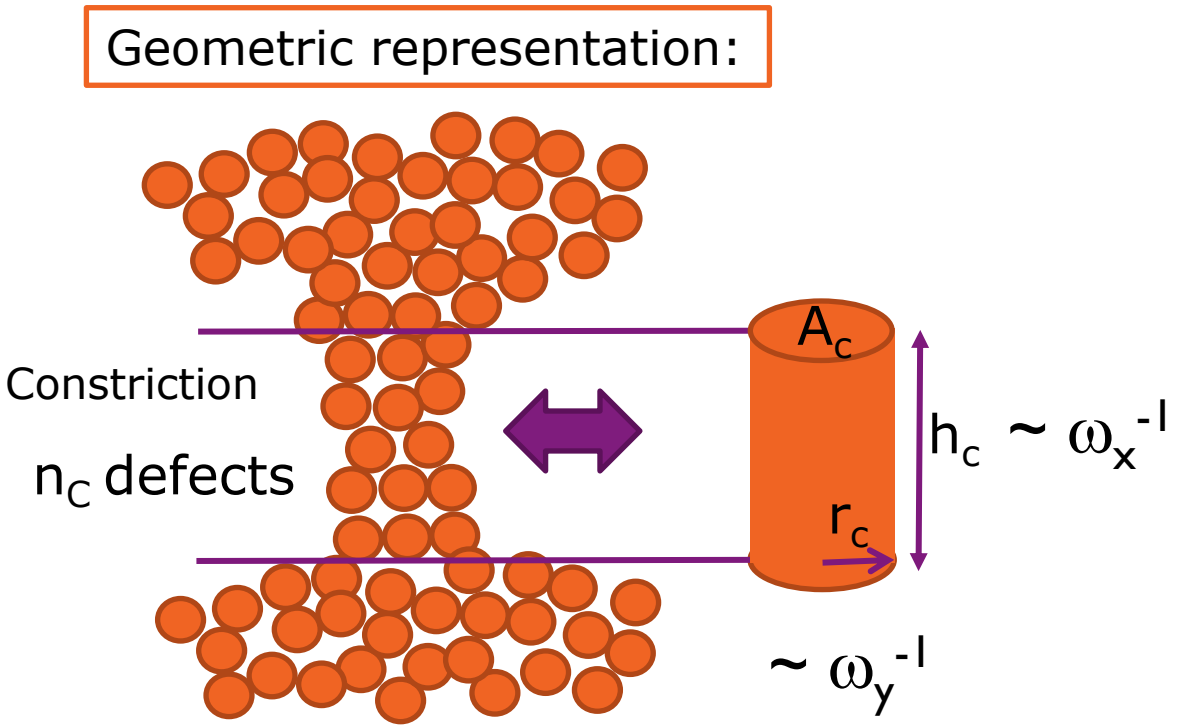




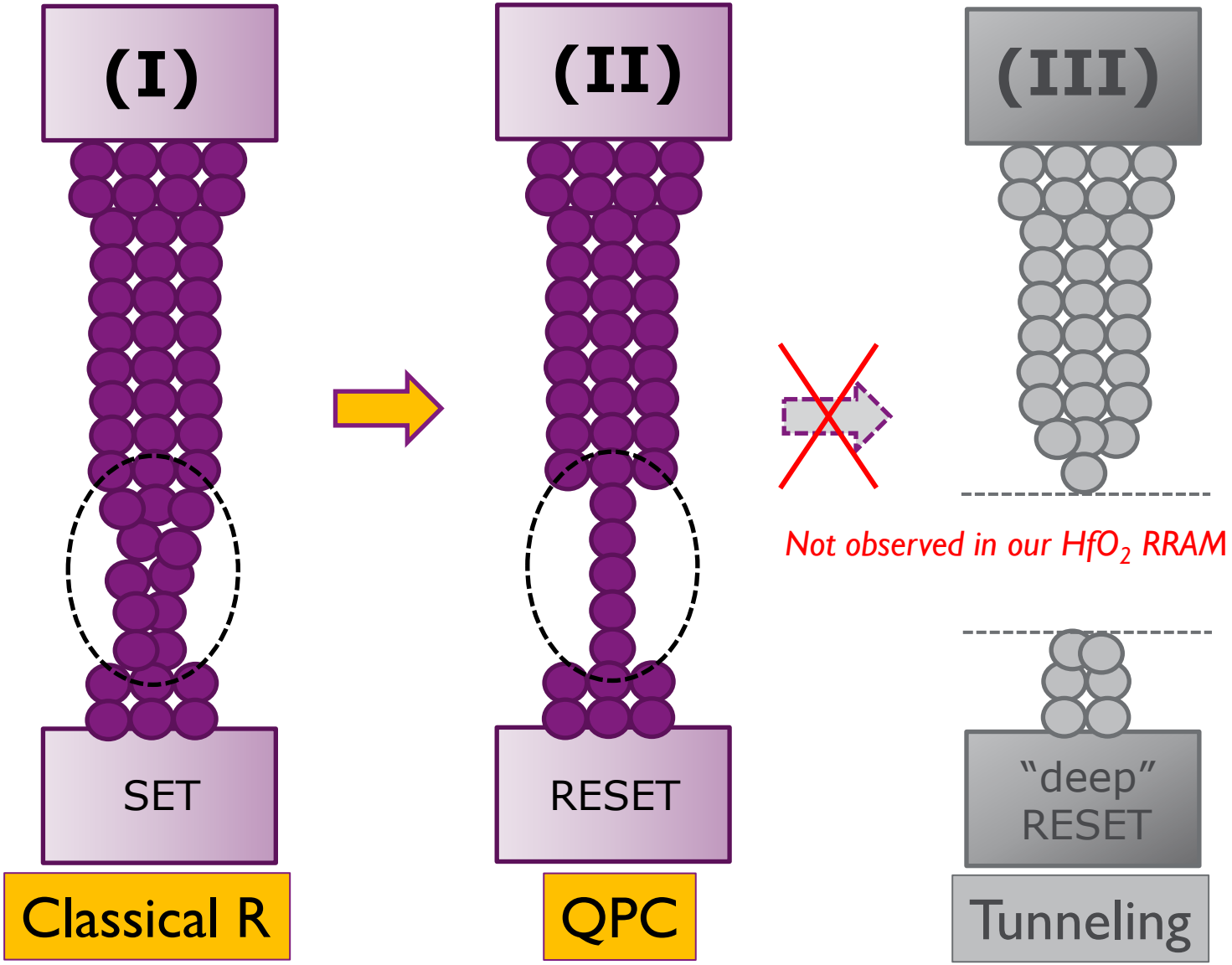


R.Degraeve et al, VLSI 2011

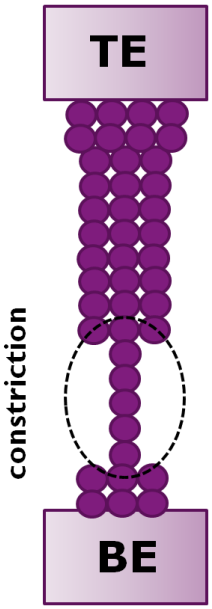
Constriction size ~ # defects

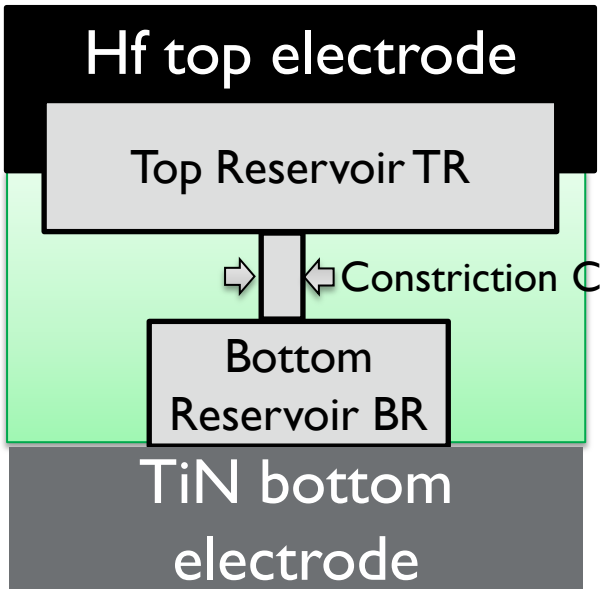


Filament Model



Abstract filament model = Hourglass





R.Degraeve et al, VLSI 2012

- Filament = 2 reservoirs of oxygen vacancies connected by a constriction
- Size of defect reservoirs, number of defect particles, and constriction length are fixed by Forming

Understanding RRAM switching

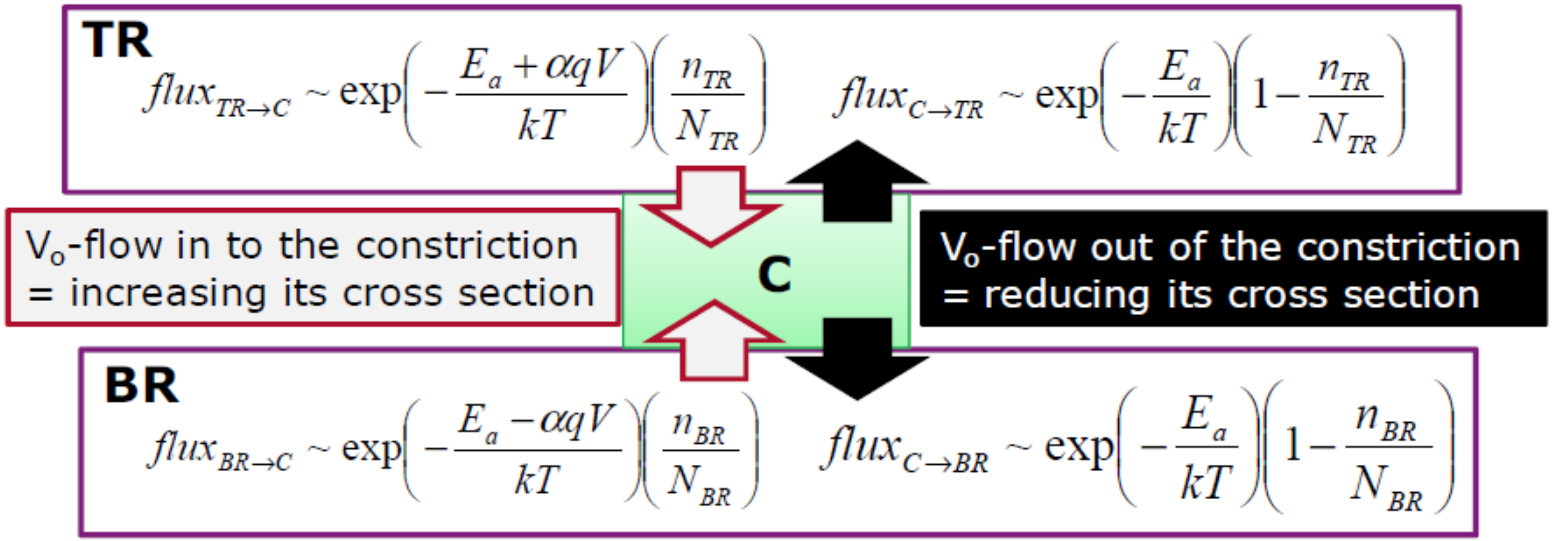
1. Modeling approaches
2. Intrinsic RRAM switching
3. QPC filament conduction model
4. **Hourglass switching model**

Dynamic Hourglass switching model

- Filament = charged defects (oxygen vacancies)
  - Moveable under influence of electric field
- Hourglass shape determined by Forming
  - Hourglass ~ substoichiometric HfOx with higher oxygen vacancy mobility :
  - defects remain in hourglass
  - No generation/recombination
- Defects can move down/up top to bottom reservoir depending on voltage polarity

Dynamic Hourglass switching model

- 4 different defect particle fluxes at TE/BE reservoir – constriction interfaces
  - Temp. activated over voltage modified energy barrier E_a
  - Depending on filling level of the reservoir



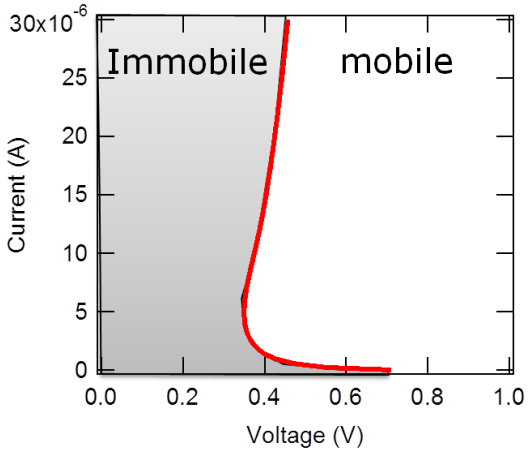
$$T = T_{ambient} + \frac{IV}{n_C} R_{th} \quad \textbf{(Eq. 1)}$$

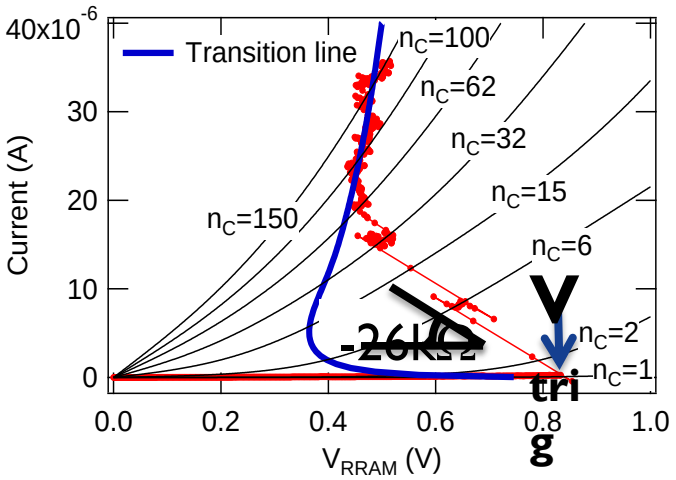
$$n_{total} = n_C + n_{BR} + n_{TR} \quad \textbf{(Eq. 2)}$$

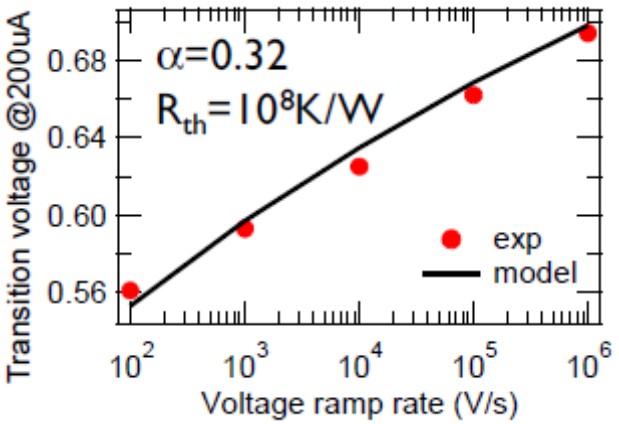
R.Degraeve et al,VLSI 2012

Explanation of transition voltage

- From this model, it is possible to calculate the minimum voltage to move a defect in or out the constriction in a certain amount of time
- This voltage ~ cte at larger currents
  = "transition voltage"
- Independent of polarity : same voltage to start RESET







R.Degraeve et al,VLSI 2012

Further work

Here focused on SET behavior and explanation of "constant voltage" filament growth

Hourglass model can explain also other effects, as:

- "overcurrent" in 1st RESET after forming
- RESET behavior as function of V and time'
- Fluctuationns and Disturb of RESET state
- ....

Outline

Need for new Non Volatile Memory?

Materials → RRAM : Classification

RRAM : Memory Structure

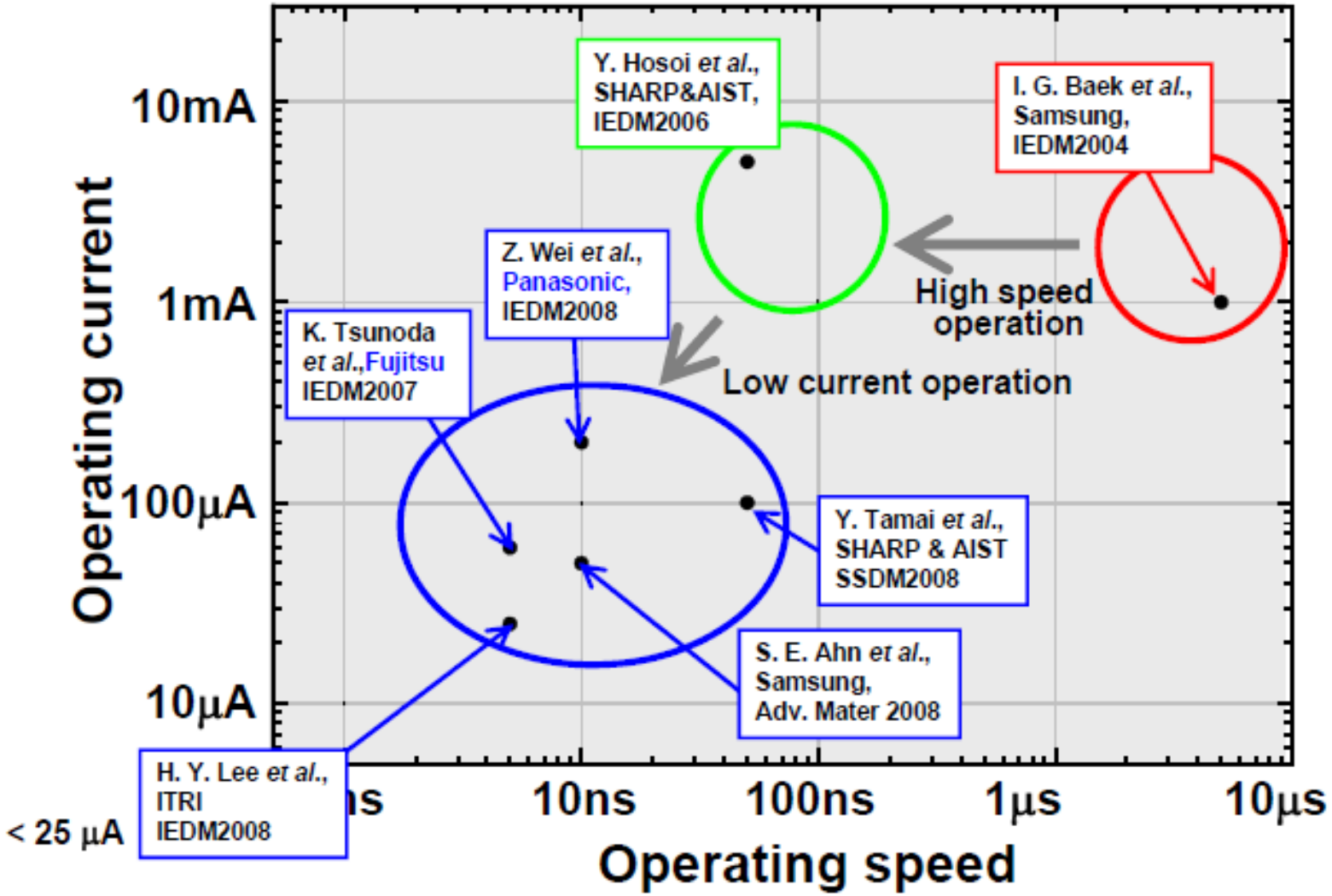
Device → Resistive Switching Behavior

RRAM: Status

RRAM Status

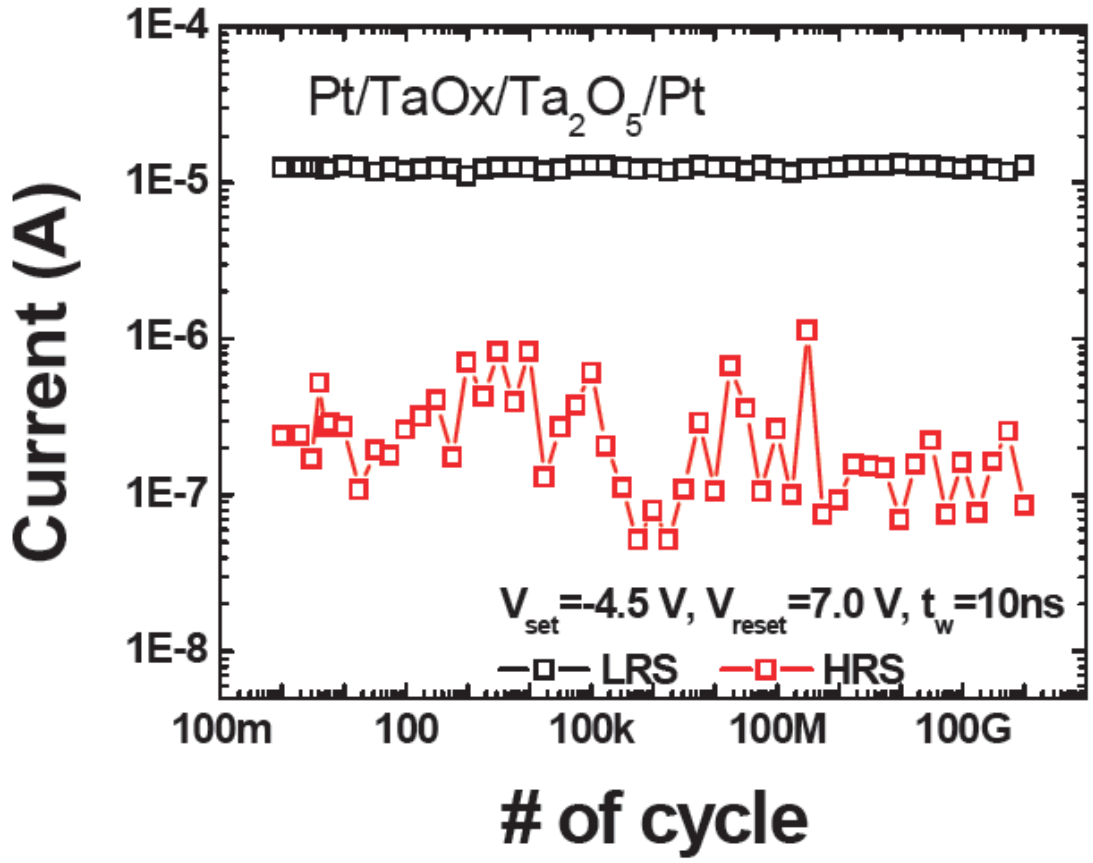
- Performance and Endurance
- Scalability
- Demonstrators
- Product announcements

Steady improvement of RRAM operation speed & current



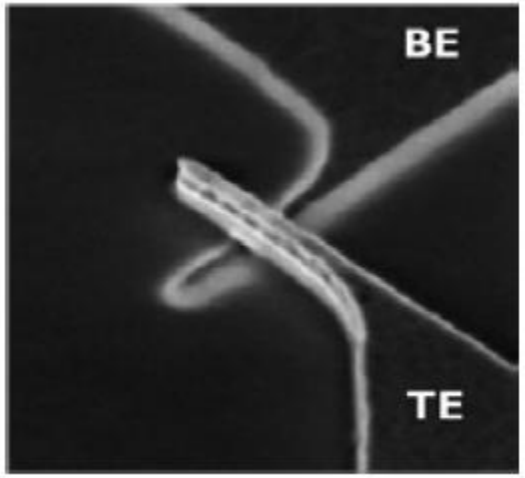
Slide courtesy G.Jurczak, imec

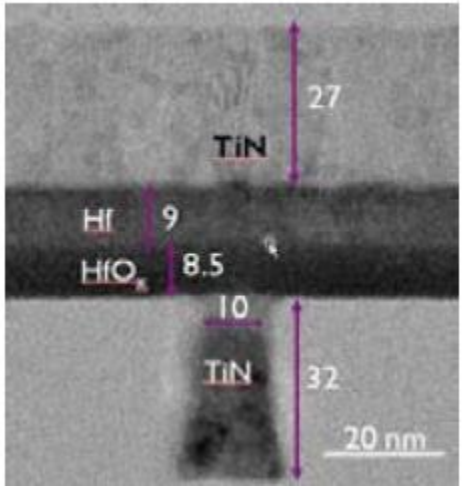
> 10^{12} "unlimited" cyclability in TaOx

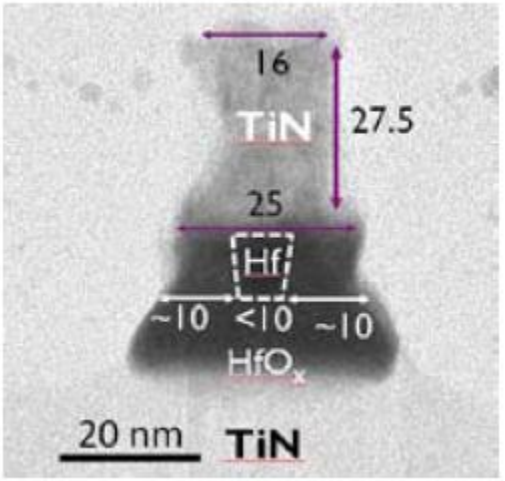


Y-B.Kim et al, VLSI Technology 2011

<10nm scalability of HfO_2 RRAM cells

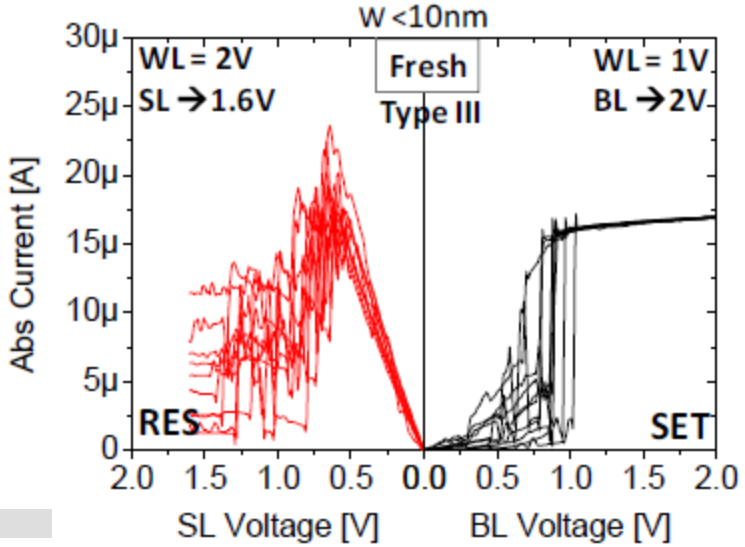




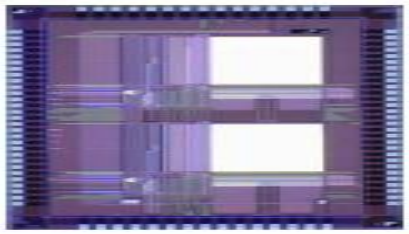


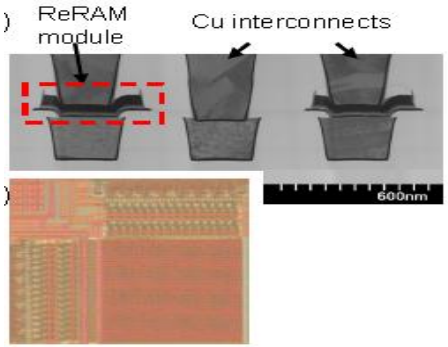
B.Govoreanu et al IEDM 2011

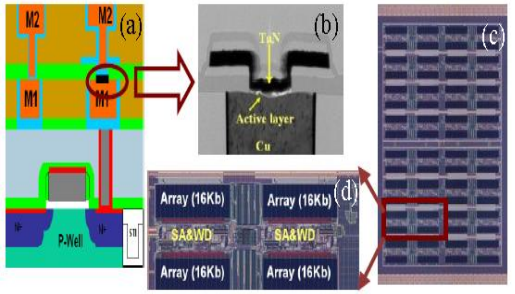
G.Kar et al VLSI 2012

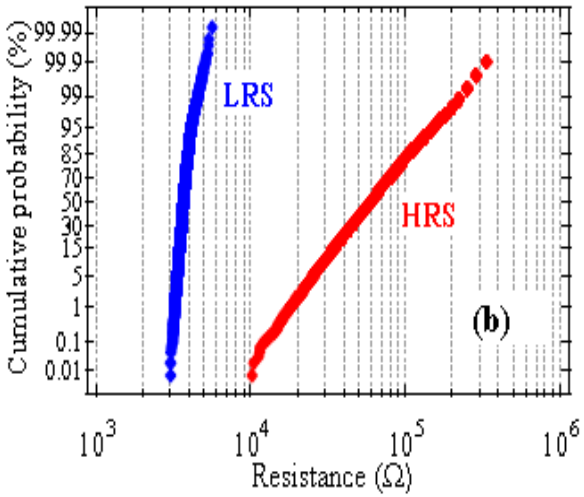


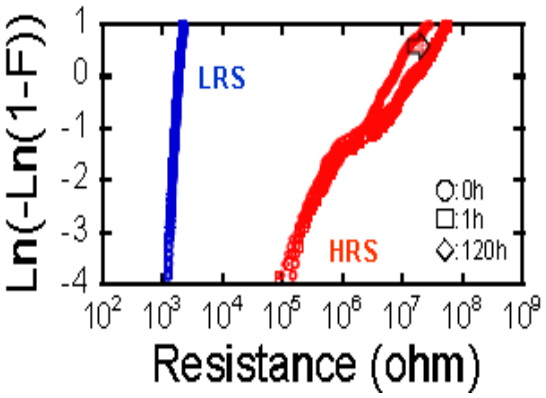
ARRAY DEMONSTRATIONS OF 1T-1R RRAM

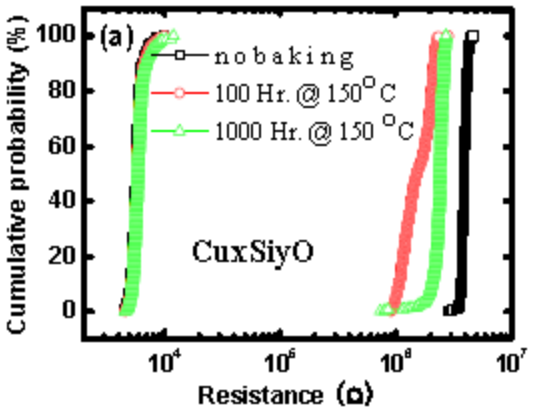












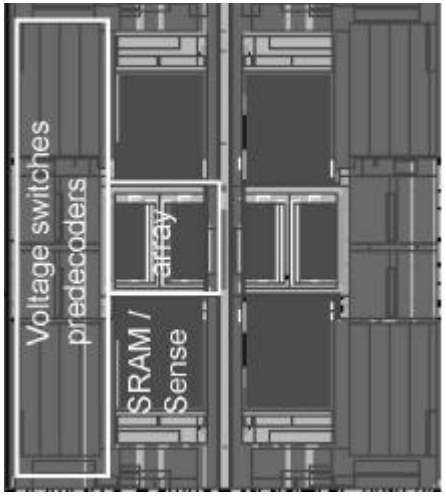
Pt/TaO_x/Pt
8kb bipolar array
Panasonic, IEDM 2008

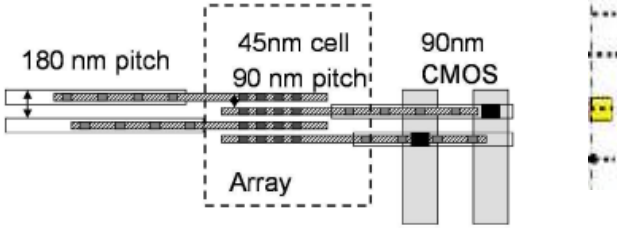
Ru/TiO_x/TaO_x/Ru
1kb unipolar array
NEC, VLSI 2010

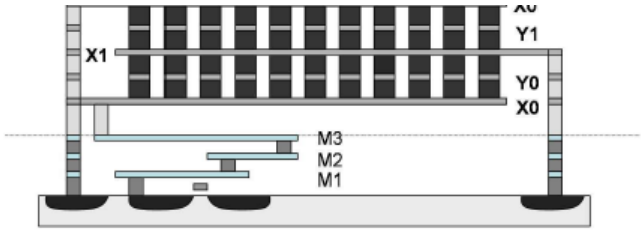
TaN/$CuSi_xO_y$/Cu
1Mb bipolar array
SMIC, VLSI 2010

ARRAY DEMONSTRATIONS OF 1S-1R RRAM

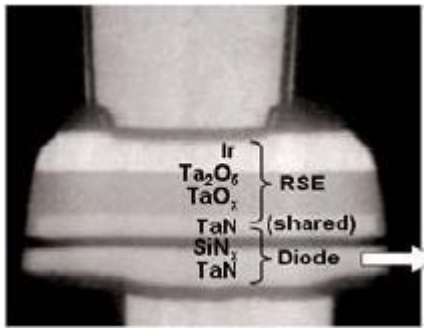
Unity, ISSCC 2010
64Mb, 130nm

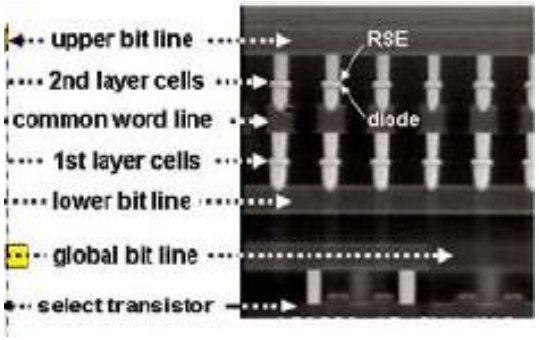


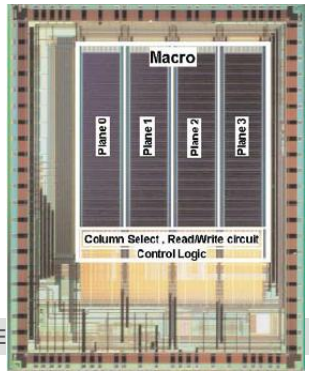




Panasonic, ISSCC 2012
8Mb,







HYNIX, VLSI 2012
54nm CMOS platform

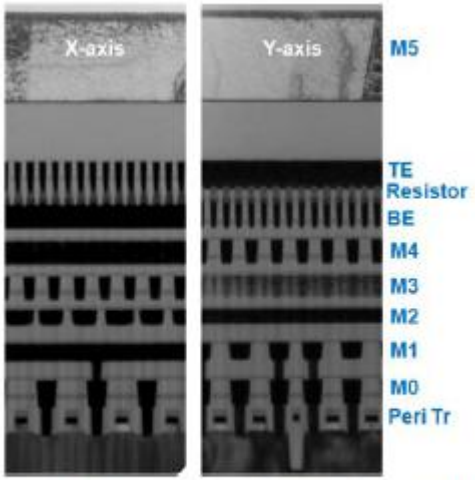
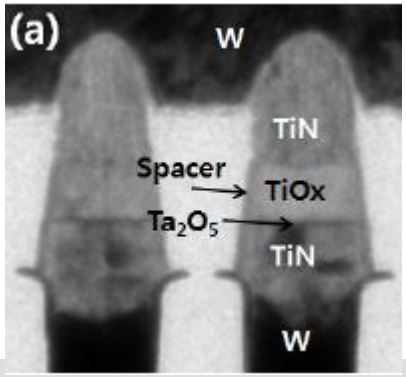


Fig. 1 TEM image of fully integrated crossbar array with the 54nm standard CMOS process technology



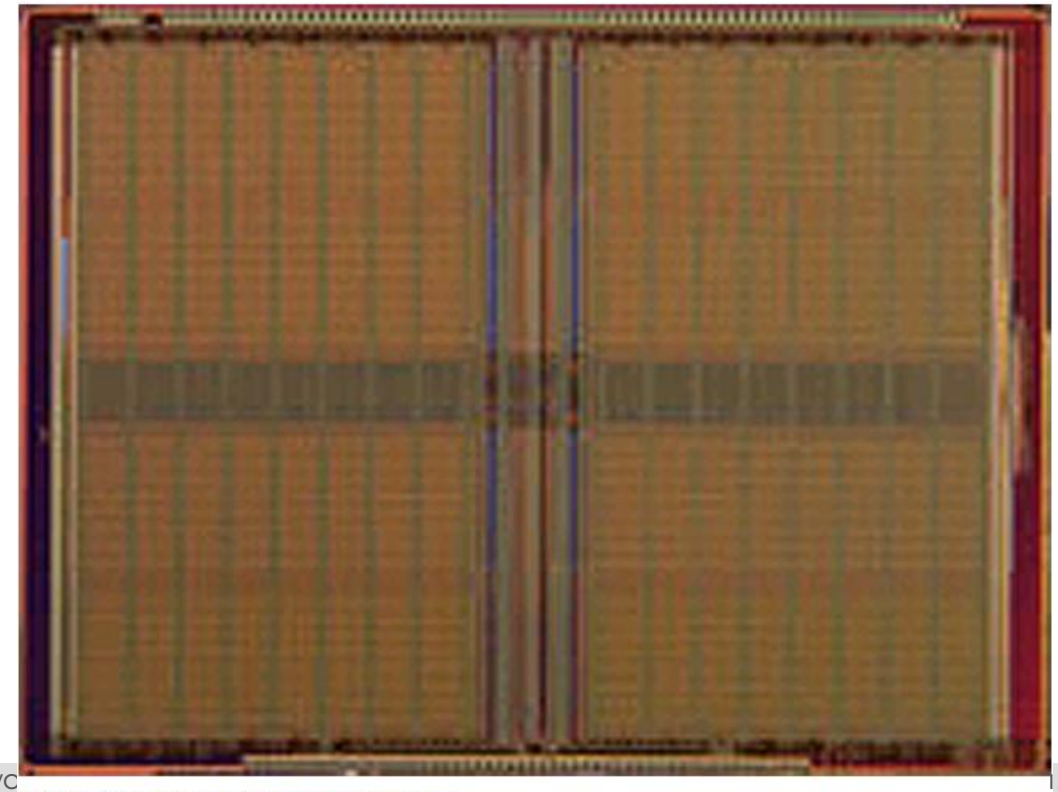
ELPIDA

Elpida announces ReRAM chip, aims to enter market 2013

Peter Clarke

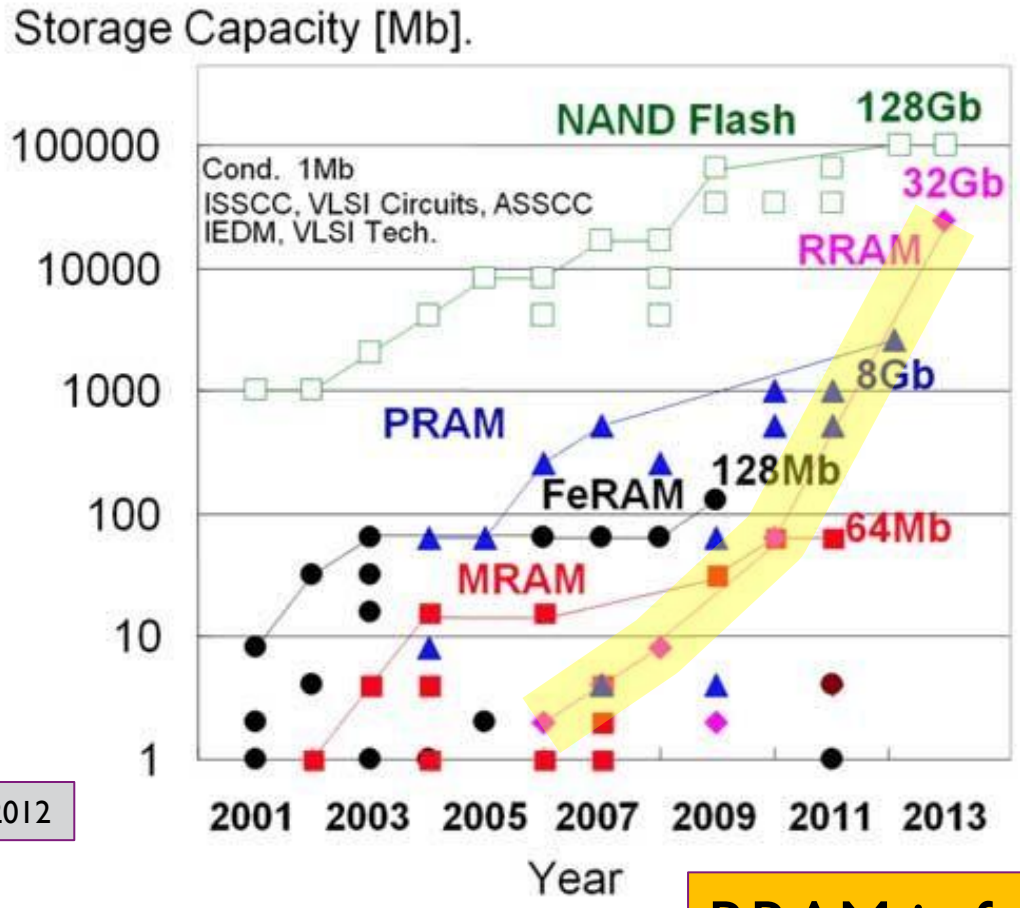
1/25/2012 3:13 PM EST

64Mb, 50nm process,
Collaboration with AIST and SHARP



Elpida Memory, Inc. 64 Megabit prototype ReRAM

Toshiba_Sandisk will announce a 32Gb 1D1R RRAM in 24nm @ ISSCC2013



EETimes Asia 21 Nov. 2012

RRAM is fastly emerging !

Conclusions

- Short introduction in why and how of RRAM
- Exciting material and device research field
  - a lot of understanding during last years
- RRAM emerging to reality ?

43rd IEEE Semiconductor Interface Specialists Conference

Thank You !

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- Many contributions from **the imec RRAM team**, especially: Y.Y.Chen, S.Clima, R.Degraeve, L.Goux, B.Govereanu, G.S.Kar, A.Fantini, L.Zhang
- **Program director** : M.Jurczak
- **Industrial partners** in imec's Core CMOS program

ASPIRE
INVENT
ACHIEVE

imec

	type	PCRAM	OxRRAM	STT-RAM
Operation	Write Speed	>10nsec	~5nsec	~1nsec
	Write current	~10's of uA	~uA's	1-10MA/cm^2
	MLC?	Yes	?	No
	Endurance	10^9	10^{12}	10^{15} (infinite?)
	Ron/Roff	>10^3	10-100	~2
CMOS compatibility	Switching Voltage	2 -4 V	2-4 V (+ needs Forming)	1-2 V
	Materials	GeSbTe	Standard (HfO_2)	NS Metal stacks
	Process limitations	None? (non-standard material)	None	Limited thermal stability
Scalability	Limitations	Current (need sub-litho scaling)	Variability (localized thin filament)	Retention (~Volume)
Configuration	Selector	1D1R	1T1R-1S1R	1T1R
	2D stackable	?	Yes	No
Target applications ?		(NOR-Flash) SCM? Embedded ?	SCM (NAND) Flash Embedded ?	DRAM Embedded ?