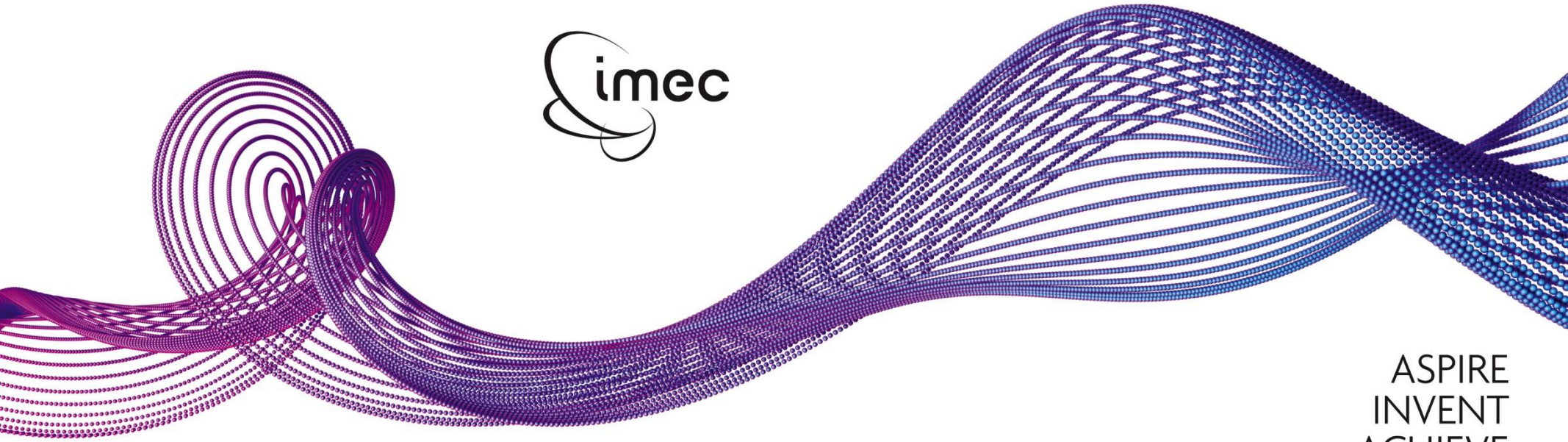
SPIN LOGIC

IULIANA RADU



ASPIRE
INVENT
ACHIEVE

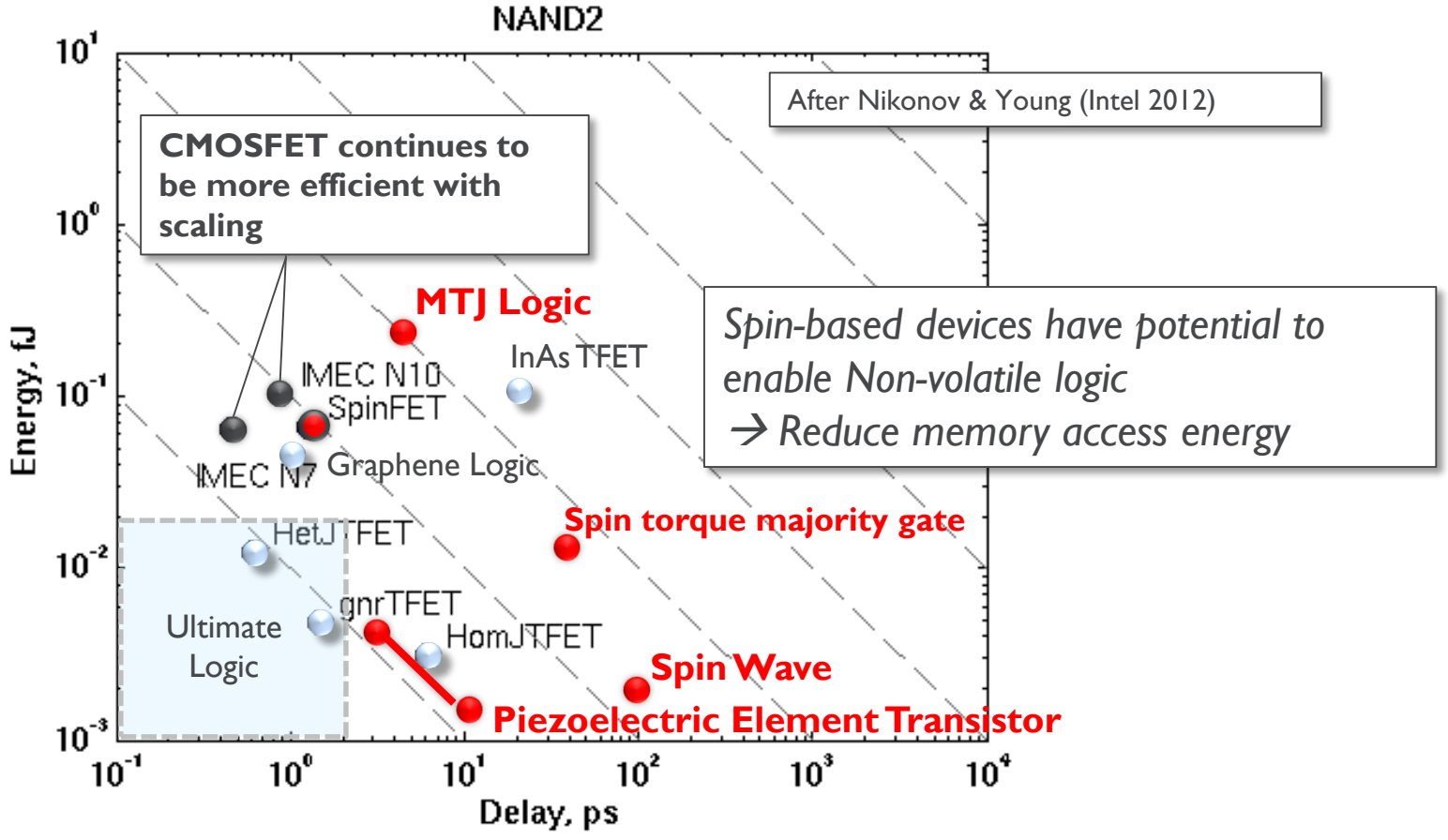
SPINTRONICS

Electronics
Electric charge

Magnetics
Magnetic moment *(spin)*

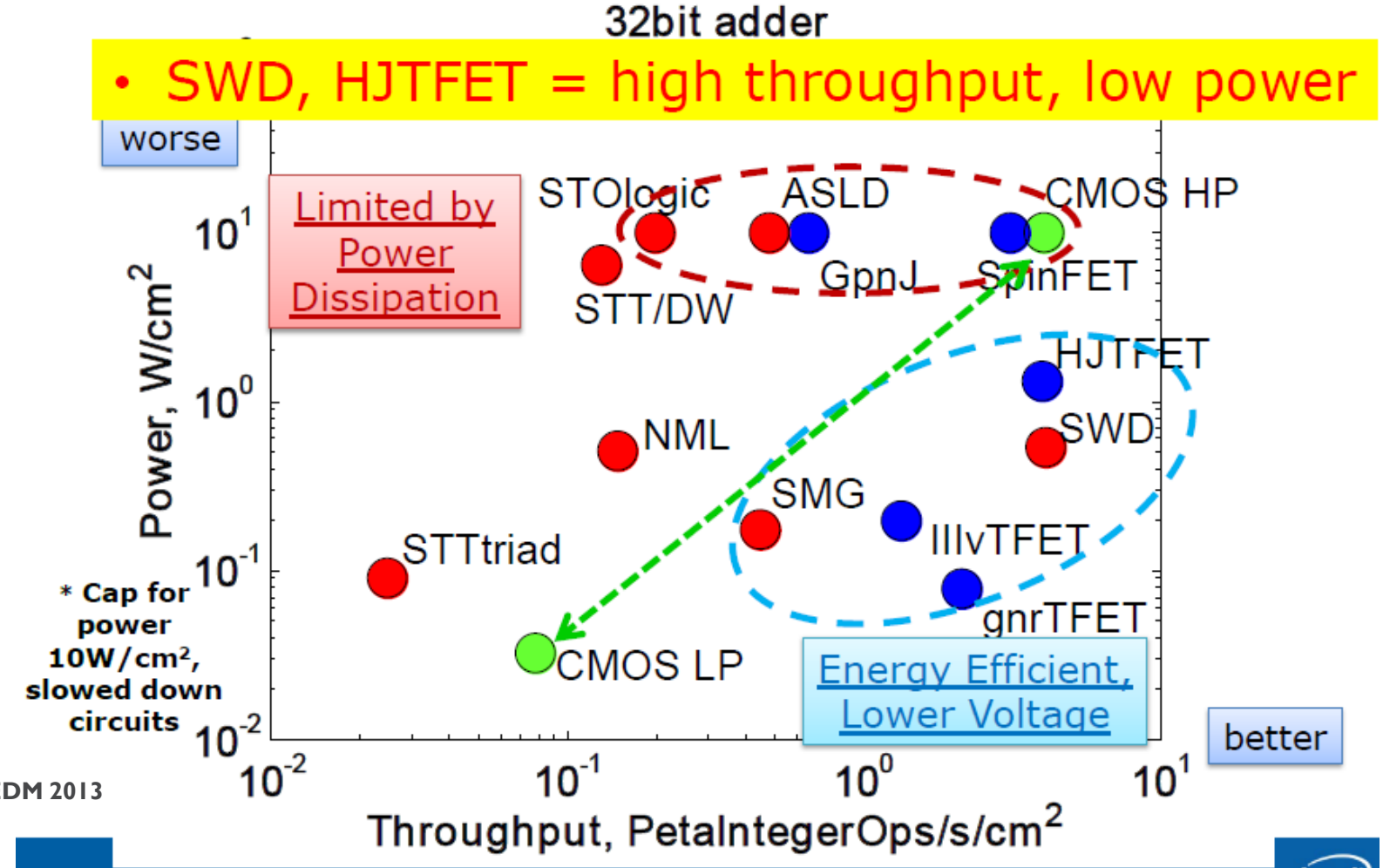
Spintronics
Uses charge and spin for new functions

ENERGY EFFICIENCY BENCHMARK



- Black/Green: Charge-based devices
- **Red: Non-charge** based devices offer different Energy-Delay tradeoffs

Throughput and Power Comparison



Nikonov et al. IEDM 2013

SPINTRONICS - APPLICATIONS

Memory

- MRAM
- STT-MRAM
- Racetrack memory

Logic

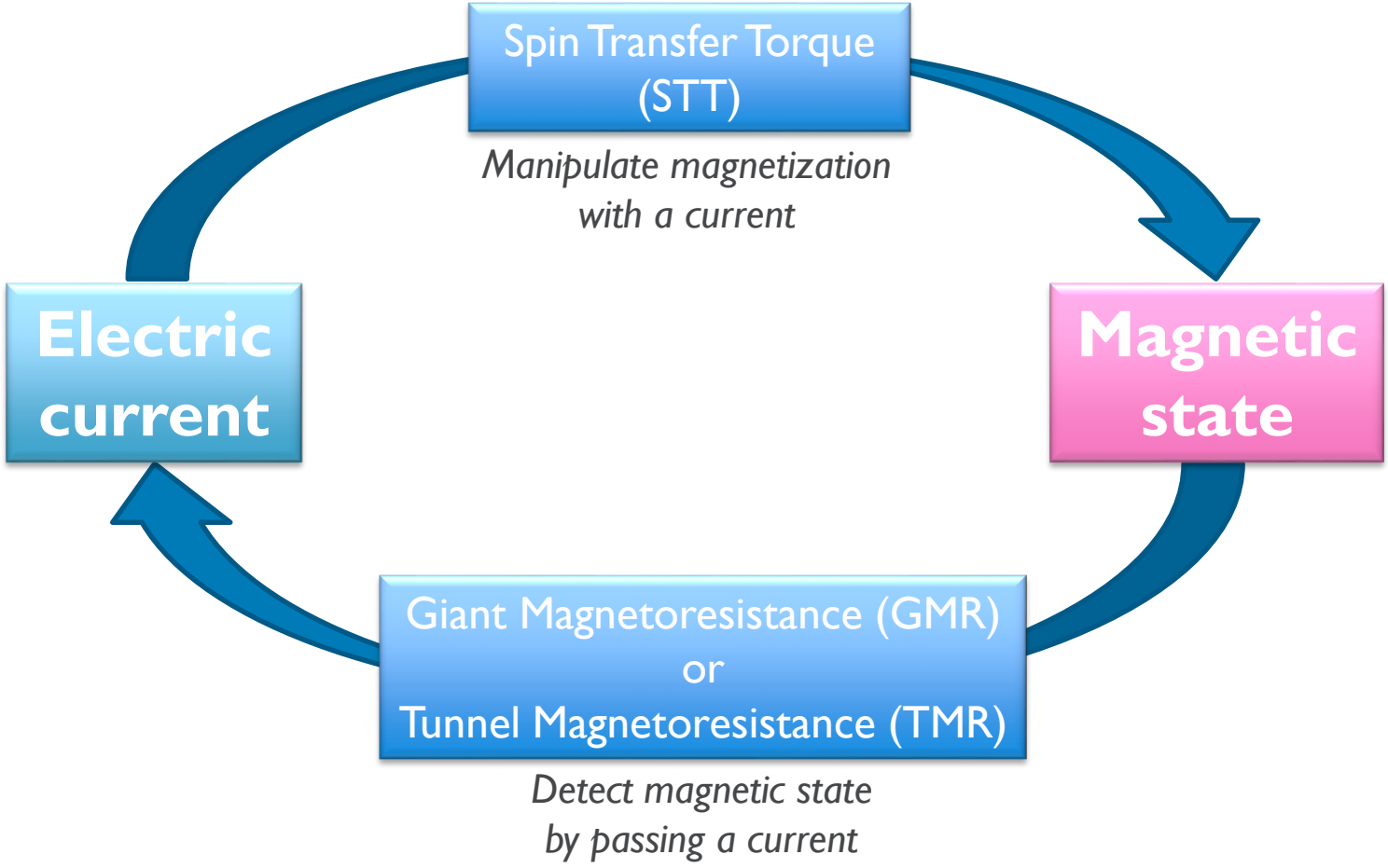
- Shift register
- Majority Gate
- Other logic gates and emerging concepts

Other electronic applications

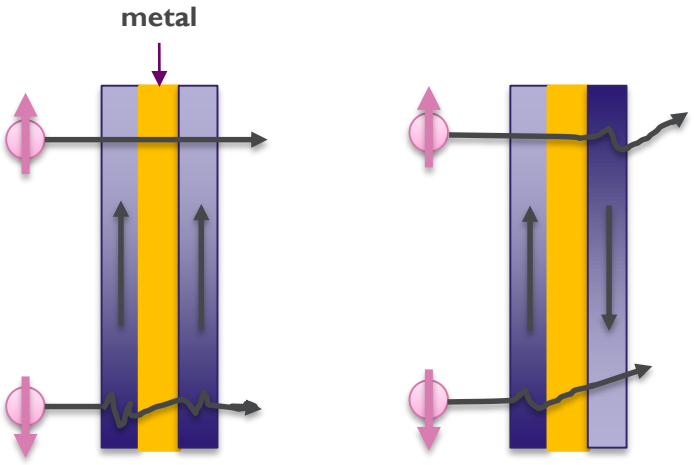
- Spin Torque Oscillator

(Voltage Controlled Oscillator)

SPINTRONICS



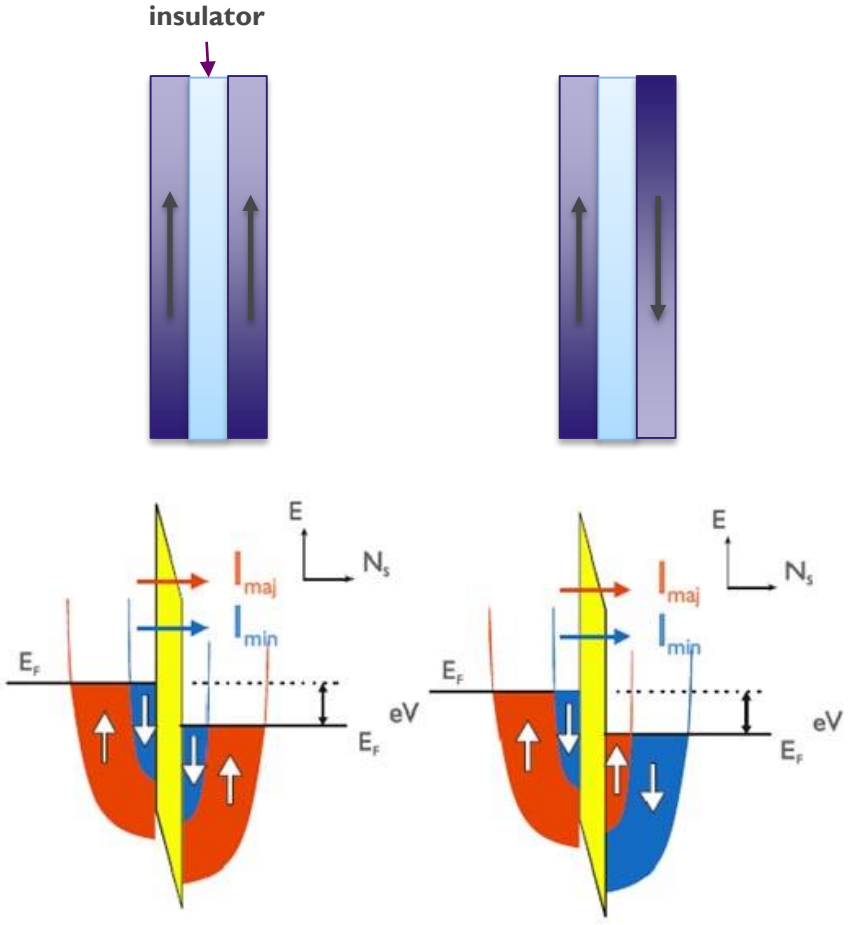
GIANT MAGNETORESISTANCE (GMR)



$$\delta_H = \frac{R_{\uparrow\downarrow} - R_{\uparrow\uparrow}}{R_{\uparrow\uparrow}}$$

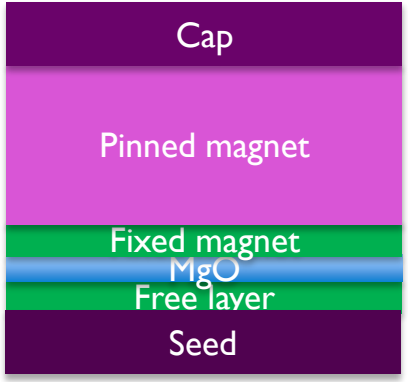
- Magnetoresistance is dependence of electrical resistance on external magnetic field
- Discovered by Fert and Grunberg in 1988.
- Electron scattering depends on relative orientation of electron spins and magnetic moments.
- Different resistance because of different scattering in the magnetic layers.
- Spin valve

TUNNEL MAGNETORESISTANCE (TMR)



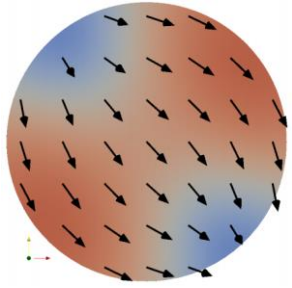
- Effect discovered by Julliere 1975
- Significant step was MgO as tunnel barrier which allows large changes in resistance (Parkin, Yuasa).
- Tunnel magnetoresistance is given by different probability of spin current polarization from the 2 magnets.

MAGNETIC TUNNEL JUNCTION (MTJ)



- They are the basis of MRAM
- If switched via STT, then STT-MRAM
- Stacks are usually much more complicated and consist of superlattices for the pinned magnet to compensate for stray fields
- The free layer is a soft(er) magnet where the magnetization can be switched via various mechanisms
- State of the tunnel junction is read via TMR→ non-volatile memory

THE LLG EQUATION



In micromagnetism:

- Smooth variation of the magnetization $\mathbf{M}(\mathbf{r}, t)$ (continuum)
- Mesoscopic scale: characteristic length $\gg$ size of an atom

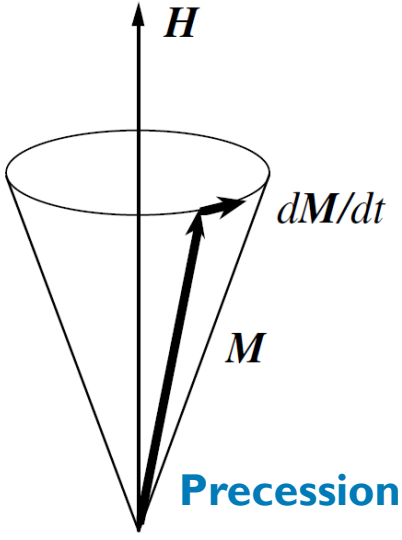
The Landau-Lifshitz-Gilbert (LLG) equation

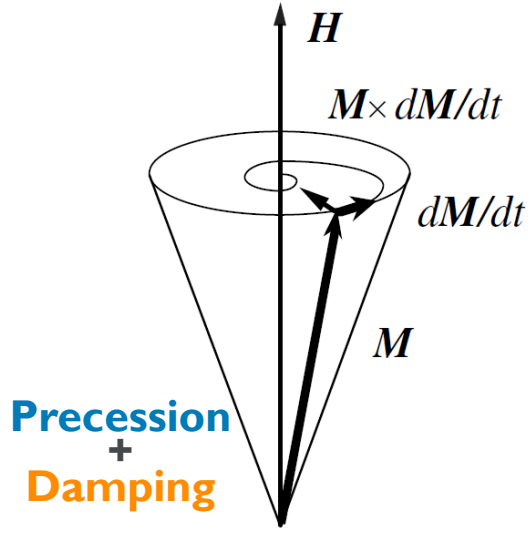
$$\frac{\partial \mathbf{M}}{dt} = \underbrace{-\gamma_0(\mathbf{M} \times \mathbf{H_{eff}})}_{\text{Precession}} \underbrace{+\frac{\alpha}{M_s}\left(\mathbf{M} \times \frac{\partial \mathbf{M}}{dt}\right)}_{\text{Damping}}$$

Precession (energy-conservative)

Damping (dissipative)

$$\mathbf{H_{eff}} = \mathbf{H_{applied}} + \mathbf{H_{ex}} + \mathbf{H_{anis}} + \mathbf{H_{demag}} + \ldots$$





CONTRIBUTING FIELDS

Applied field (H_{app})

Any external field

$$E_{Zeeman} = \mu_0 V \, \mathbf{M} \cdot \mathbf{H_{app}}$$

Exchange field (H_{ex})

- Comes from Pauli exclusion principle
- Tends to align the magnetic moments along the same direction

$$\mathbf{H_{ex}} = -\frac{2A_{ex}}{\mu_0 M_s}\Delta\mathbf{m}$$

$$E_{ex} = \int_{\Omega} A_{ex}\left[(\nabla m_x(\mathbf{r}))^2 + (\nabla m_y(\mathbf{r}))^2 + (\nabla m_z(\mathbf{r}))^2\right] d\mathbf{r}$$

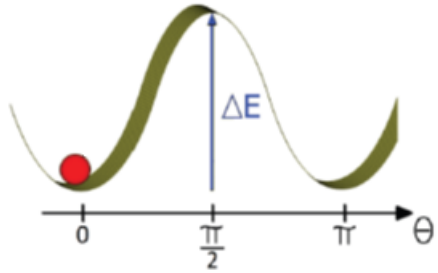
CONTRIBUTING FIELDS

Magnetocrystalline anisotropy (H_{anis})

- Preferred crystalline axis
- Most common case: uniaxial anisotropy ($\mathbf{u_K}$: unit vector)

$$\mathbf{H_{anis}} = \frac{2K_u}{\mu_0 M_s}(\mathbf{u_K} \cdot \mathbf{m})\mathbf{u_K}$$

$$E_{anis} = \int_\Omega K_u \left[1 - (\mathbf{u_K} \cdot \mathbf{m}(\mathbf{r}))^2\right] d\mathbf{r}$$



Interfacial anisotropy

$$\epsilon_{s,Néel} = K_s \left[1 - (\mathbf{m} \cdot \mathbf{n})^2\right]$$ → Changes the boundary conditions

↳ Energy / unit surface

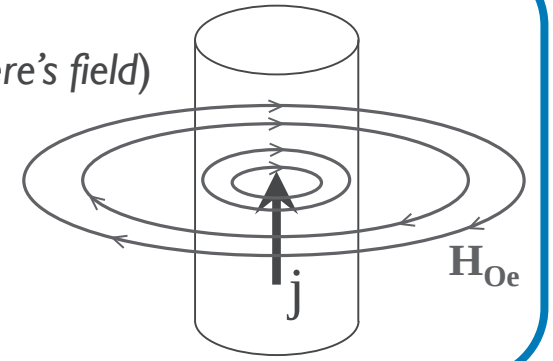
Louis Néel. *Journal de Physique et Le Radium*, **15** (4), 225–239 (1954).

CONTRIBUTING FIELDS

Oersted field

- Field generated by a current (also called *Ampère's field*)
- Calculated from Maxwell equation
- Can be considered as an external field

$$\nabla \times \mathbf{H_{Oe}} = \mathbf{j}$$



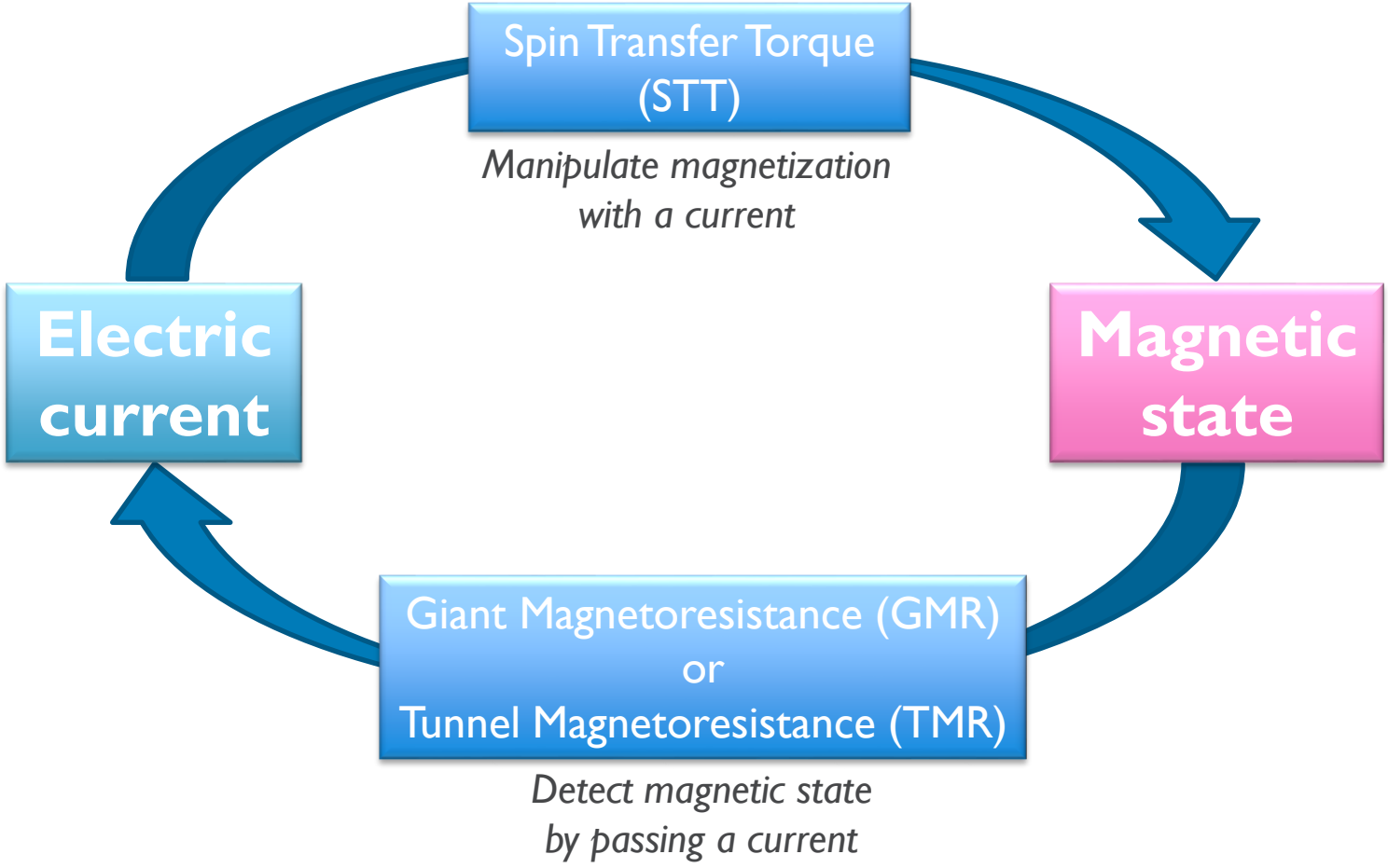
Magnetoelastic interaction

Inverse magnetostrictive effect (Villari effect): magnetic field due to a strain.

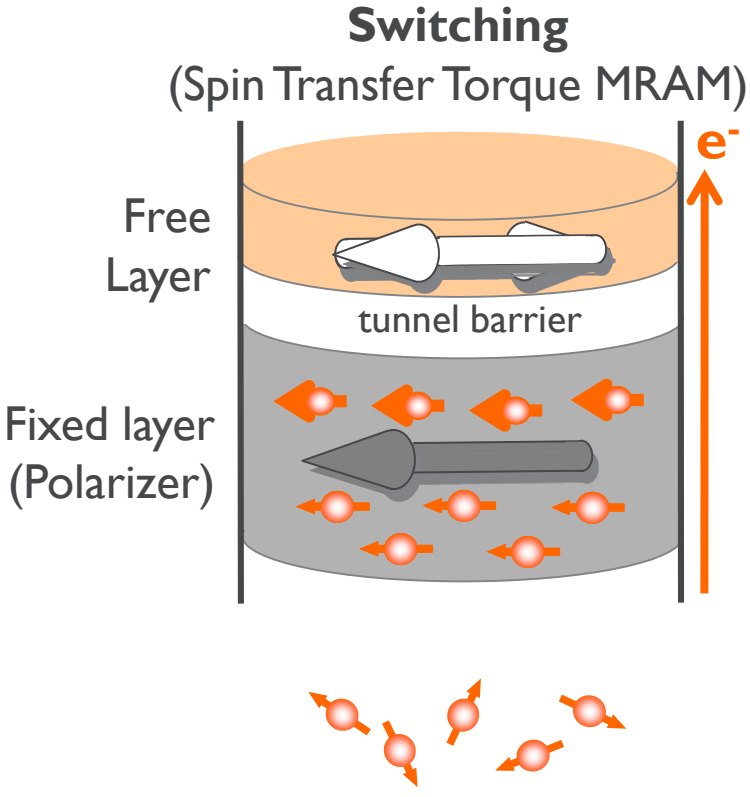
$$\mathbf{H_{elas}} = \frac{3\lambda_s \sigma}{\mu_0 M_s} (\mathbf{m} \cdot \mathbf{u_\sigma})\, \mathbf{u_\sigma}$$

$$\mathbf{E_{elas}} = -\int_\Omega \frac{3\lambda_s \sigma}{2} (\mathbf{m} \cdot \mathbf{u_\sigma})^2 \, d\mathbf{r}$$

SPINTRONICS



THE SPIN TRANSFER TORQUE



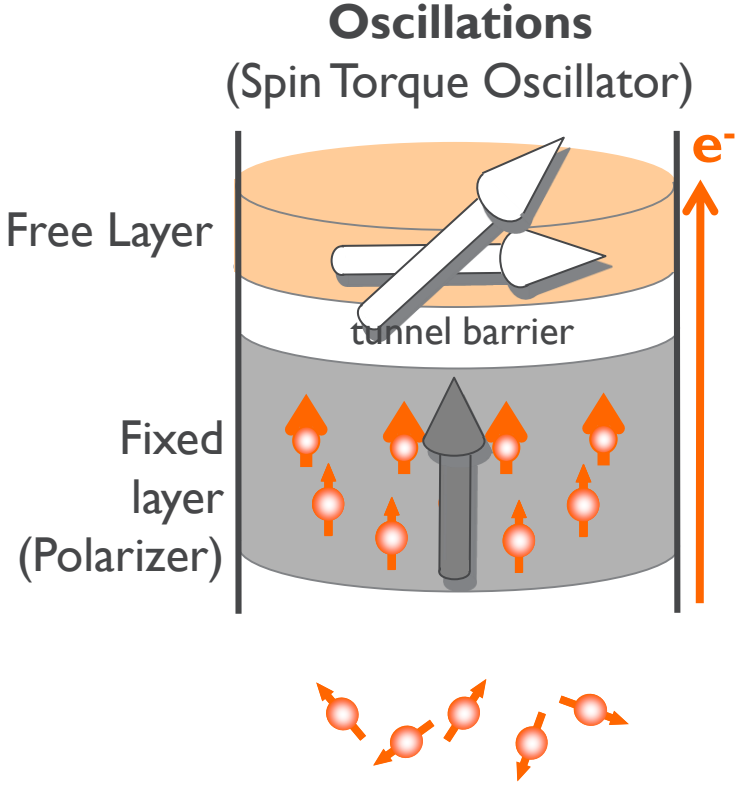
Spin Transfer Torque:
Action of the spin-polarized current on the magnetization

The tunnel barrier (usually MgO) acts as a 'spin filter':

- ✓ enhanced writability
- ✓ enhanced read-out signal (TMR)

TMR = Tunnel Magneto-Resistance:
Change of resistance depending on magnetic orientation (read-out signal).

THE SPIN TRANSFER TORQUE



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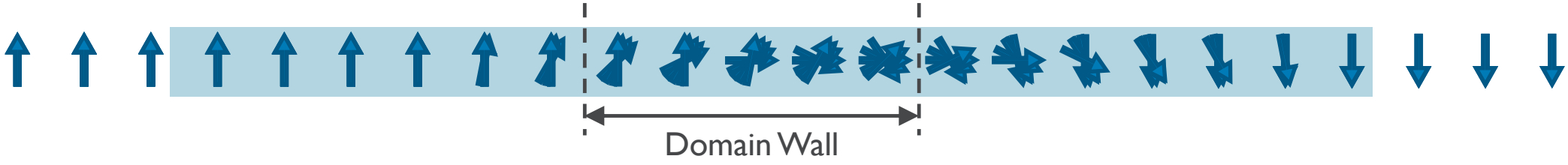

Generalized LLG equation (for Current In-Plane)

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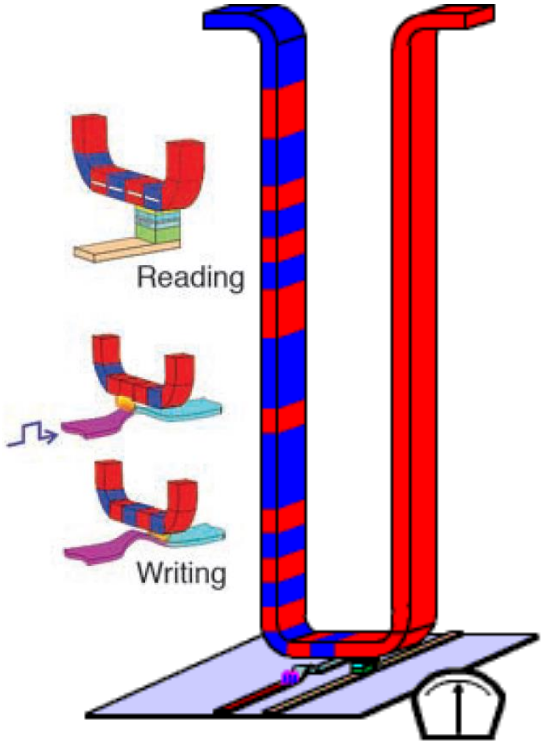
L. Berger, JAP **49**, 2156 (1978)
S. Zhang and Z. Li, PRL, **93**,127204 (2004)
A. Thiaville *et al.*,Y.. *Europhysics Letters*, **69**, 990 (2005)
J. Xiao *et al*, PRB, **73**, 054428 (2006)
I. Garate *et al.*, Phys. Rev. B 79, 104416 (2009).

$\mathbf{u} \propto J$ *(current density)*

OTHER APPLICATIONS: THE RACETRACK MEMORY



http://researcher.watson.ibm.com/researcher/view_group_subpage.php?id=3811

Magnetic domain-wall racetrack memory

S. S. P. Parkin *et al.* Science, **320**, 190 (2008)

- Non-volatile memory
- (Potentially) very fast and reliable
- Potentially 3D
- Could be used for logic (shift register)

Since 2008, improvements (due to Spin Hall, Rashba, Dzyaloshinskii–Moriya interaction...)

- Higher speed (up to 750m/s*)
- Promise of lower currents

*S. S. P. Parkin, *Highly Efficient Exchange-Coupling Torque Driven Domain-Wall Velocities in Synthetic Antiferromagnet Racetracks*, MMM Conference (2014).

MAGNETOELECTRIC EFFECT

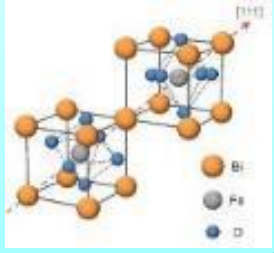
Conversion from charge to spin domain by **voltage control** is most energy efficient method.
Several physical effects that can come into play.

Multiferroic materials

Few materials multiferroic at room temperature

$BiFeO_3$

Weak effect



Synthetic multiferroics

Stacks of piezoelectric and magnetostrictive materials

Stronger effect, but complicated materials

Magnetostrictive

Piezoelectric

Interfaces

Tune magnetic anisotropy at magnetic metal/ oxide interface with an electric field (very thin metal).

Interesting effect

Temperature sensitive

SPINTRONICS

Electronics
Electric charge

Magnetics
Magnetic moment *(spin)*

Spintronics
Uses charge and spin for new functions

SPINTRONICS - APPLICATIONS

Memory

- MRAM
- STT-MRAM
- Racetrack memory

Logic

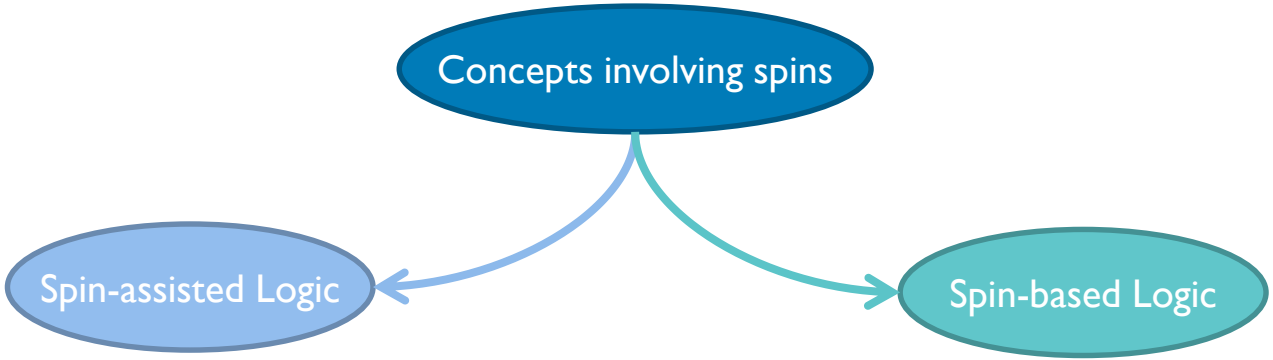
- Shift register
- Majority Gate
- Other logic gates and emerging concepts

Other electronic applications

- Spin Torque Oscillator

(Voltage Controlled Oscillator)

SPINTRONIC LOGIC



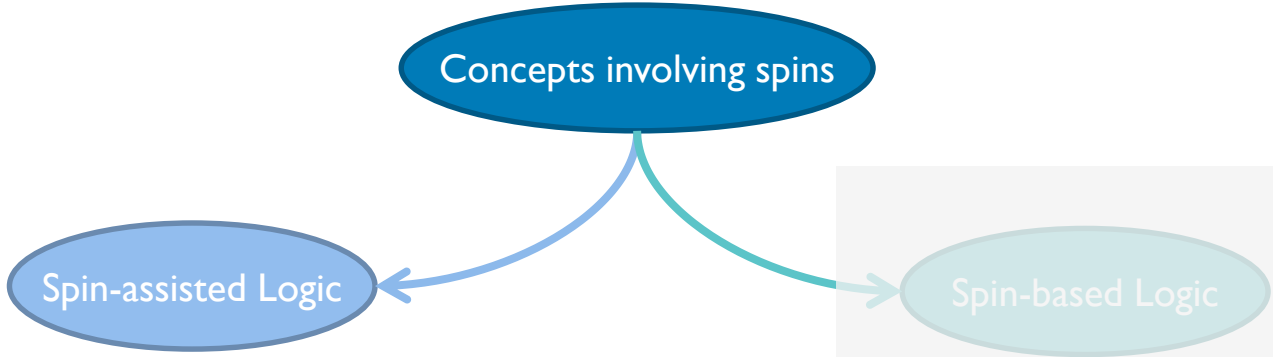
Spins are involved in the computation but electrical input and output is required

Datta-Das Spin modulator
Sugahara-Tanaka Spin-FET
NV MTJ-enhanced logic

Pure spin input and output

Magnetic cellular automata
Domain wall logic
All-spin logic,
Spin Wave devices

SPINTRONIC LOGIC



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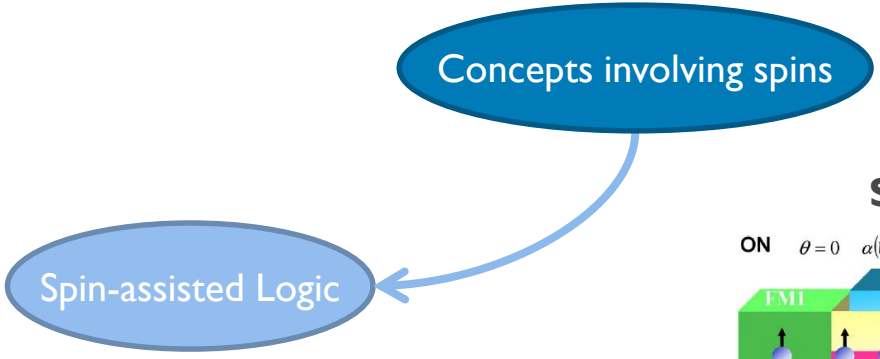
SPIN-ASSISTED LOGIC



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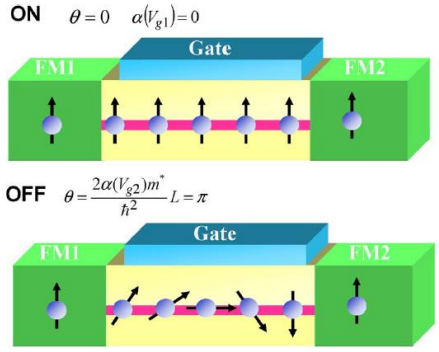
Sugahara-Tanaka Spin-FET

Spin FET

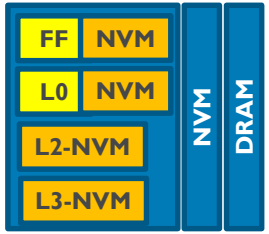


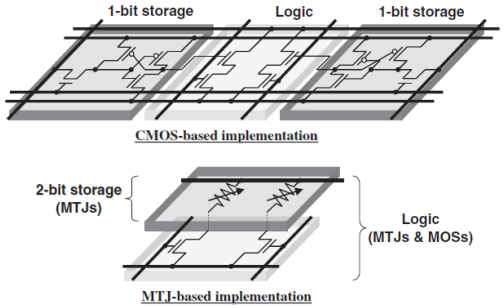
Sugahara *et al.*, Proceedings of the IEEE , **98**, 2124 (2010)

- Advantages
  - fast transit and long spin diffusion length
- Challenges:
  - MR readout, materials, Rashba spin control, Temperature.
  - Inefficient encoding due to spin info on top of charge

MTJ ENHANCED LOGIC

NV on-chip logic





Matsunaga *et al.*, Appl. Phys. Expr. **2**, 023004 (2009)

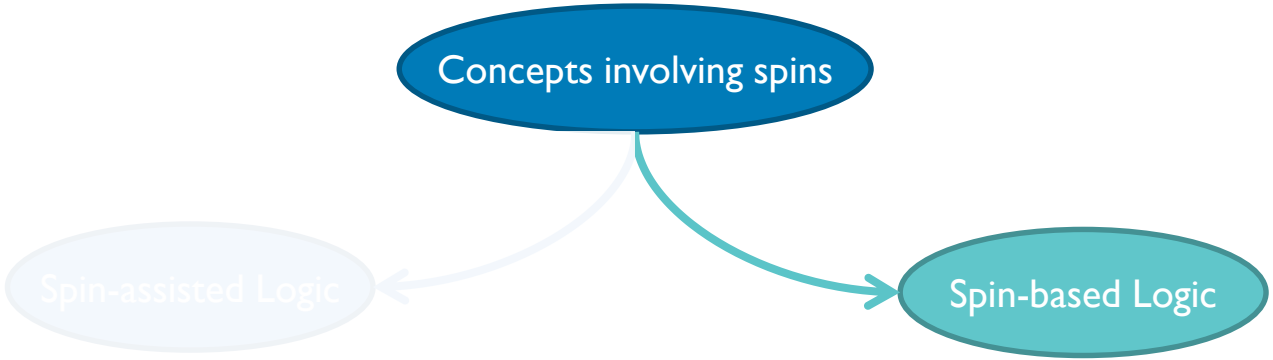
Expected for targets for 14nm logic base line

	NV FF	L0(SRAM)
Capacity – [KB]	1-4KB	32KB
Height – [nm]	60nm	60nm
Overall Area – [F^2]	4320xF^2	210F^2
Latency – CPU cycles	1	1
Read time at Vdd=0.8V @ array	10 ps @ cell	1 ns
Write time at Vdd=0.8V @ array	10 ps @ cell	1 ns
Erase time	10 ps @ cell	-
Retention time	N/A	>10 years
Write endurance [cycles]	>1e16	>1e16
Write operating voltage	0.6V	0.6V
Read operating voltage	0.6V	0.6V
Write energy per cell – [fJ/bit]	0.3 fJ/bit	0.5 fJ/bit

- Advantages
  - Scalability, non-volatility, CMOS-friendly
- Challenges
  - Performance and energy consumption
  - Overhead by adding MTJ to circuit/ architecture
  - Current MTJ speeds suit L3 and L2 replacements

NV MTJ-enhanced logic is promising but key challenges must be addressed

SPINTRONIC LOGIC



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Pure spin input and output

Magnetic cellular automata
Domain wall logic
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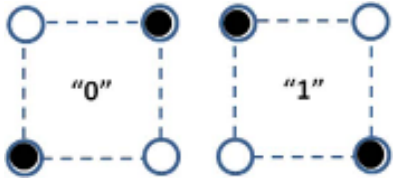
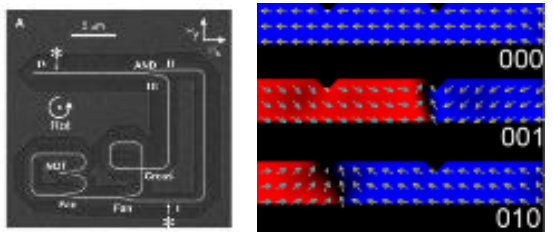
SPIN-BASED DEVICES



Wolf *et al.,* Proceedings of the IEEE , **98**, 2155 (2010)

Magnetic Cellular automata

Pros: non-volatility, scalability, simple physics
Cons: speed, CMOS- compatible materials?

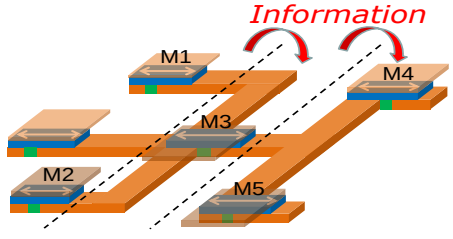


Alwood *et al*., Science **309**, 1688 (2005)

Kunz *et al*., SPIE Newsroom **1**, 1 (2010)

Domain Wall logic

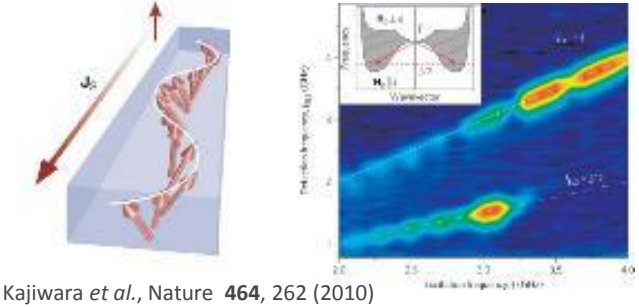
Pros: non-volatile gate, resonant clock networks
Cons: scalability & defects, DW speed (1500 m/s)



Sarkar *et al.,* IEDM 2012, 11.1

All-spin logic

Pros: Fast, energy efficient, non-volatile & materials
Cons: Simulations only, low temperatures



Kajiwara *et al.*, Nature **464**, 262 (2010)

Kurebayashi *et al.*, Nature Material **10**, 660 (2011)

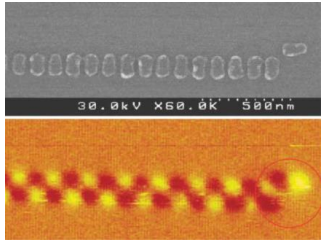
Spin-wave based devices

Pros: phase-encoding, multifunction circuit
Cons: materials and SW speed (10^5 m/s)

MAGNETIC QUANTUM CELLULAR AUTOMATA

MQCA

Majority Logic Gate

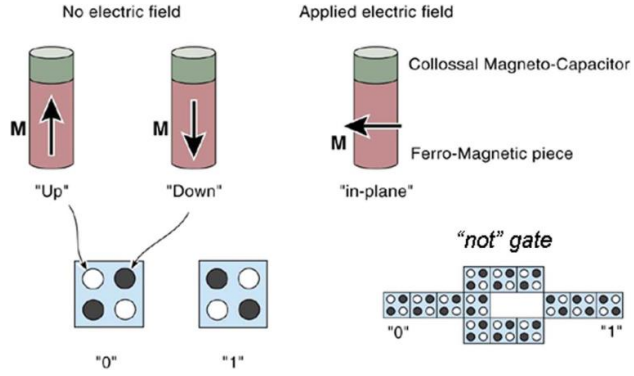


The antiferromagnetic ordering along the chain is controlled by an additional, horizontally oriented elongated driver magnet

Imre *et al.*, Science **311**, 205 (2006)

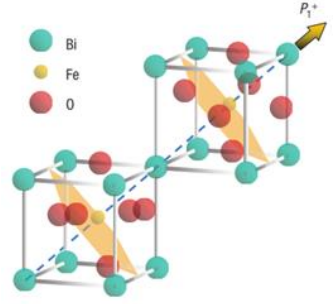
- Technology
  - MQCA: dipolar exchange interactions
  - RAMA: reconfigurable array of magnetic automata
  - Multiferroics with polymeric self-assembly fabrication
- Operation
  - MQCA: magnetic fields applied fields
  - RAMA: voltage-induced stress on ferromagnet
- Challenges:
  - Power, speed and CMOS-compatible materials

RAMA



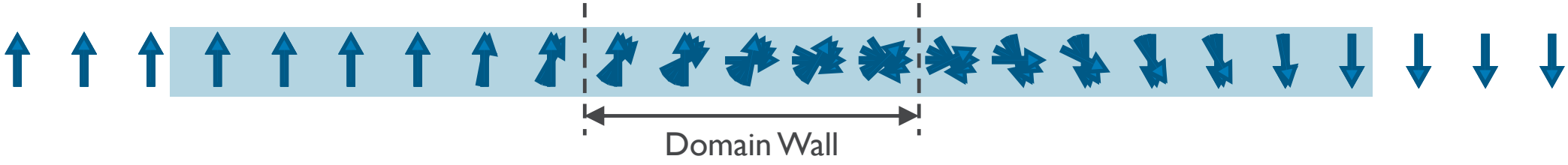
Wolf *et al.,* Proceedings of the IEEE **98**, 2155 (2010)
Kabir *et al.,* Proceedings of GLSVLSI, 25 (2011)

BiFeO3 – multiferroic pillars



Zhao *et al.*, Nature materials **5**, 823 (2006)

THE SPIN TRANSFER TORQUE



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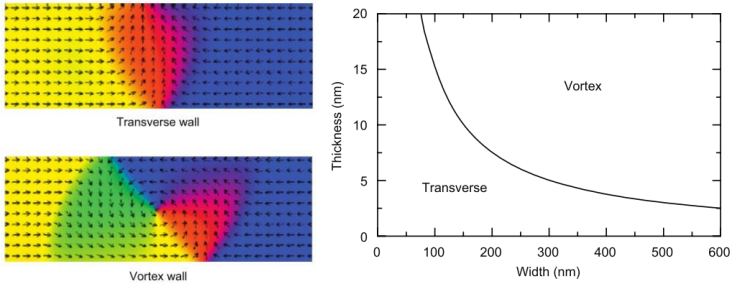
J. Xiao *et al*, PRB, **73**, 054428 (2006)
I. Garate *et al.*, Phys. Rev. B 79, 104416 (2009).

$\mathbf{u} \propto J$ *(current density)*

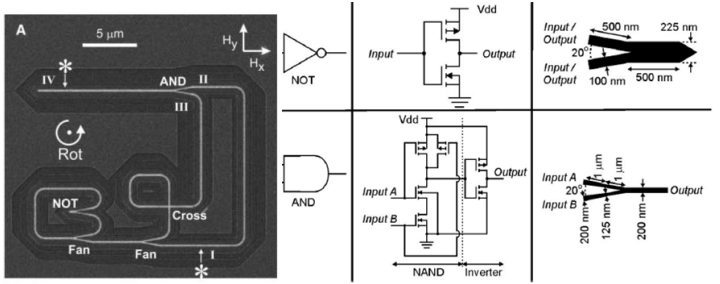
DOMAIN WALL LOGIC

DW types and dimensions



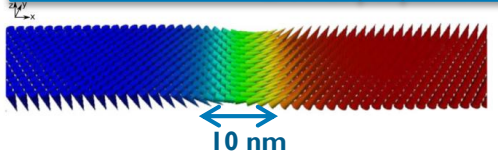
Beach, JMMM 320, 1272 (2008)

DW logic gates

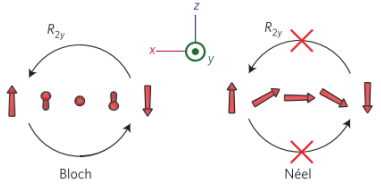


Alwood *et al.*, Science **309**, 1688 (2005)

DW in perpendicular materials



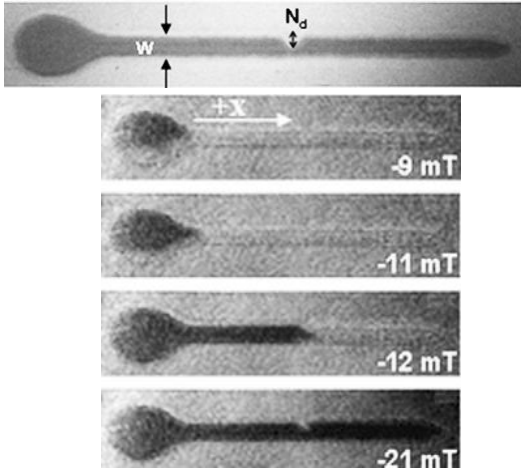
Albert *et al.*, JPCM **24**, 024219 (2012)



Haazen *et al.*, Nat Mat **12**, 1 (2013)

- Technology
  - Encoding in DWs → spin ensemble
  - Several bits per line → wire geometry allows logic gates
- Operation
  - DW control with current or voltage
- Challenges:
  - Power, scalability, DW pinning and creep

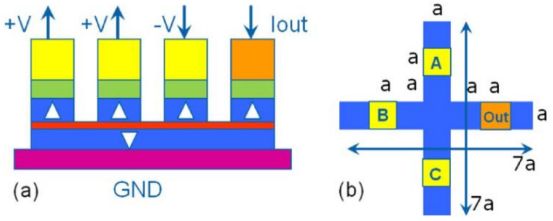
DW propagation and pinning



Im *et al.*, JPCM **24**, 024203 (2012)

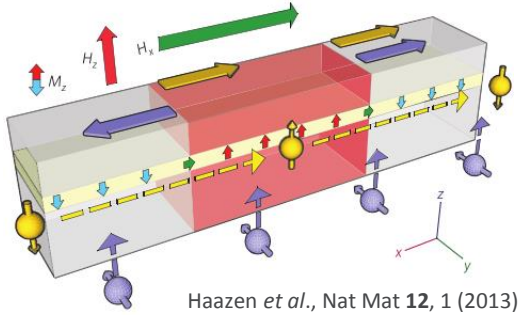
DOMAIN WALL LOGIC CONCEPTS

Spin-torque Majority Gates



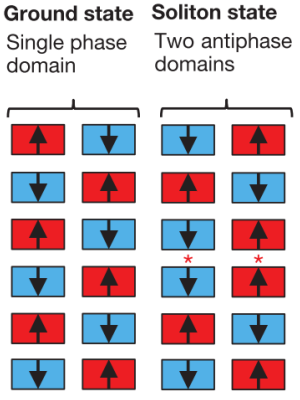
Nikonov *et al.*, IEEE EDL **32**, 1128 (2011)

Pure spin current DW depinning



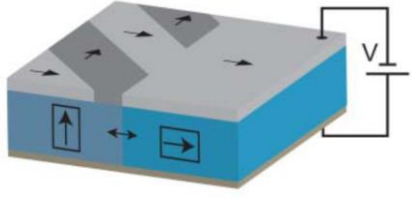
Haazen *et al.*, Nat Mat **12**, 1 (2013)

3D shift register of solitons



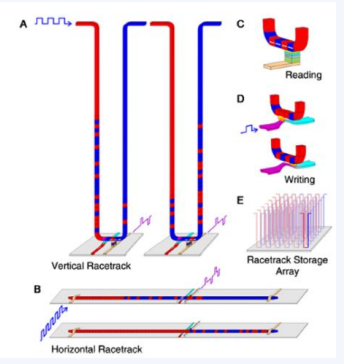
Lavrijsen *et al.*, Nature **493**, 647 (2013)

Voltage-driven DWs in Multiferroics



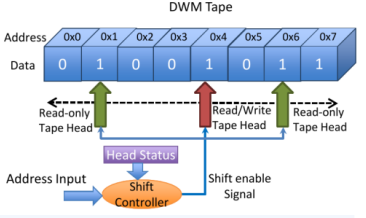
Lahtinen *et al.*, Scientific reports **2**, 258 (2012)

Racetrack Memory



Parkin *et al.*, Science **320**, 190 (2008)

TapeCache

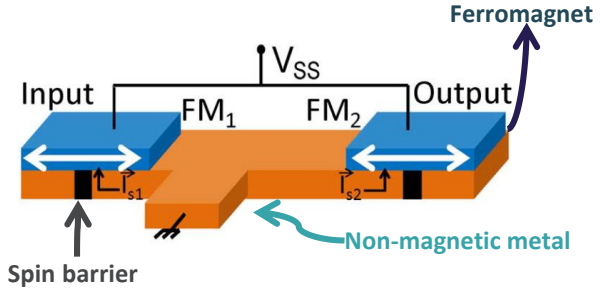


Venkatesan *et al.*, ISLPED'12

DW memory is fast enough (1500 m/s) to be considered for L1 replacement

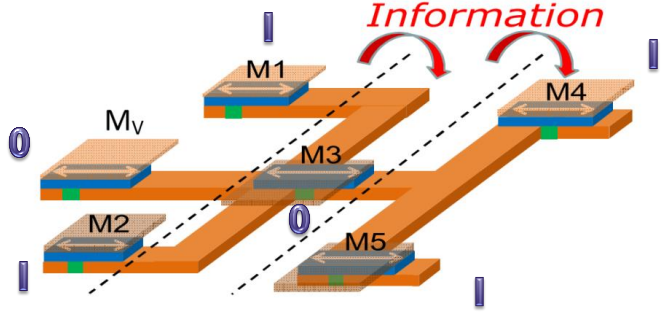
ALL SPIN LOGIC

ASL device



Srinivasan *et al.*, IEEE Trans. Mag **47**, 4026 (2011)

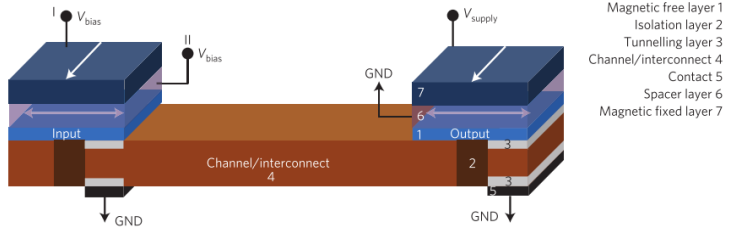
NAND gate proposal



Sarkar *et al.*, IEDM 2012, 11.1

- Technology
  - Binary data stored in magnets
  - Fast, energy efficient, non-volatile
- Operation
  - Prompt conversion from charge to spin.
  - Voltage over bits with pure spin current propagation
  - MTJ readout
- Challenges:
  - No demonstrator at RT
  - Very low T for long spin diffusion.
  - High anisotropy materials for enough thermal stability
  - Suitable materials for conducting channels

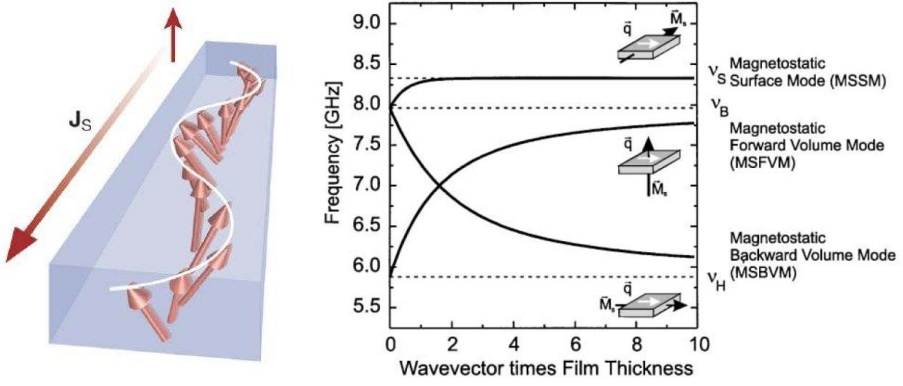
ASL device with built-in memory



Behin-Aein *et al.*, Nat. Nano **5**, 266 (2010)

SPIN WAVE LOGIC

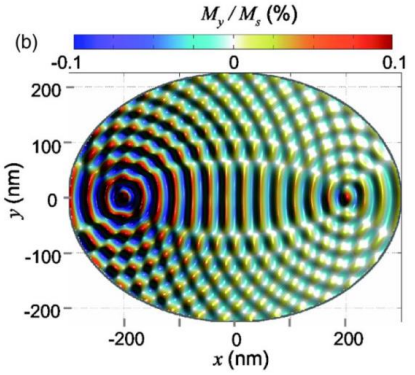
Spin Wave and its excitation modes



Kajiwara *et al.*, Nature **464**, 262 (2010)

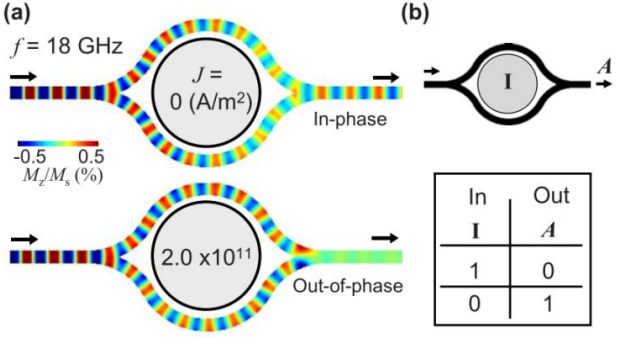
Demokritov *et al.,* Physics Reports **348** 441 (2001)

Computation via interference



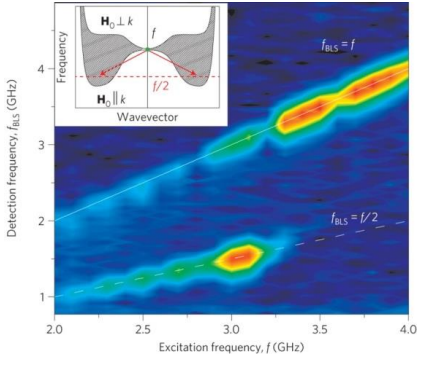
Choi *et al.*, Appl. Phys. Lett. **90**, 083114 (2007)

Mach–Zehnder-type SW interferometer



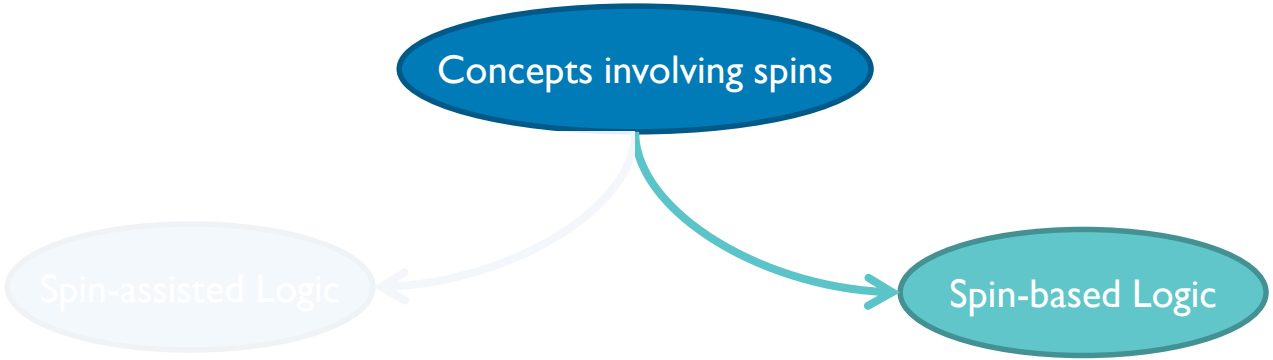
Lee *et al.*, J. Appl. Phys. **104**, 053909 (2008)

Multiple excitation frequencies



Kurebayashi *et al.*, Nature Material **10**, 660 (2011)

SPINTRONIC LOGIC



Spins are involved in the computation but electrical input and output is required

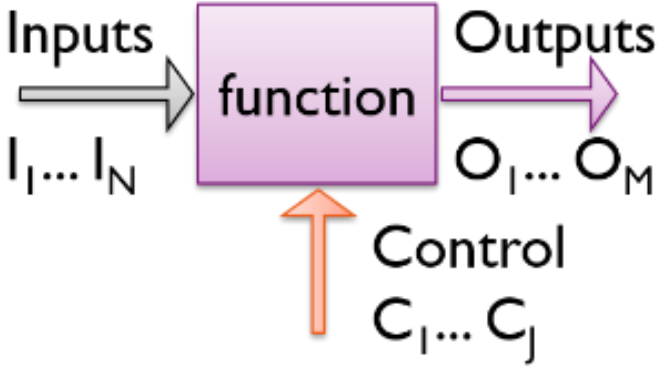
Datta-Das Spin modulator
Sugahara-Tanaka Spin-FET,
NV MTJ-enhanced logic

Pure spin input and output

Magnetic cellular automata
Domain wall logic
All-spin logic
Spin Wave devices

MAJORITY GATES

Majority Logic Gate			
Input 1	Input 2	Input 3	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



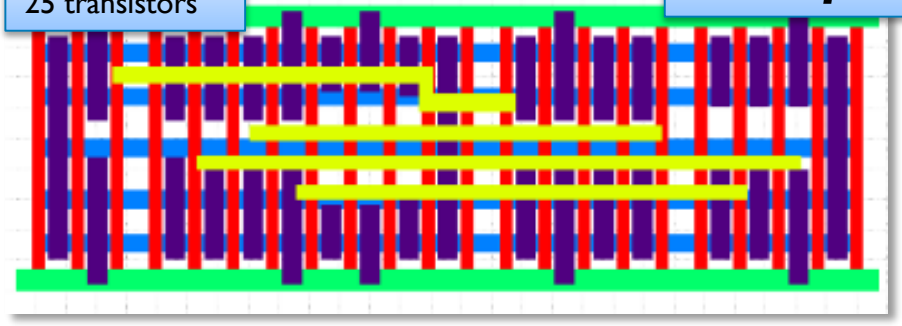
Truth table of a simple 3 input 1 output majority gate
Universal logic= majority gate+ inverter

Arithmetic circuits can be more efficiently built using majority gates rather than NAND or XOR

Envision devices with large number of inputs and control gates and a large number of complex outputs, reducing the complexity of the circuits

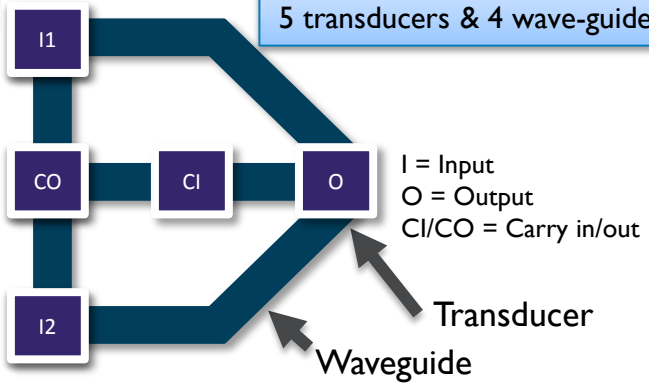
FUNCTIONAL SCALING

CMOS circuit
25 transistors

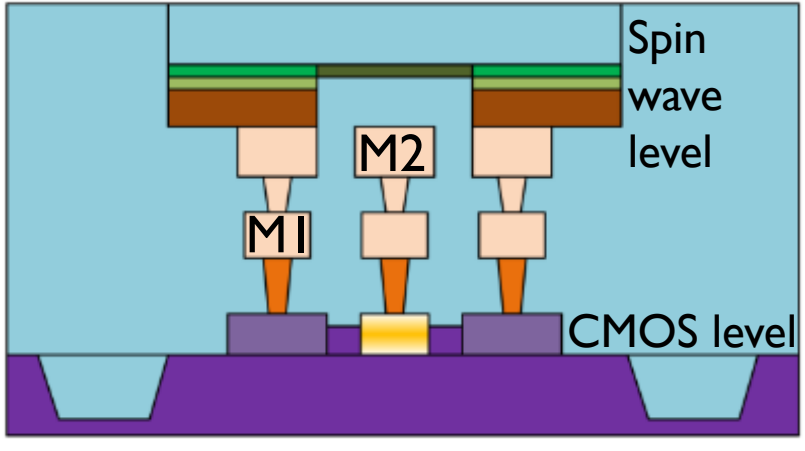


1-bit full adder

Wave computing circuit
5 transducers & 4 wave-guides



3D stacking on CMOS

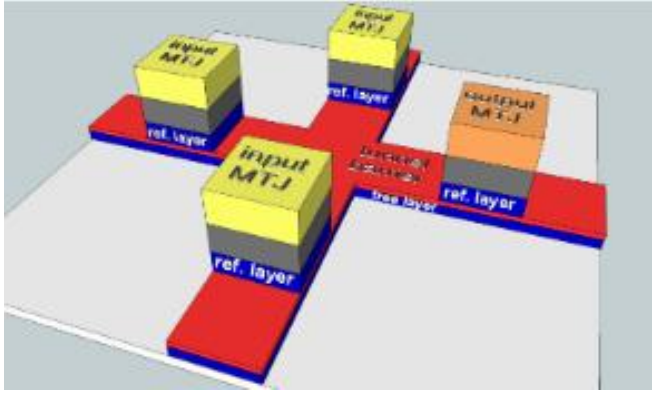


- Majority gates could lead to more compact designs as they simplify circuits while using larger CD.
- IMEC benchmarking:
  - 100× lower power
  - 4× area reduction

vs CMOS 10nm

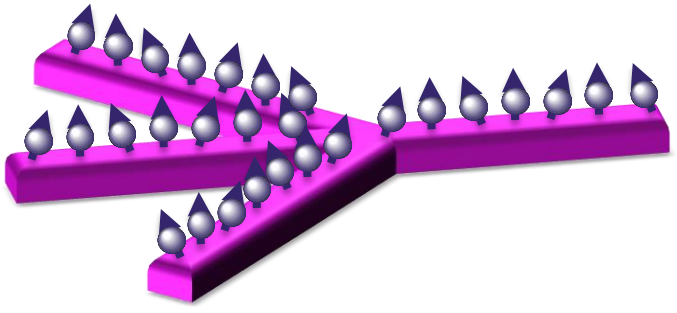
2 EXAMPLES OF MAJORITY GATES

Spin torque majority gate



- Based on domain wall motion driven by spin transfer torque
- Conversion to charge domain via STT and TMR or multiferroics—takes energy
- Scalable device and more efficient circuits with fewer devices

Spin wave majority gate



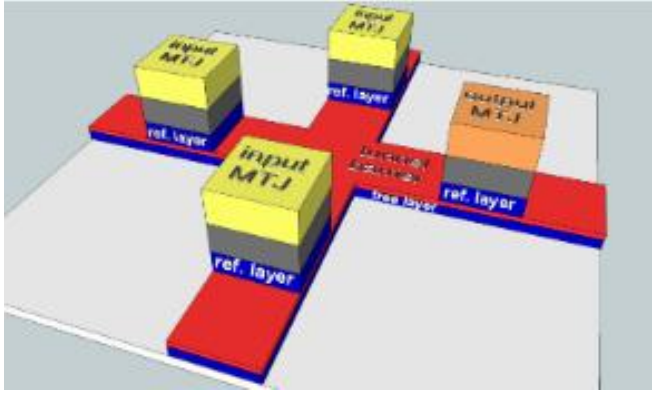
- Based on interference of spin waves
- Information encoded in amplitude or phase of spin wave
- Conversion to charge domain via magnetoelectric element—takes energy
- Ultra low power circuits

STMG VS. SPIN WAVE

	Spin torque majority gate	Spin wave majority gate
Physics principle	Domain wall motion/exchange	Spin wave interference
Write	Spin transfer torque	Magnetoelectric element
Read	magntoresistance	Magnetoelectric element
Non-volatile	Could be	Could be
Scaling	scalable	No clear how far
Cascading	No clear how	Proposals exists
Inverter	Proposal exists but v. difficult	ok
Materials	Comparable to MRAM	Piezoelectric+ magnetostrictive
Experimental demo	N/A	N/A

2 EXAMPLES OF MAJORITY GATES

Spin torque majority gate



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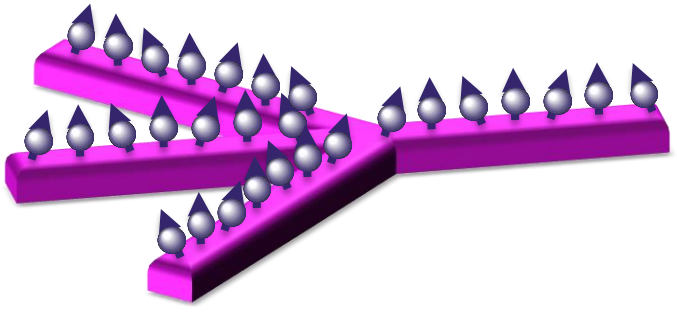
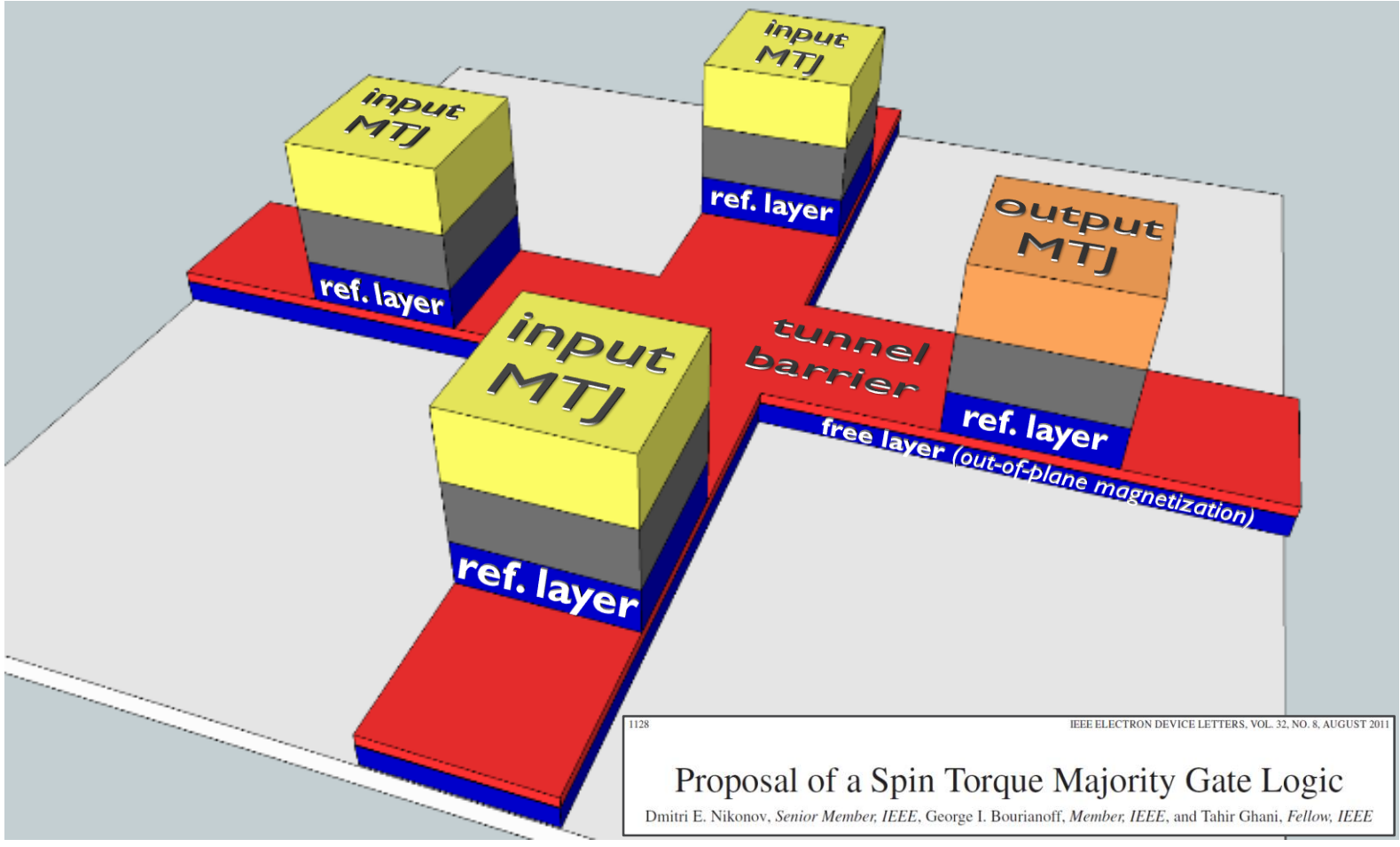


- Based on interference of spin waves
- Information encoded in amplitude or phase of spin wave
- Conversion to charge domain via magnetoelectric element—takes energy
- Ultra low power circuits

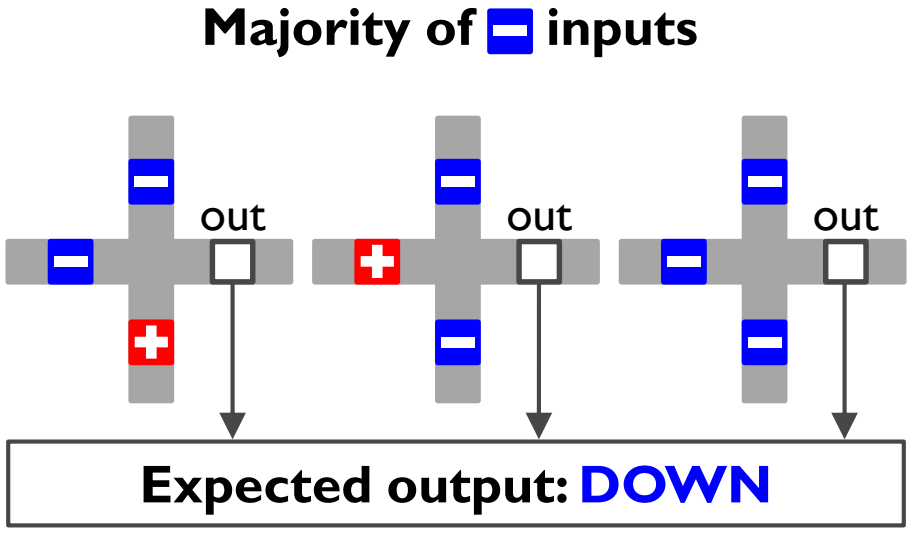
STMG: WORKING PRINCIPLE

Writing: STT

Read-out: TMR



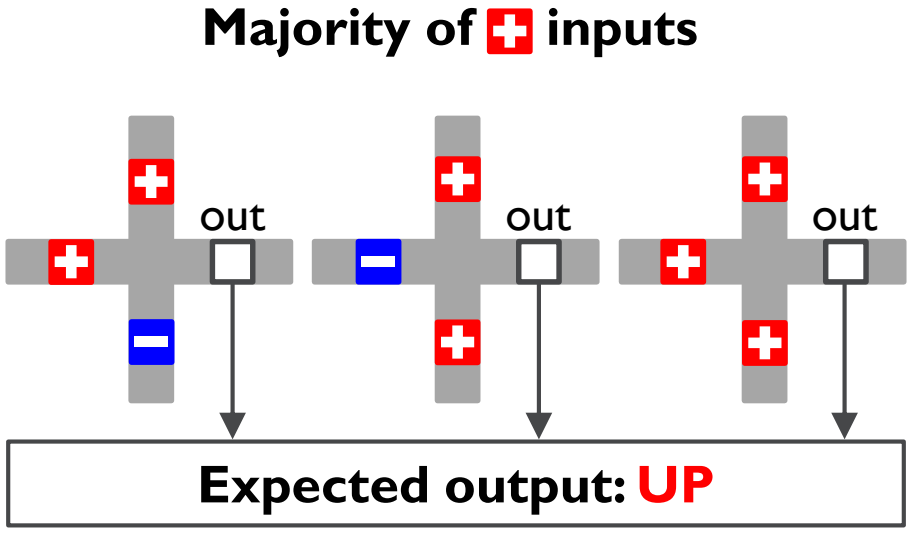
STMG: WORKING PRINCIPLE



'0'= + +V: magnetization pushed UP

'1'= − -V : magnetization pushed DOWN

STMG: WORKING PRINCIPLE



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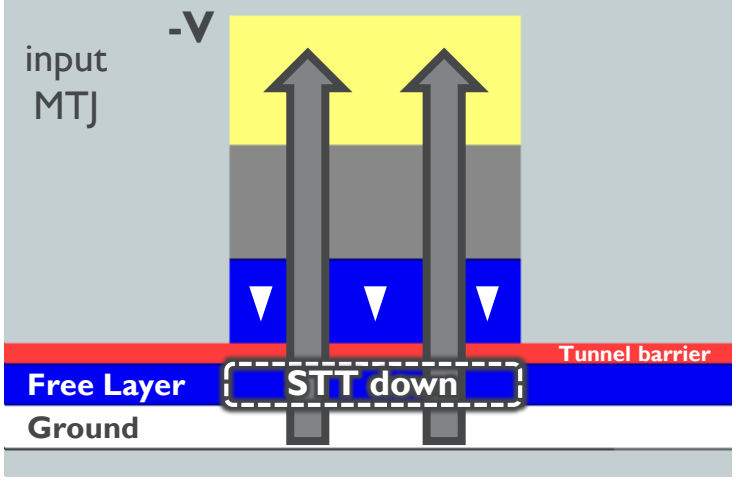
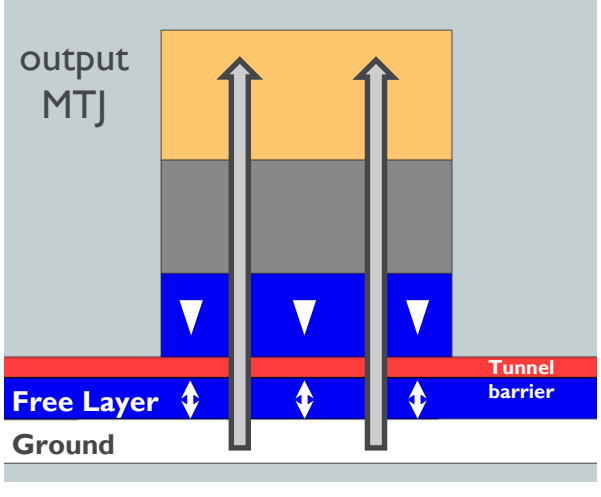


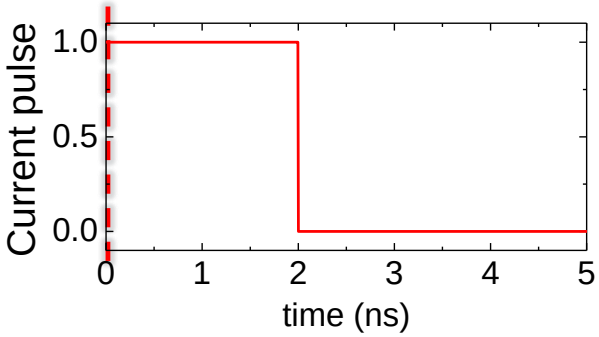
Input MTJs:
The current creates a "spin torque" acting on the local FL magnetization steering it upward or downward.

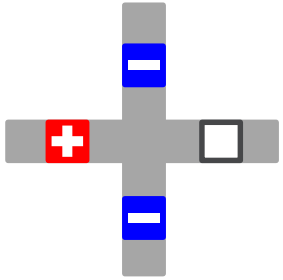


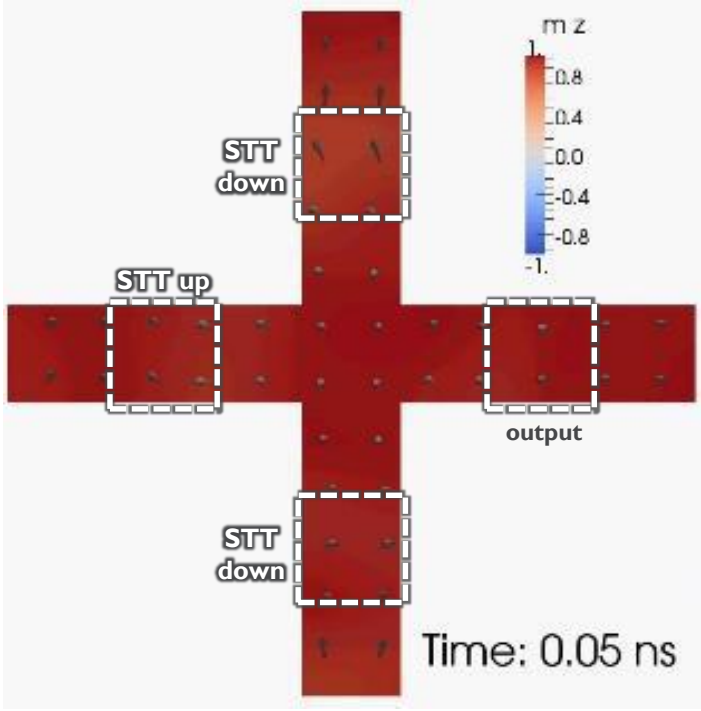
Output MTJ: read-out by TMR effect.

- FL magnetization DOWN = low resistance
- FL magnetization UP = high resistance

STMG: WORKING PRINCIPLE

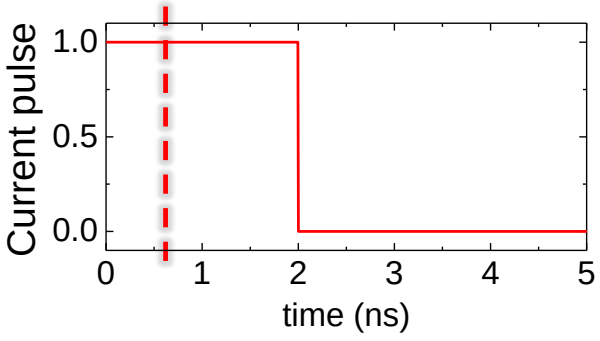


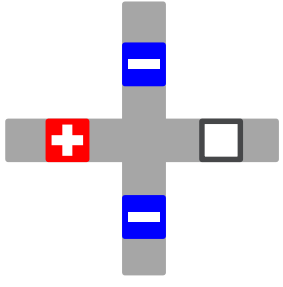


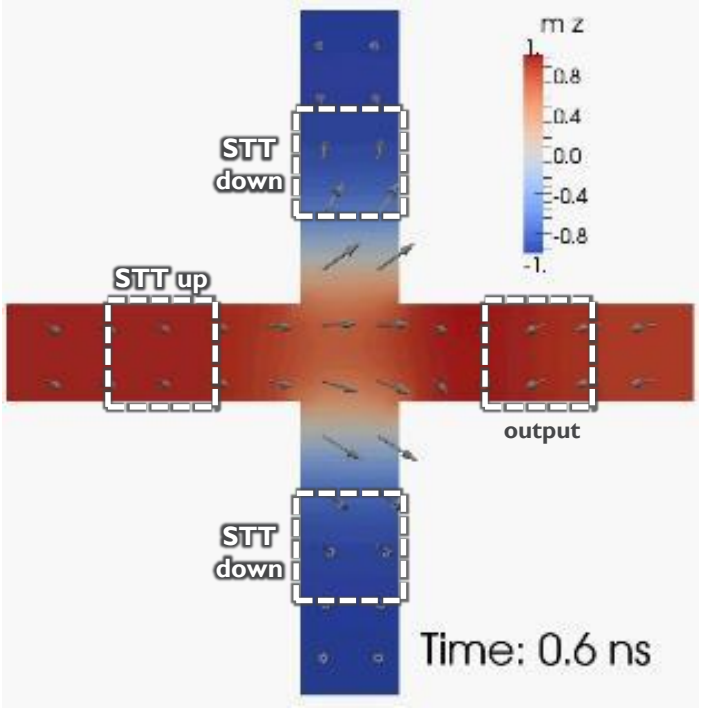


The initial state is UP.

STMG: WORKING PRINCIPLE

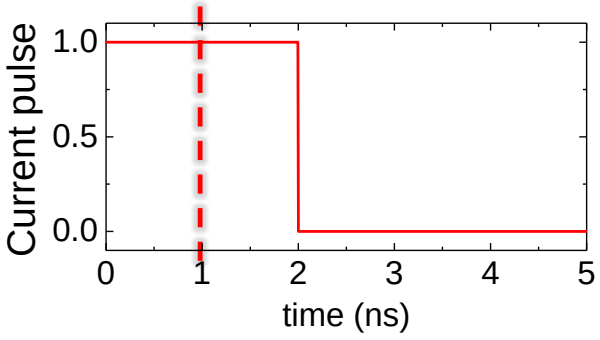


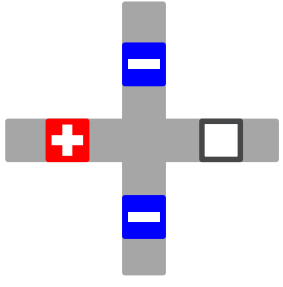


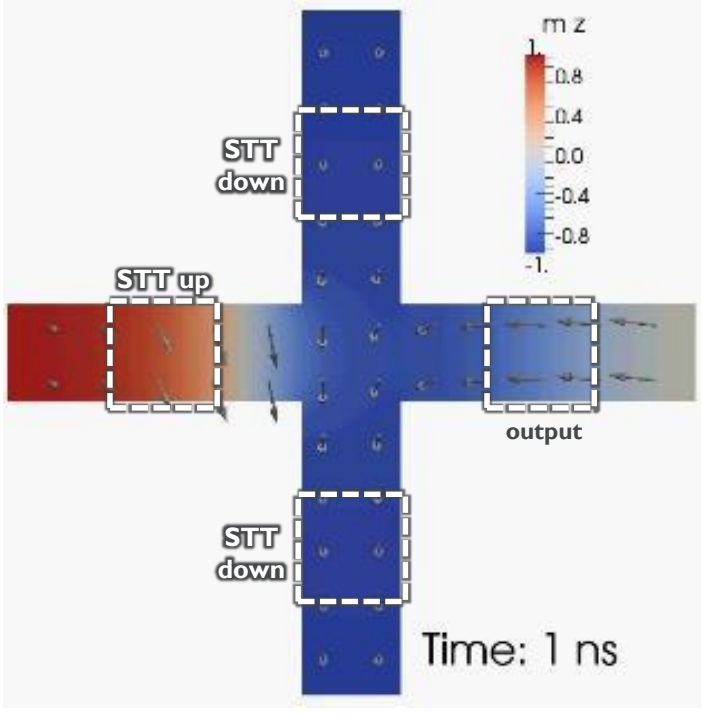


First, the magnetization is switched at the input MTJs that have negative voltage.

STMG: WORKING PRINCIPLE

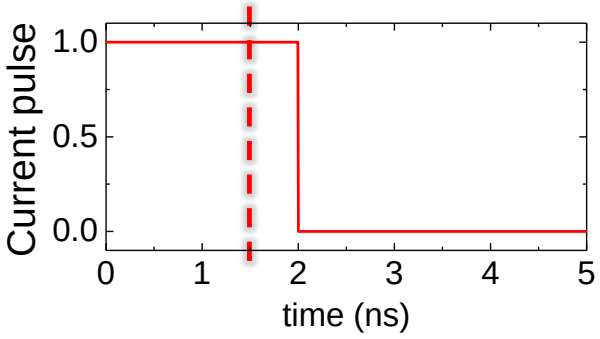


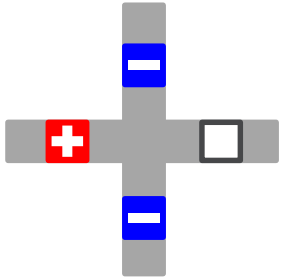


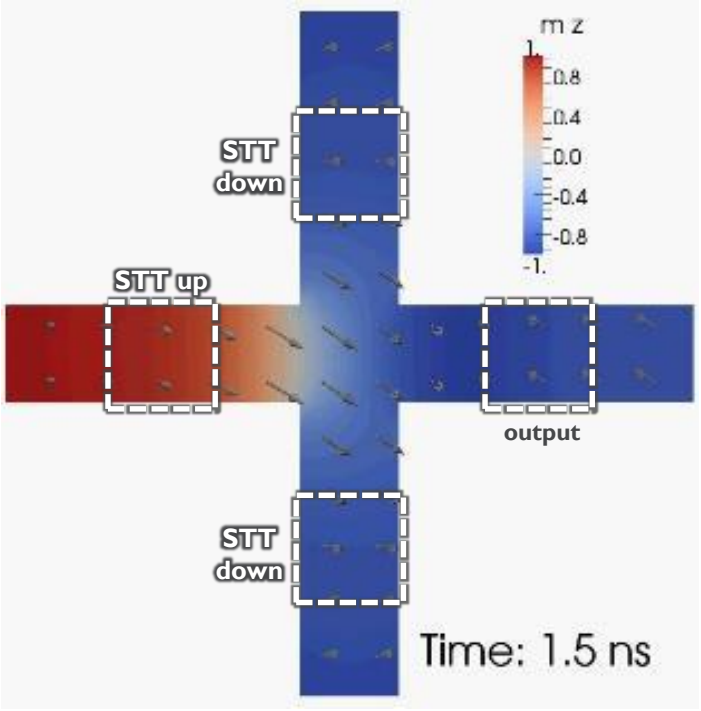


Then, domains propagate to the output arm via the exchange interaction.

STMG: WORKING PRINCIPLE







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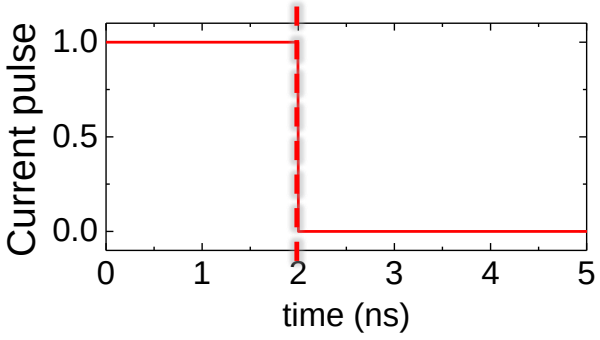

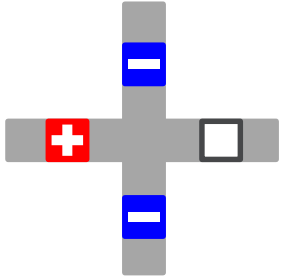

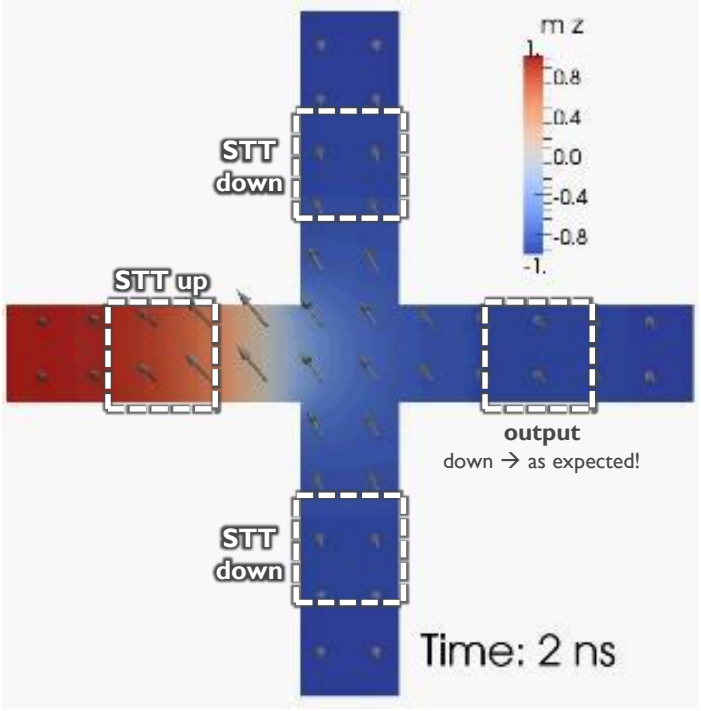

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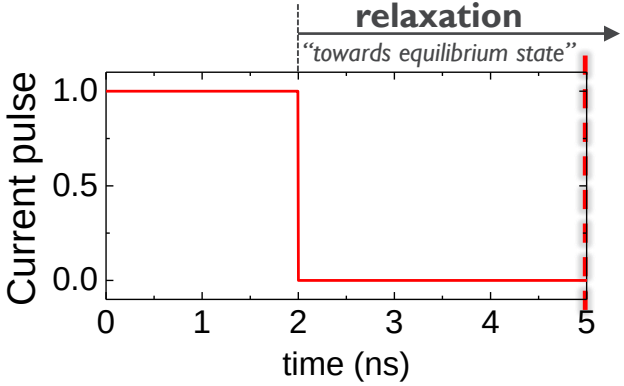
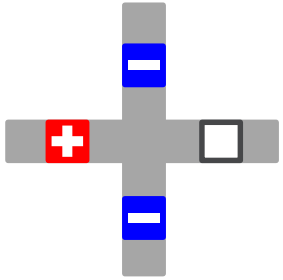
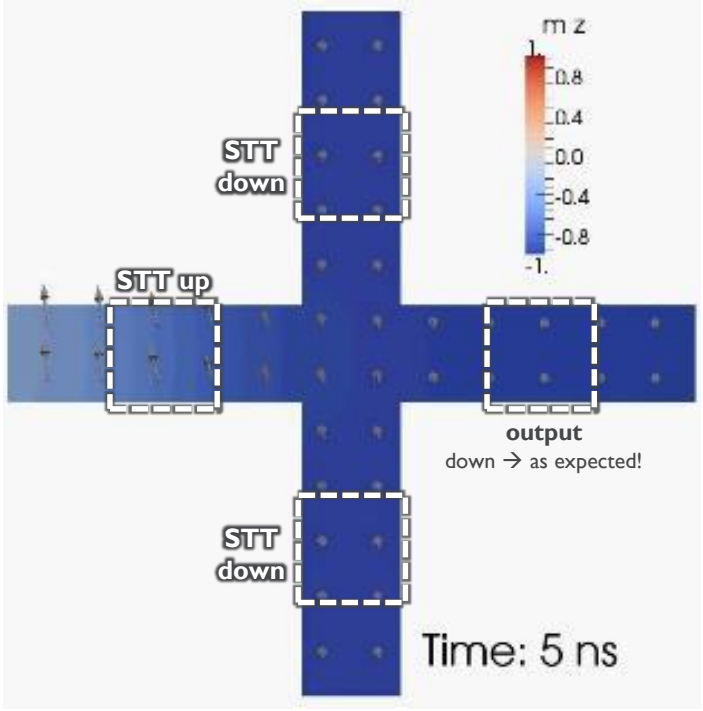
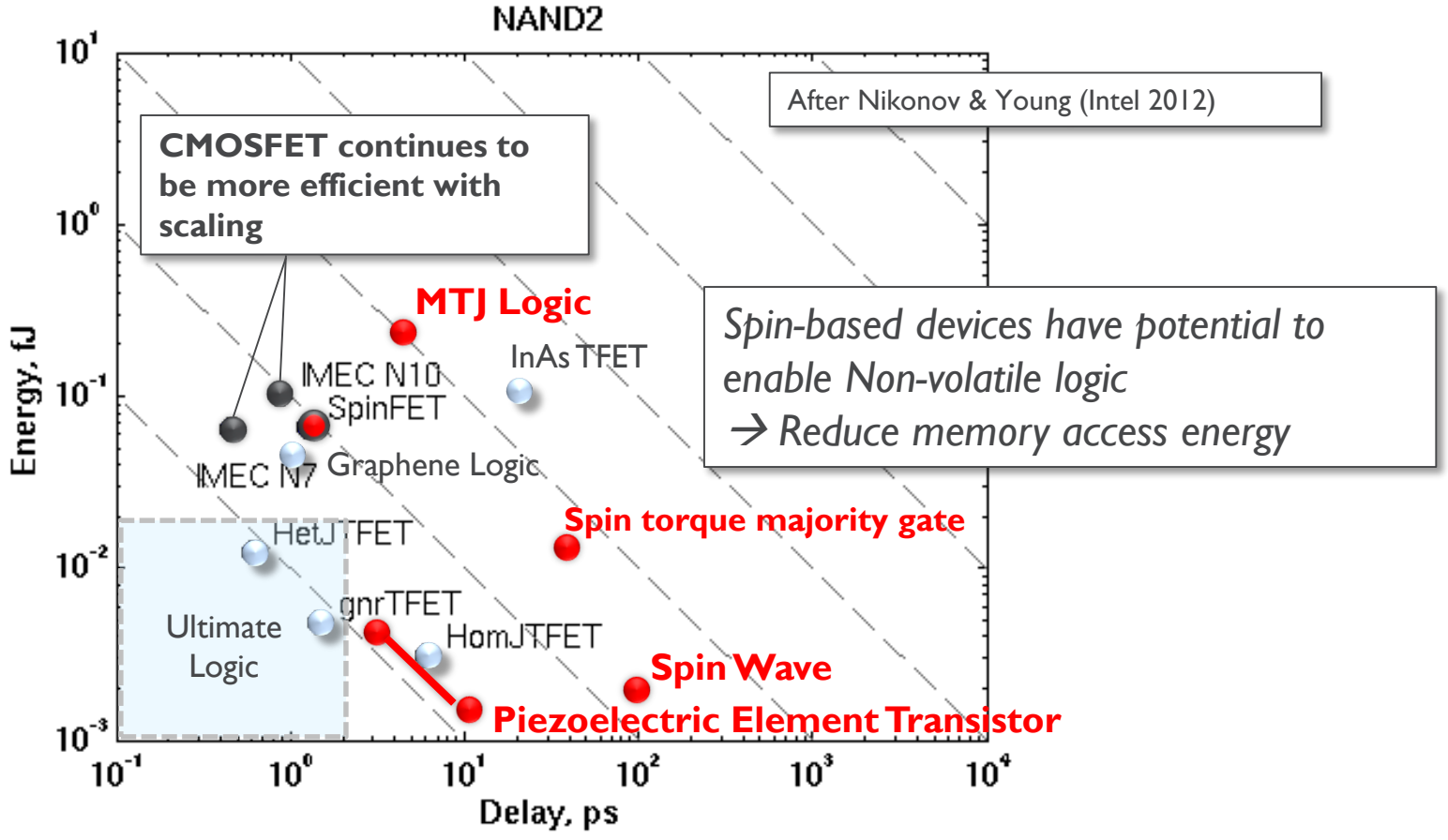






At the end, the output magnetic state is the majority of the three inputs (down because, the majority of inputs are down).

ENERGY EFFICIENCY BENCHMARK



- Black/Green: Charge-based devices
- **Red: Non-charge** based devices offer different Energy-Delay tradeoffs

MAGNETOELECTRIC EFFECT

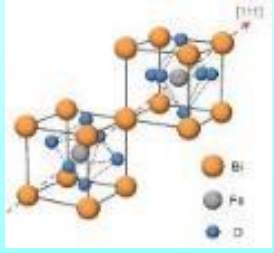
Conversion from charge to spin domain by **voltage control** is most energy efficient method.
Several physical effects that can come into play.

Multiferroic materials

Few materials multiferroic at room temperature

$BiFeO_3$

Weak effect



Synthetic multiferroics

Stacks of piezoelectric and magnetostrictive materials

Stronger effect, but complicated materials

Magnetostrictive

Piezoelectric

Interfaces

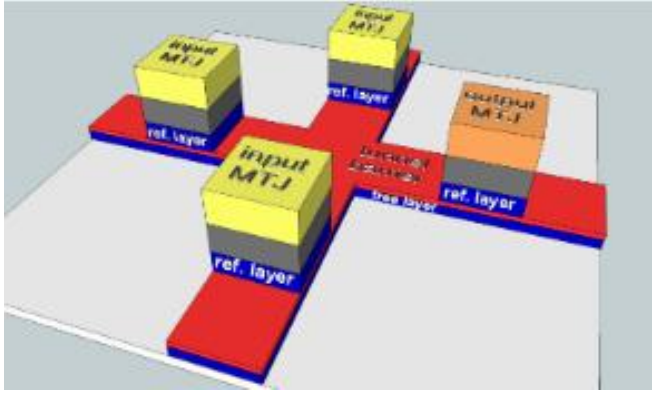
Tune magnetic anisotropy at magnetic metal/ oxide interface with an electric field (very thin metal).

Interesting effect

Temperature sensitive

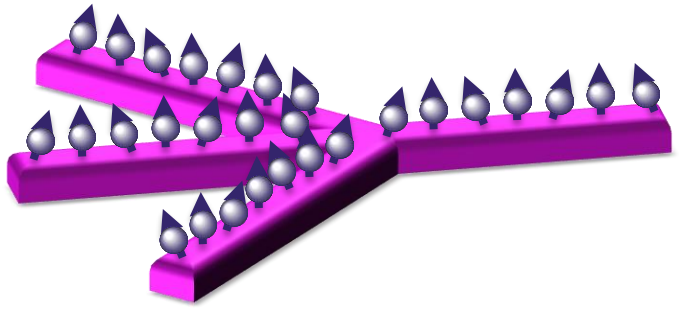
2 EXAMPLES OF MAJORITY GATES

Spin torque majority gate



- Based on domain wall motion driven by spin transfer torque
- Conversion to charge domain via STT and TMR or multiferroics—takes energy
- Scalable device and more efficient circuits with fewer devices

Spin wave majority gate



- Based on interference of spin waves
- Information encoded in amplitude or phase of spin wave
- Conversion to charge domain via magnetoelectric element—takes energy
- Ultra low power circuits

BASIC BUILDING BLOCKS OF WAVE COMPUTING

Wave emitter
(Transducer)

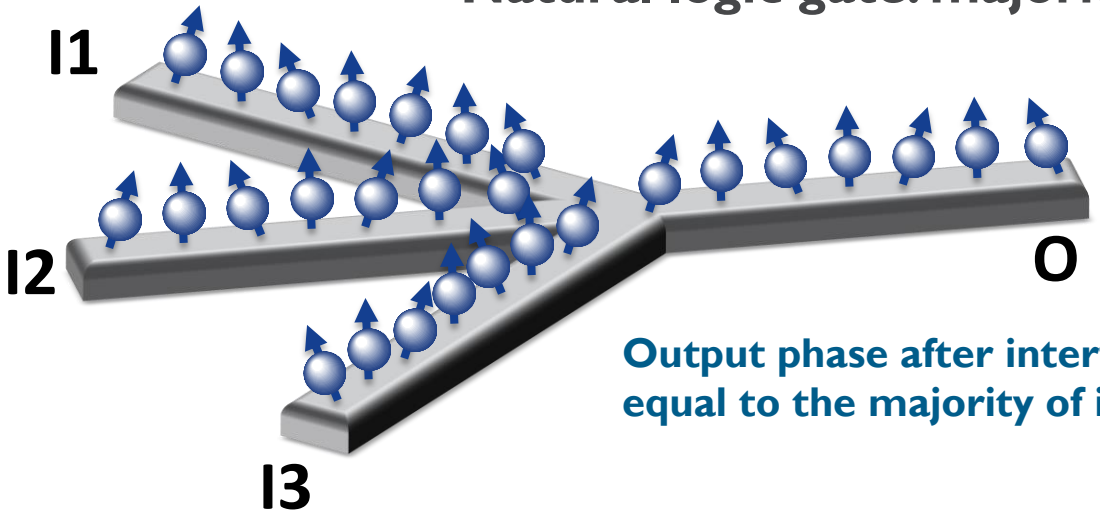
Waveguide for propagation
and interference

Wave detector
(Transducer)

When wave computing circuits are integrated alongside CMOS, the emitters and detectors have to be transducers between the wave and the electric domains

WAVE COMPUTING: LOGIC BY INTERFERENCE

Computation by interference
Natural logic gate: majority gate



I1	I2	I3	O
0	0	0	0
0	0	1	0
0	1	1	1
1	1	1	1

Output phase after interference is equal to the majority of input phases

0	0
1	π

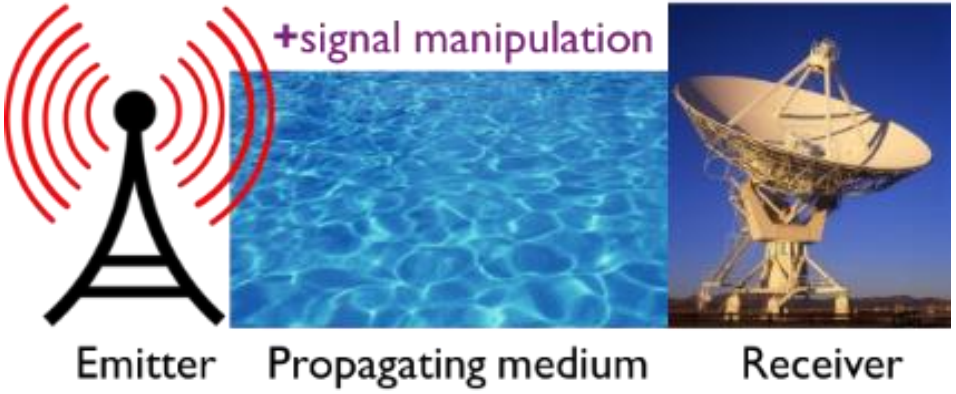
In wave computing, information is coded in the phase of the wave
However, also amplitude coding has been proposed and pursued

WHICH WAVE?

Wave computing can be realized using any wave in a solid support medium

Wave	Advantages	Disadvantages
Spin wave	• Simple wave guiding, good confinement • Scalable • **Compact transducer (ME cell)**	• Moderate group velocity • Damping
Plasmon	• High group velocity	• Damping for confined modes • Not yet scalable to short λ, large modes
Photon	• High group velocity • Mature technology	• Poor scalability • No compact excitation
Acoustic wave	• Compact transducer • NEMS technology comparably mature	• Low to moderate group velocity • High frequency for short wavelength • Compact waveguiding challenging

SPIN WAVE DEVICES



Spin waves devices consist of:

- Emitter
- Receiver
- Propagating medium (ferromagnet)
- Means to manipulate the phase or amplitude of the signal

Emission/detection and modulation of spin waves can be done by many means, but **voltage control** is most energy efficient method

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Few materials multiferroic at room temperature

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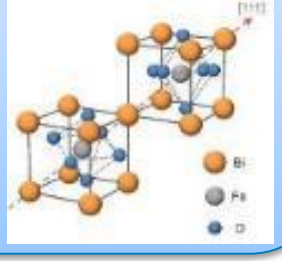
Weak effect



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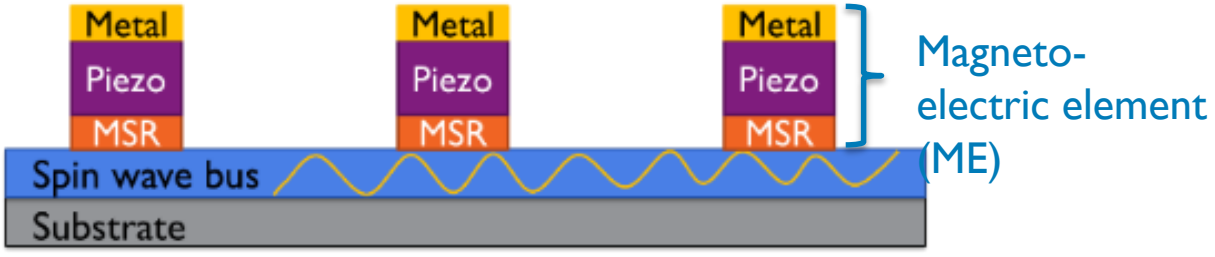
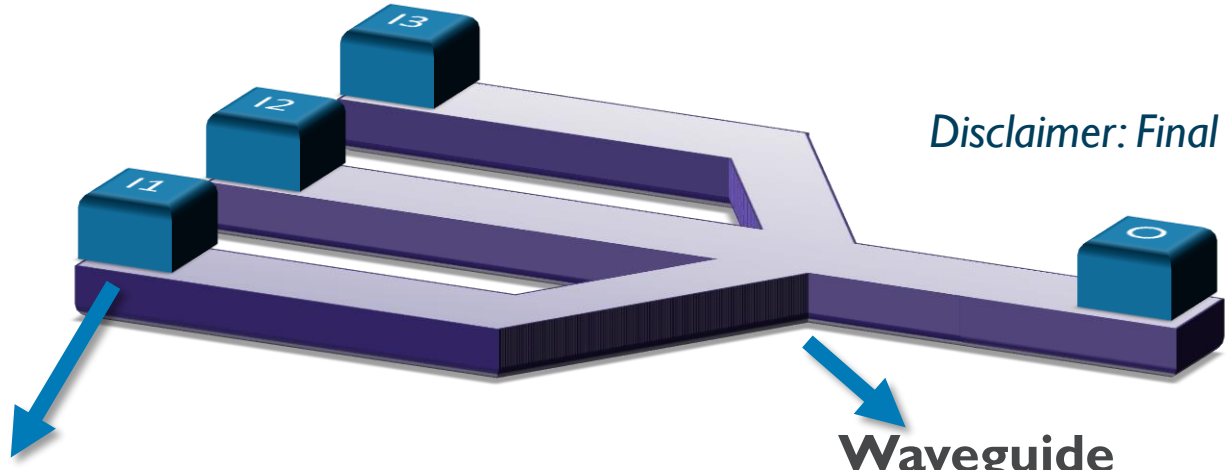
SPIN WAVE DEVICES



- Electric field induces strain in the piezoelectric
- Strain induces rotation of magnetic anisotropy in magnetostrictive material (MSR)
- Change in magnetic anisotropy generates or modulates spin wave in nearby ferromagnet (spin wave bus)
- One ME for injection of spin wave, one ME for manipulation of phase, one ME for read-out.
- Work on **material components for MEs**
- Investigate **device properties (phase/ amplitude control) with MEs**.
- **Evaluate efficiency** of spin wave injection/ detection via MEs.

SPIN WAVE MAJORITY GATE



Disclaimer: Final layout may/will vary...

A. Khitun, et al., J. Appl. Phys., ***110*** *(2011)*

EXCITATION OF SPIN WAVES VIA STT

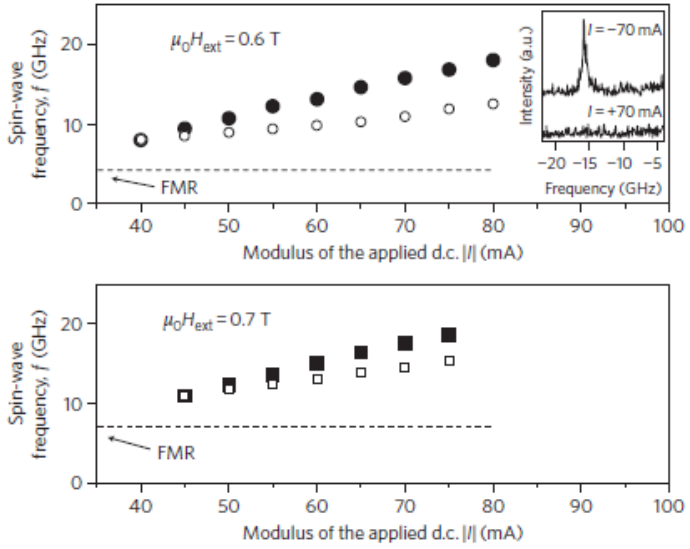


Figure 3 | Spin-wave frequencies as a function of the injected d.c. intensity. Measured (filled symbols) and simulated (open symbols) spin-wave frequency dependence on d.c. intensity for two different values of the magnetic field. Dashed lines represent the calculated FMR frequency. Inset: μ-BLS spectra (Stokes side) recorded at $\mu_0 H_{ext} = 0.6$ T and for different signs of the current $|I| = 70$ mA.

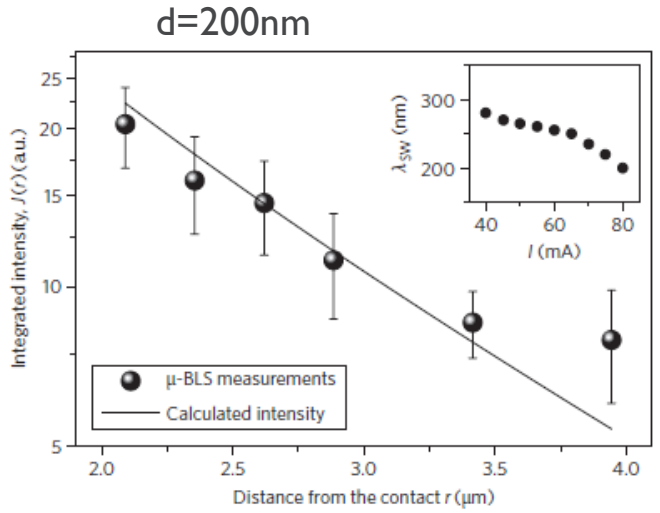


Figure 5 | Spin-wave attenuation as a function of distance from the STO. Integrated intensity (symbols) of the spin-wave excitations detected using μ-BLS as a function of distance from the centre of the point contact (r). Analytical calculation (line) of the decay obtained using the function described in the text. Inset: simulated spin-wave wavelength as a function of applied d.c. intensity.

Madami et al. Nature Nanotech. 2011

TUNING OF PHASE VIA ME EFFECT

Bao APL 101 022409 (2012)

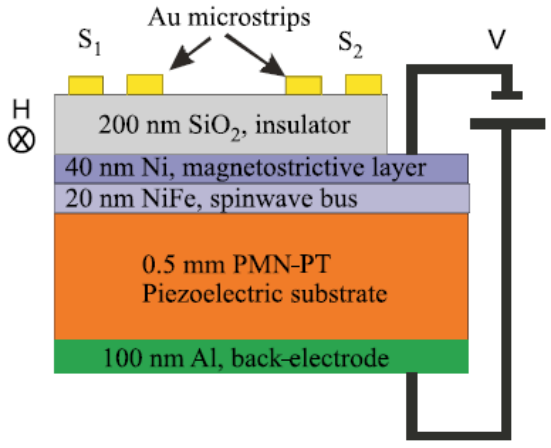
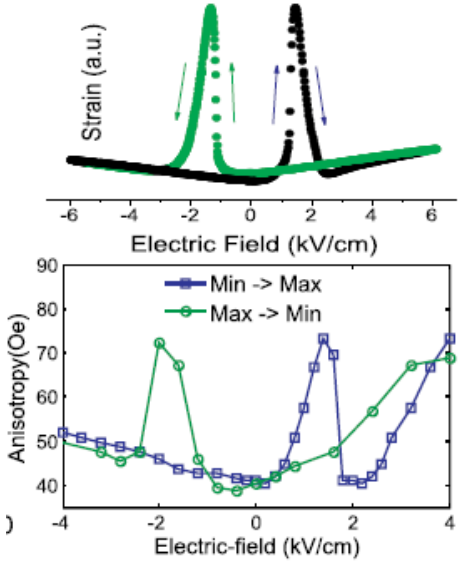


FIG. 1. Cross section of device layer structure and experimental configuration of spinwave excitation (S_1)/detection (S_2) antennas, bias magnetic field, and bias electric field.



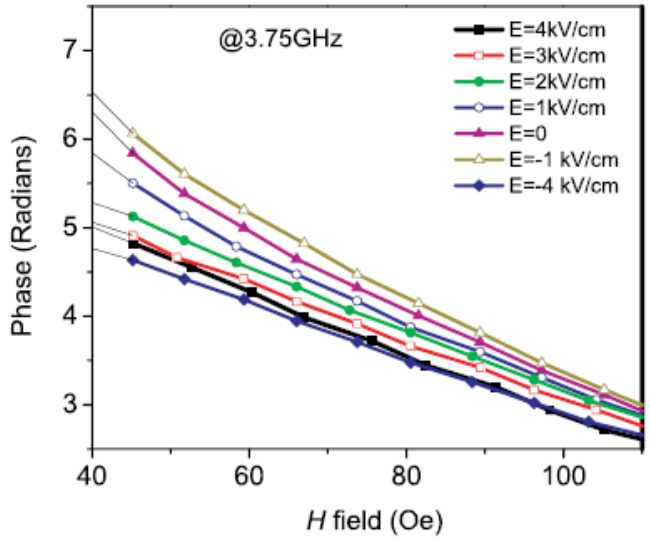


FIG. 4. Measured phase shift of the spinwaves at different electric fields for one fixed frequency.

- First demonstrations of phase control using magnetoelectric effect
- But ME element not patterned

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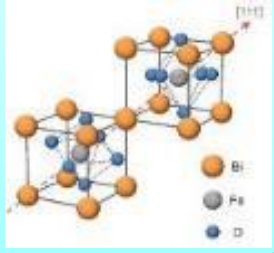

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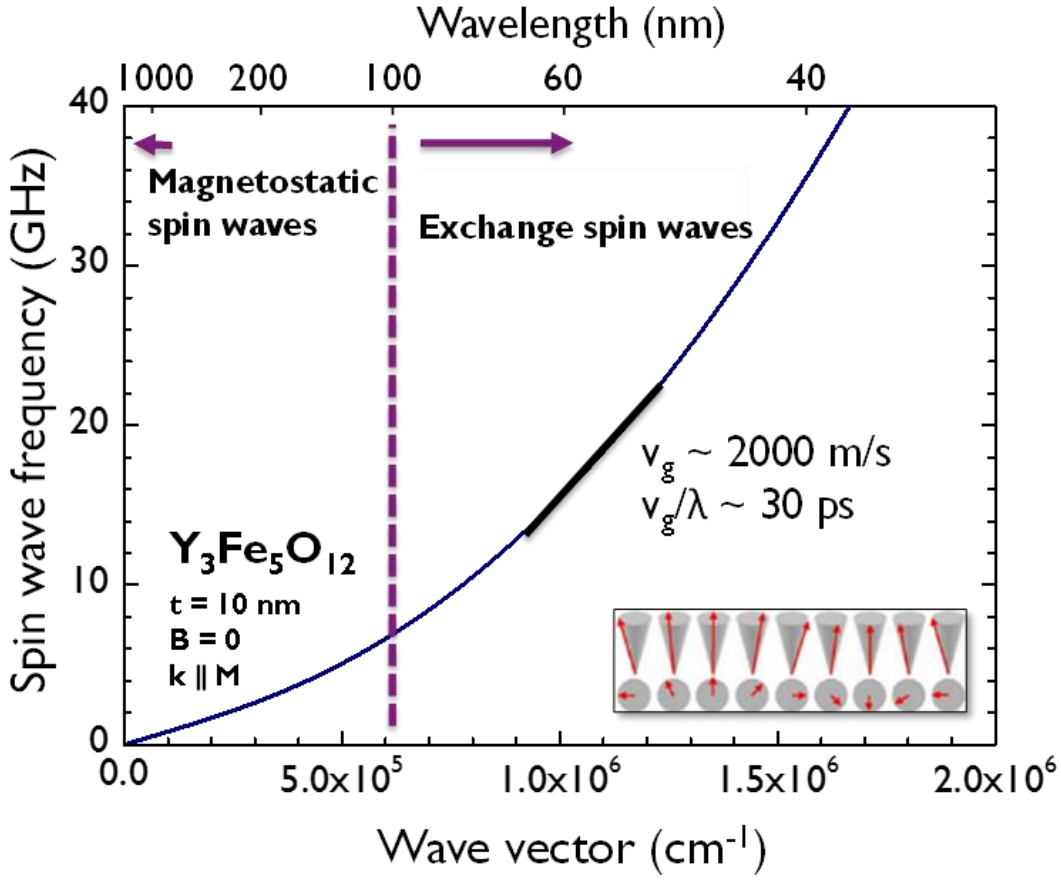
CRITERIA FOR HIGH PERFORMANCE WAVE COMPUTING

- Critical dimension (wavelength, transducer size)
  < 100 nm (area)
- Logic gate delay **< 500 ps** (throughput)
  limited by group velocity, dispersion, transducer bandwidth
- Transducer output signal >3 kT/e (**~100 mV**) (power, area)
  <1V input; lower output signal requires complex (and costly) periphery

Exchange spin waves and magnetoelectric transducers promise to satisfy all three criteria

EXCHANGE SPIN WAVE IN YIG WAVEGUIDES

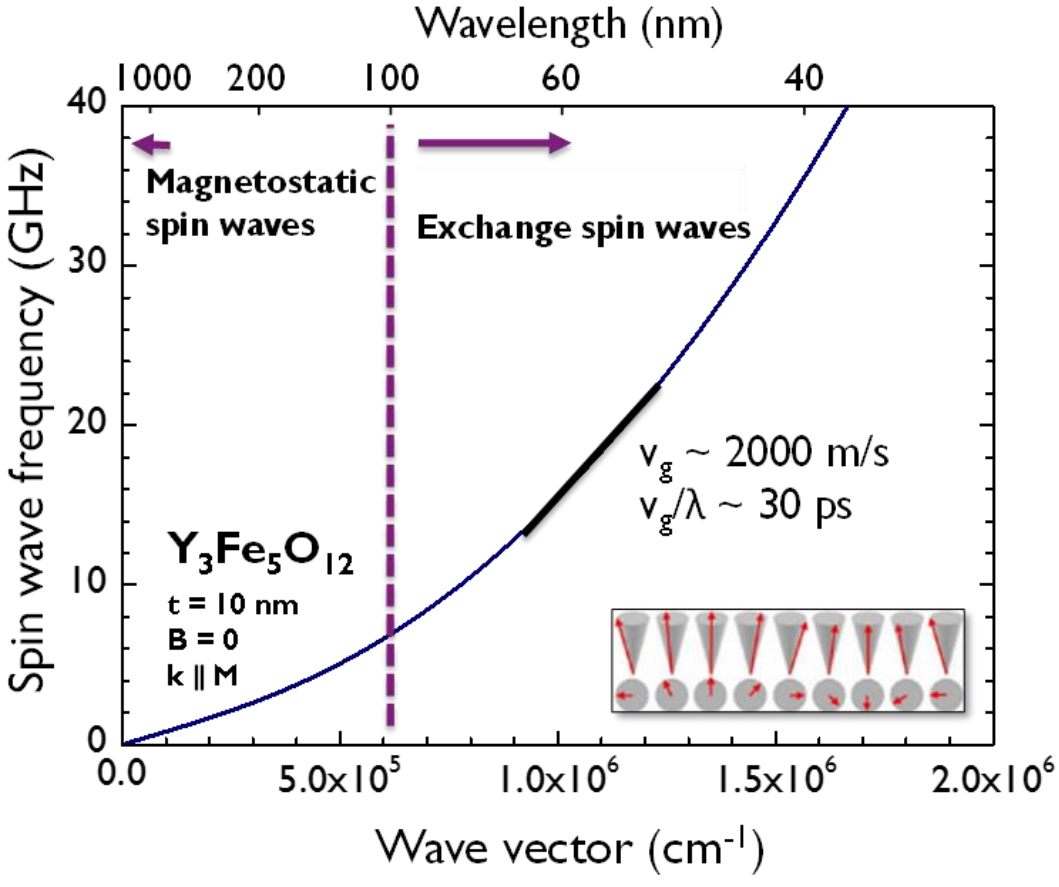
Faster propagation possible for short λ exchange modes without applied external field



EXCHANGE SPIN WAVE IN YIG WAVEGUIDES

Limitations by damping

- Propagation over a few wavelengths are sufficient for a single gate
- Damping target: $\alpha \sim 10^{-2}$
- Magnetostatic spin waves in YIG $\alpha \sim 10^{-5}$, polycrystalline transition metals $\alpha \sim 10^{-3}$ to 10^{-2}
- Little data however available in exchange range

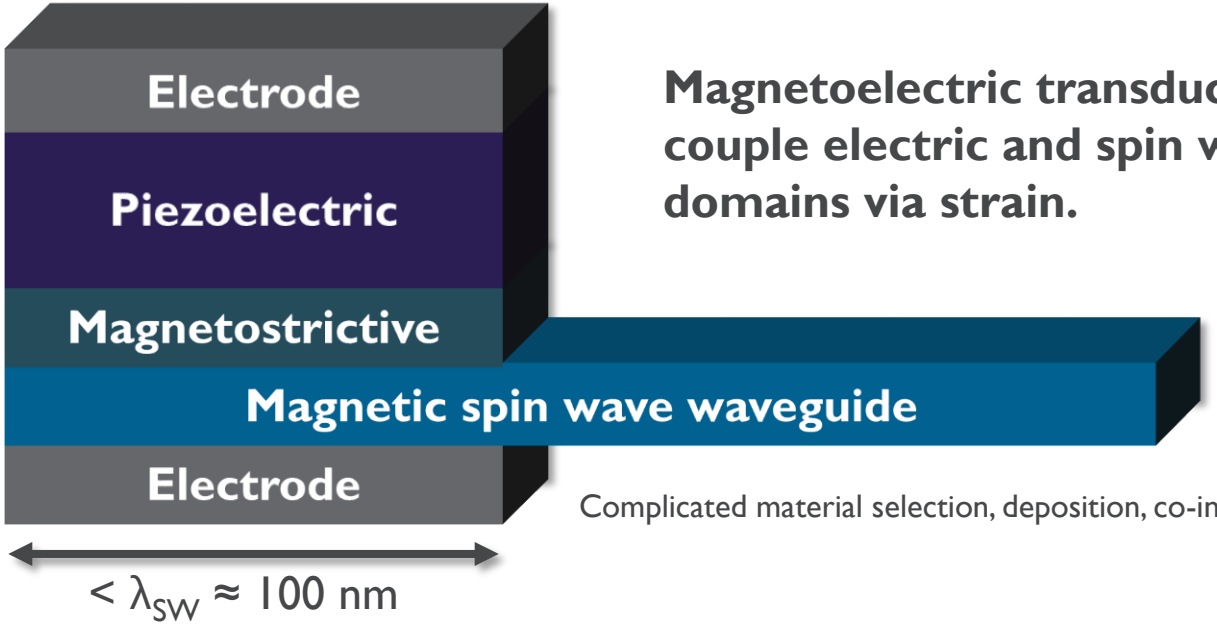


MAGNETOELECTRIC SPIN WAVE TRANSDUCERS

Synthetic multiferroic

Film properties can be individually optimized.

PMN-PT/Terfenol-D
> 4000 mV/cm Oe
cf. $BiFeO_3$
7 mV/cm Oe



Magnetoelectric transducers couple electric and spin wave domains via strain.

Complicated material selection, deposition, co-integration, and processing problems.

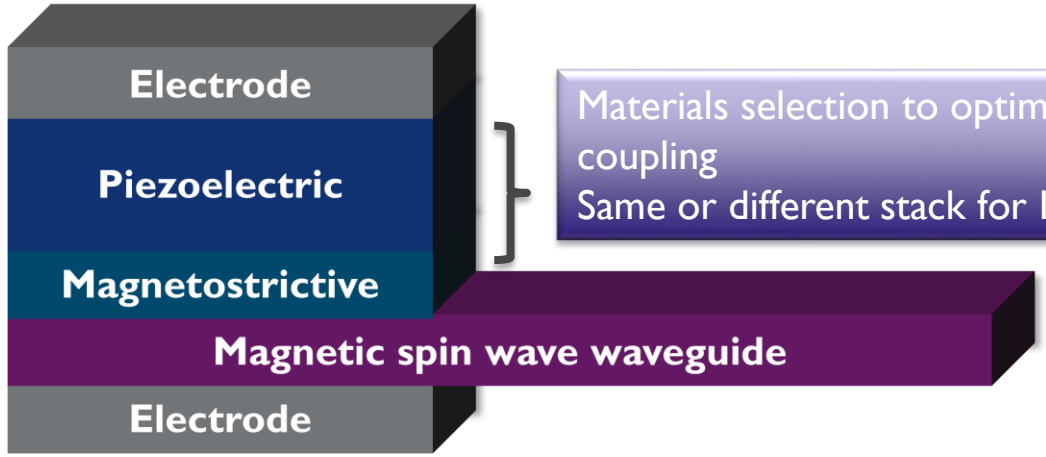
Magnetoelectric transducers show great promise for efficient coupling between electric and spin wave domains and large output signal. Devices are scalable to small dimensions and short wavelengths.

CHALLENGES OF MAGNETOELECTRIC TRANSDUCERS

Piezoelectric materials behavior at GHz frequencies and small thicknesses

Integration of heterogeneous materials; interface formation

Coupling between MS layer and waveguide. MS waveguide?



Materials selection to optimize coupling
Same or different stack for I/O?

Magnetoelectric transducers require considerable materials development

Principle demonstrated but need to be brought to relevant dimensions/frequency

SPIN WAVE DEVICES: MATERIALS ASPECTS

Piezoelectric-magnetostrictive compound

Piezoelectric material:

- High piezoelectric coefficient @
  - High frequency (GHz)
  - Thin films (sub-100 nm)
  - Small lateral size (sub-100 nm)

Magnetostrictive material:

- High magtnetostrictive coefficient
- Low damping
- Coupling with waveguide?

Co-integration and magnetoelectric coupling

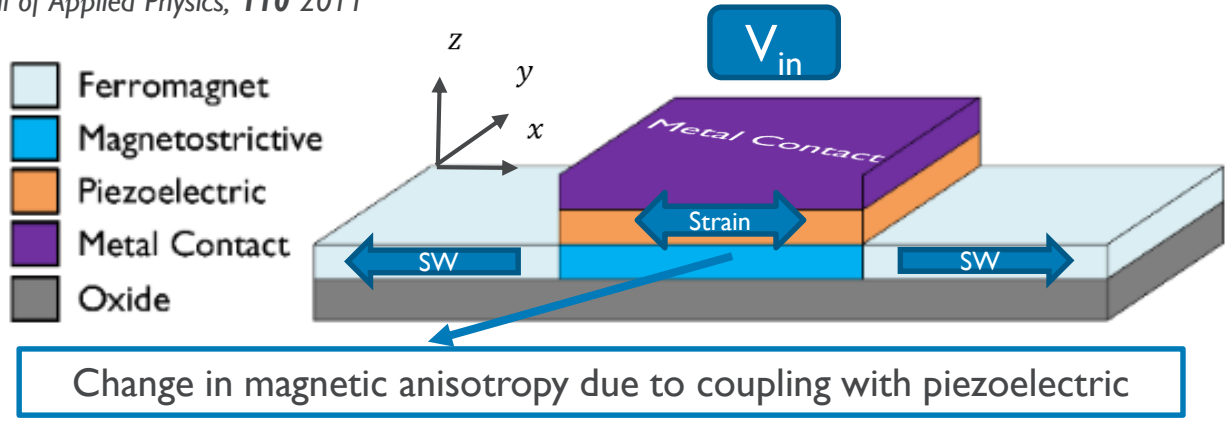
ME CELL AS BASIC COMPONENT FOR SW DEVICES

MAGNETO-ELECTRIC (ME) CELL [1] IS THE BASIC COMPONENT FOR SW GENERATION AND DETECTION

*[1]: A. Khitun, et al., Journal of Applied Physics, **110** 2011*

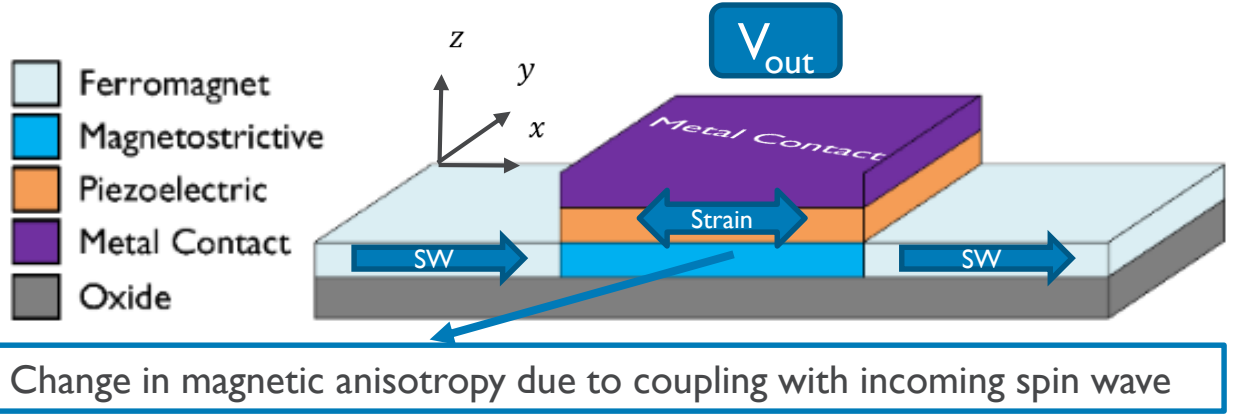
Generation :

Input voltage applied at the ME element causes the piezoelectric to strain which in turn induces a change in magnetic anisotropy resulting in the generation of a spin wave



Detection :

Incoming spin wave induces a change in magnetic anisotropy causing a stress in the piezoelectric which in turn induces an output voltage



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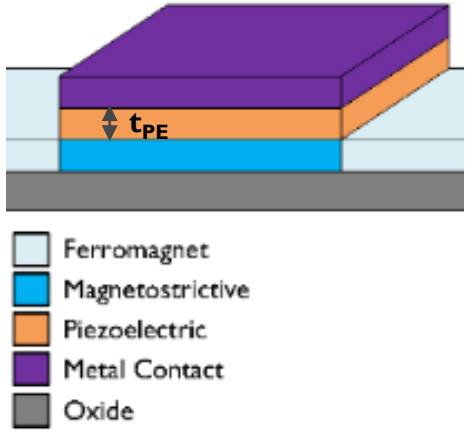
ME SWITCHING

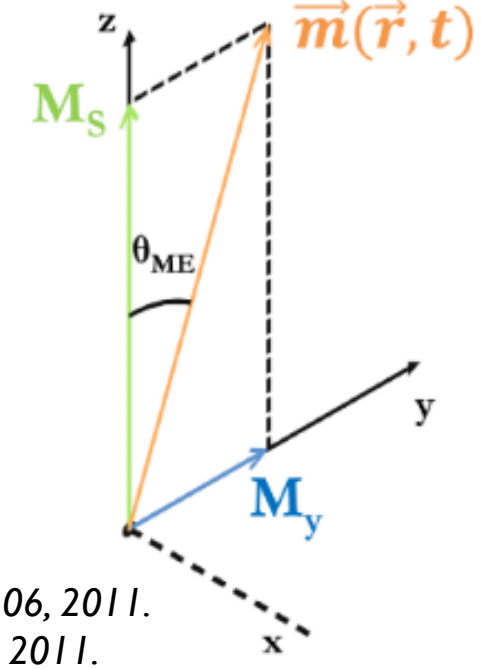
Output Voltage Modeling



Need to increase predicted output voltage of ±10mV [1]

$$V_{out} = \left|\vec{E}\right| \cdot t_{PE}$$
$$V_{out} = c_{ME} \cdot \left|\vec{H}_{eff}\right| \cdot t_{PE}$$
$$V_{out} = c_{ME} \cdot 2 \cdot M_Y \cdot t_{PE}$$

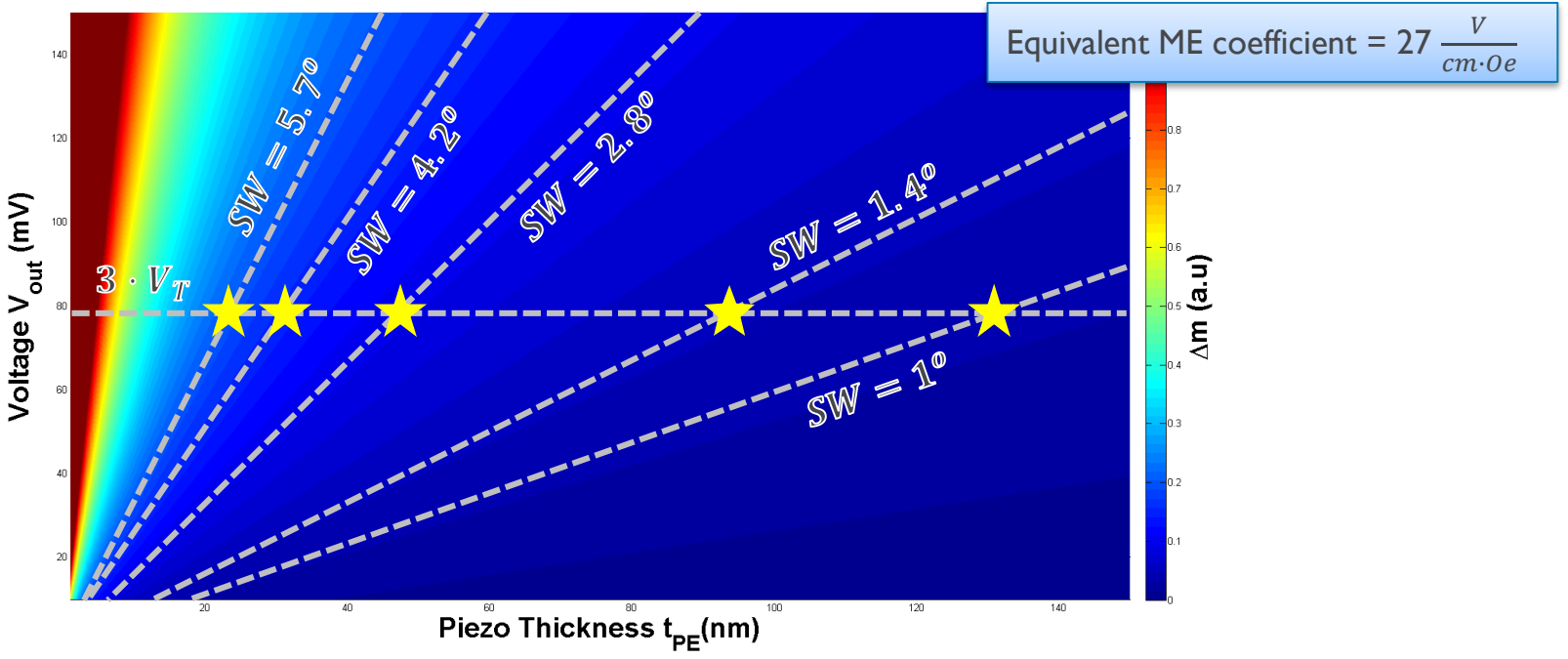
$$\boxed{V_{out} = c_{ME} \cdot M_S \cdot \tan(2 \cdot \theta_{ME}) \cdot t_{PE}}$$



We assume magneto-electric coeff. c_{ME}=27V/cm·Oe [2]

[1]:A. Khitun, et al., Journal of Applied Physics, 110:034306, 2011.
[2]:T.Wu, et al., Journal of Applied Physics, 109:07D732, 2011.

ME CELL DESIGN SPACE



- To make a reasonable sense-amp → V_{out}>3$V_{thermal}$
- Device delay is proportional to piezo thickness → want min piezo thickness → increase SW angle → non-liner effects
- Literature focused on SW in linear regime

CIRCUIT BENCHMARKING

AREA 4X SMALLER!

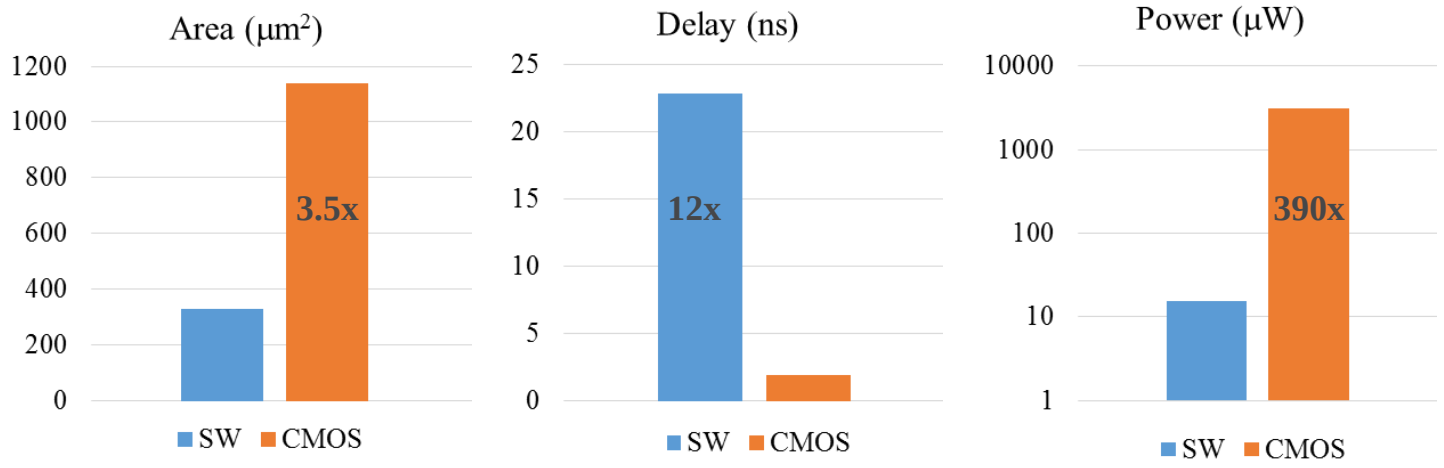
DELAY 10X SLOWER...

POWER 200X SMALLER!

ADPP 100X BETTER!

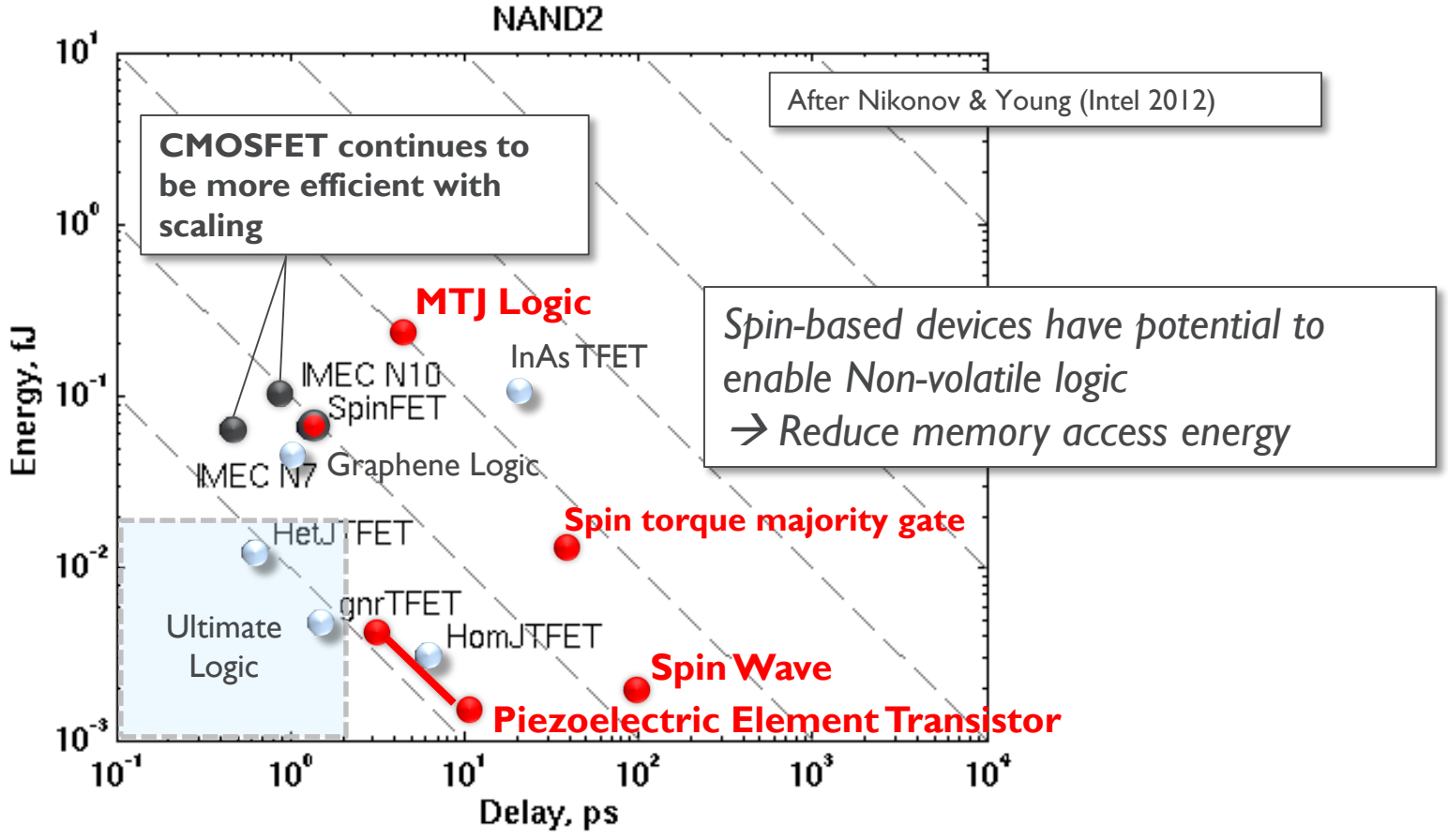
	Area (µm2)				Energy (fJ)	Delay (ns)		Power (µW)		ADPP		
Name	SWD core	CMOS SA	SWD Total	N10 Ref.	SWD Total	SWD	N10 Ref.	SWD	N10 Ref.	SWD	N10 Ref.	Impr. (x)
BKA264	36.48	3.12	39.60	118.55	175.50	5.07	0.21	34.62	133.92	6.95E+3	3.33E+3	0.48
HCA464	82.71	3.17	85.88	262.63	178.20	8.01	0.29	22.25	594.28	1.53E+4	4.53E+4	2.96
CSA464	78.42	3.17	81.59	240.26	178.20	7.59	1.78	23.48	663.17	1.45E+4	2.84E+5	19.51
DTM32	326.31	3.07	329.38	1183.64	172.80	14.73	0.52	11.73	3667.50	5.69E+4	2.26E+6	39.66
WTM32	264.96	3.07	268.04	1163.37	172.80	20.61	0.58	8.38	3571.90	4.63E+4	2.41E+6	52.04
DTM64	1192.69	6.14	1198.83	3459.32	345.60	18.09	0.63	19.10	12793.10	4.14E+5	2.79E+7	67.29
GFMUL	44.09	0.82	44.91	162.98	45.90	7.17	0.16	6.40	433.92	2.06E+3	1.13E+4	5.49
MAC32	295.25	3.12	298.37	1372.83	175.50	24.39	0.66	7.20	3872.10	5.24E+4	3.51E+6	67.00
DIV32	899.04	6.14	905.18	3347.73	345.60	117.21	14.00	2.95	5346.10	3.13E+5	2.51E+8	800.94
CRC32	27.61	1.54	29.14	95.88	86.40	5.07	0.22	17.04	304.30	2.52E+3	6.42E+3	2.55
Averages	324.76	3.34	328.09	1140.72	187.65	22.79	1.91	15.31	3138.03	9.24E+4	2.87E+7	105.79

CIRCUIT BENCHMARKING



- Area of SW circuit is on average 3.5x smaller than CMOS but delay is about 12X longer
- Power for SW circuit is on average ~400x lower than CMOS

ENERGY EFFICIENCY BENCHMARK



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- **Red: Non-charge** based devices offer different Energy-Delay tradeoffs

ASPIRE
INVENT
ACHIEVE