Materials, Devices, and Circuit Architectures for Future Electronics

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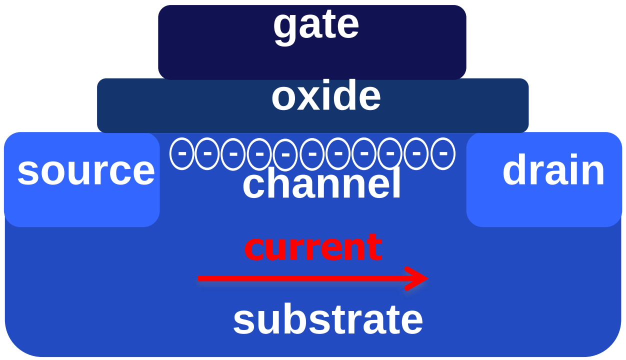
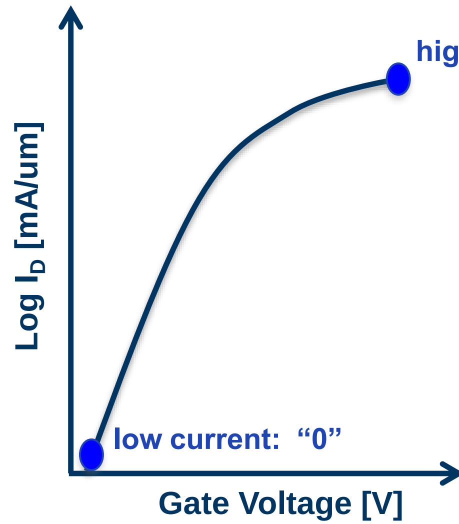
MOSFET:

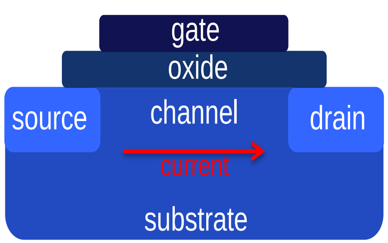
(Metal Oxide Semiconductor Field Effect Transistor

gate voltage modulates current in channel

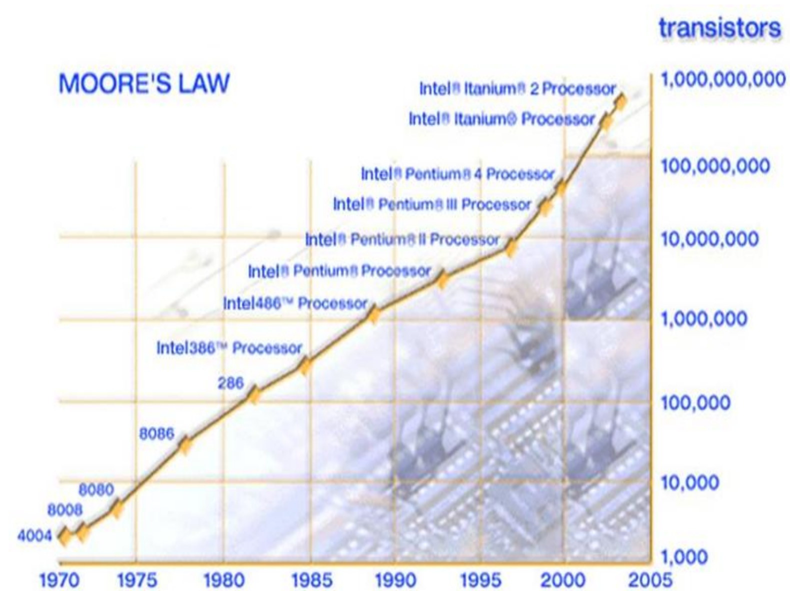




Dennard Scaling:
shrink device
lower voltage
constant E-field

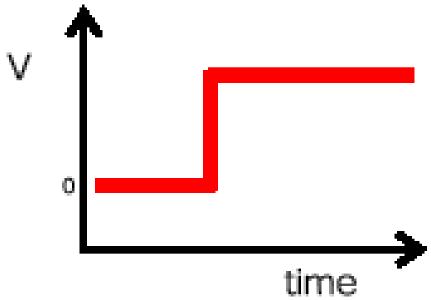


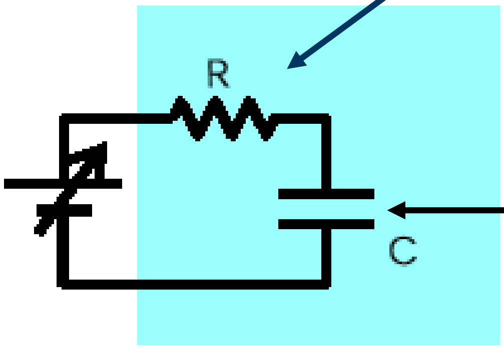
Result:
- Increased Density
- Lower Power
- Faster Switching



Simple Model for Switching of an FET:

Abrupt Charging of a Capacitance





Channel resistance of the charging (switching) device

Gate capacitance of the charged (switched) device

$$E_{diss} = \int_0^\infty i^2 R(t)\, dt = \tfrac{1}{2} CV^2$$

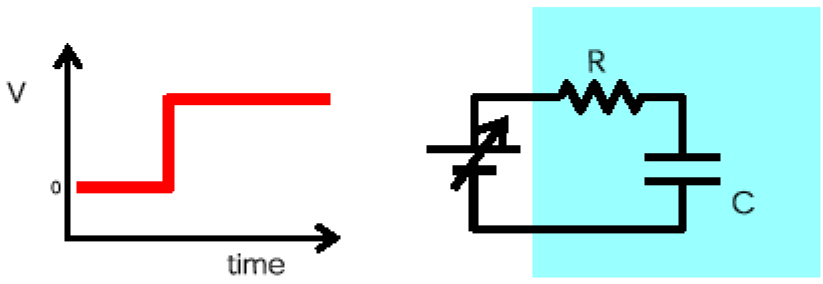
(independent of R!)

$$E_{stor} = \tfrac{1}{2} QV = \tfrac{1}{2} CV^2$$

Adiabatic Switching

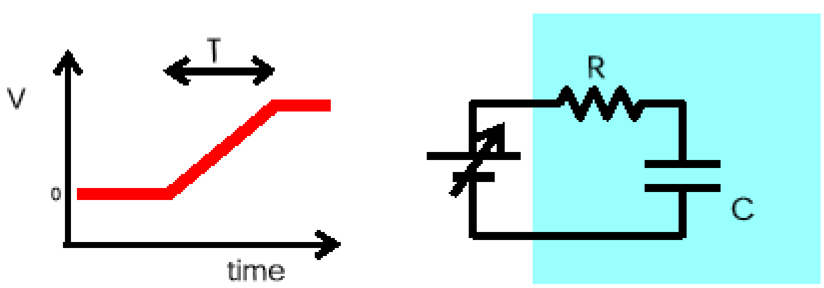
The stored energy need not be dissipated

Abrupt method



$$E = \frac{1}{2} C V^2$$

Quasi-static Charging



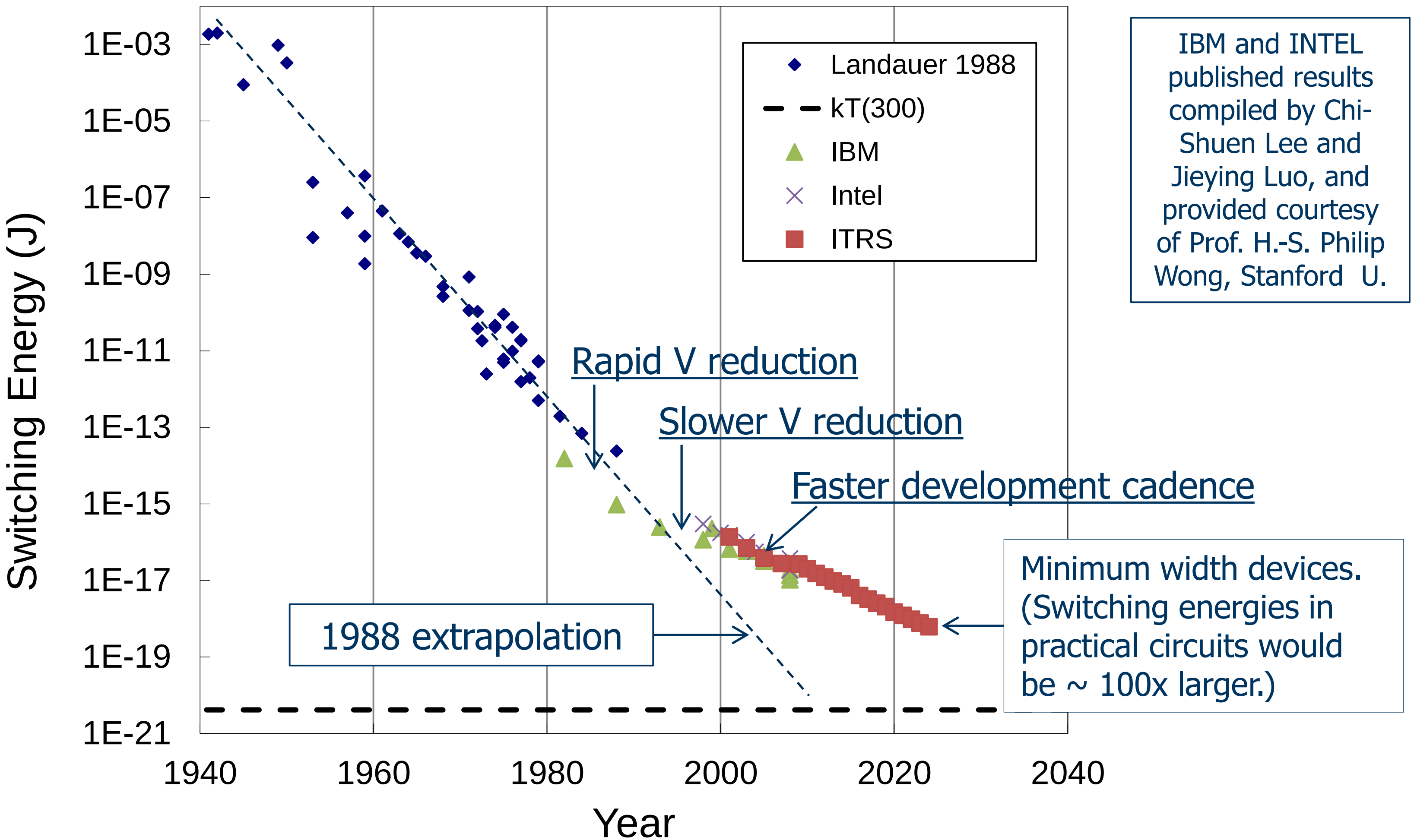
$$E = \frac{1}{2} C V^2 \left(\frac{2RC}{T} \right)$$

(T >> RC)

Topics

- Post-CMOS Device Research – the Need and the Vast Opportunity
- Growing Research Investment
- Two Broad Classes of Emerging Devices
  - “Steep Slope” Devices (TFETs and More)
  - Nanomagnetic Devices (Spintronics)
- Device Performance Benchmarking: Comparing and Evaluating Emerging Devices
- Conclusion: Devices *and* Architectures – the Unexplored Research Landscape

Minimum Switching Energy for Logic: A Long View

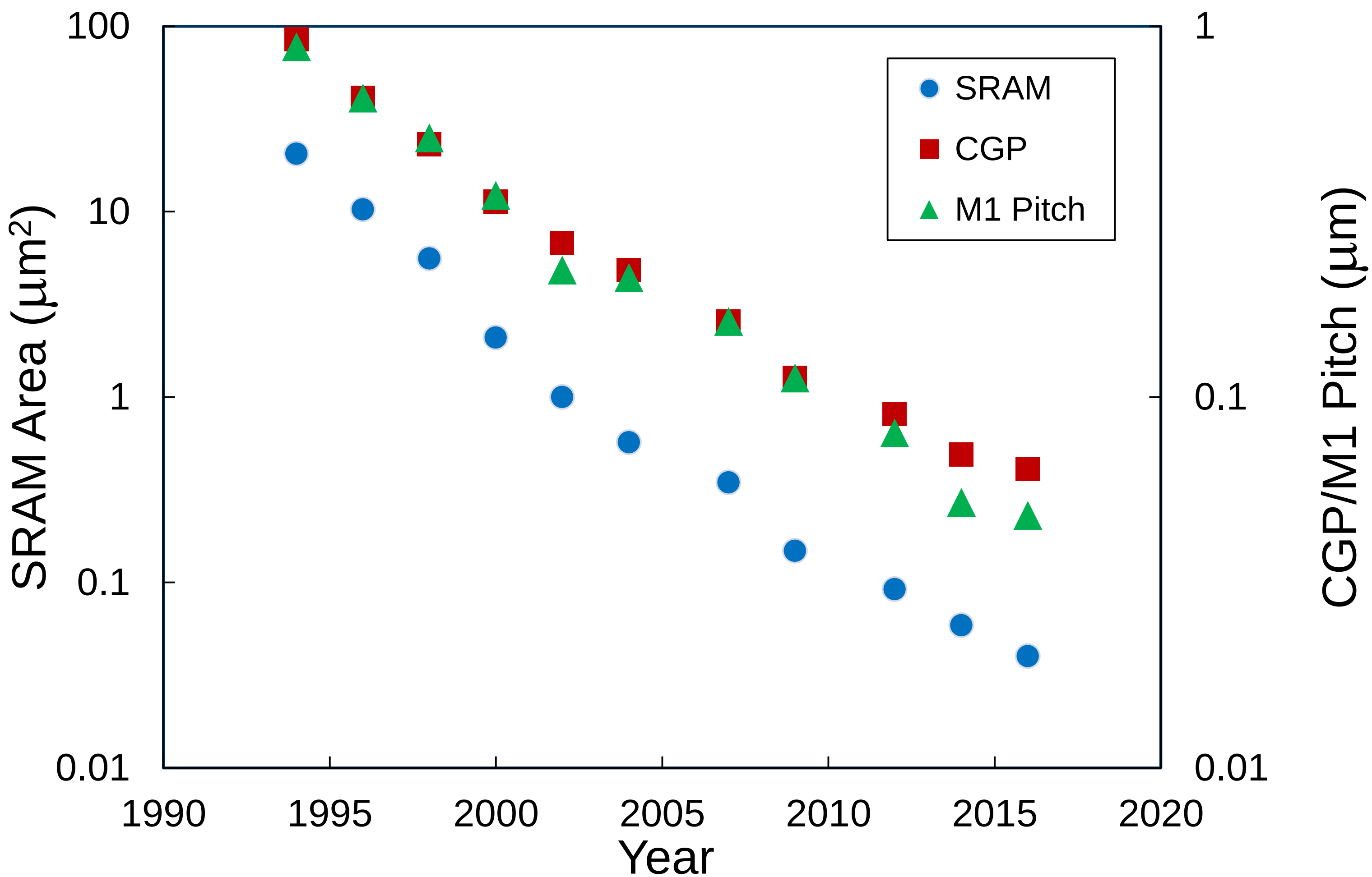


IBM and INTEL published results compiled by Chi-Shuen Lee and Jieying Luo, and provided courtesy of Prof. H.-S. Philip Wong, Stanford U.

T.N. Theis and H.-S. P. Wong, Computing in Science and Engineering, to be published.

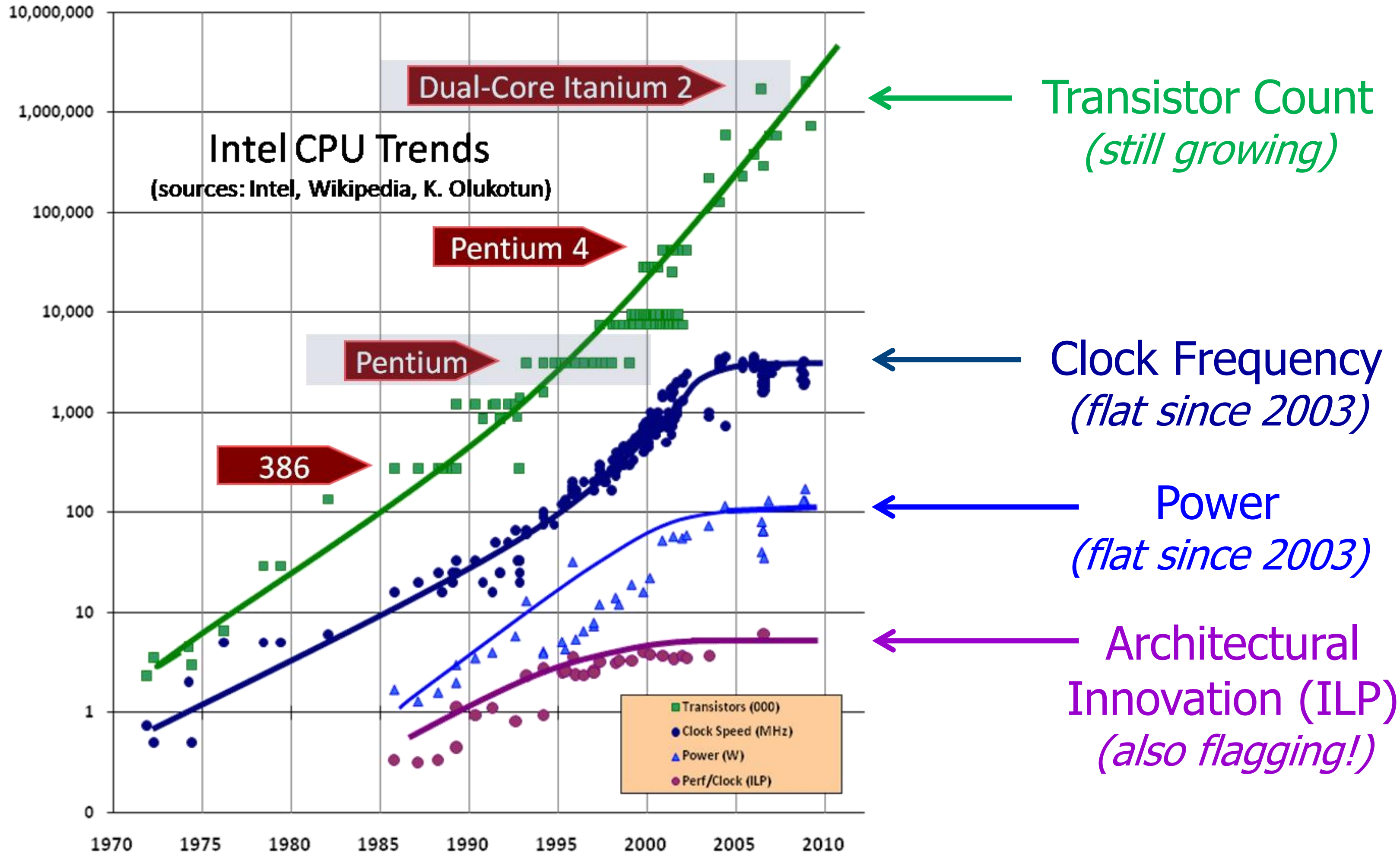
Key Indicators of Integration Density

Progress continues, but appears to be gradually slowing.



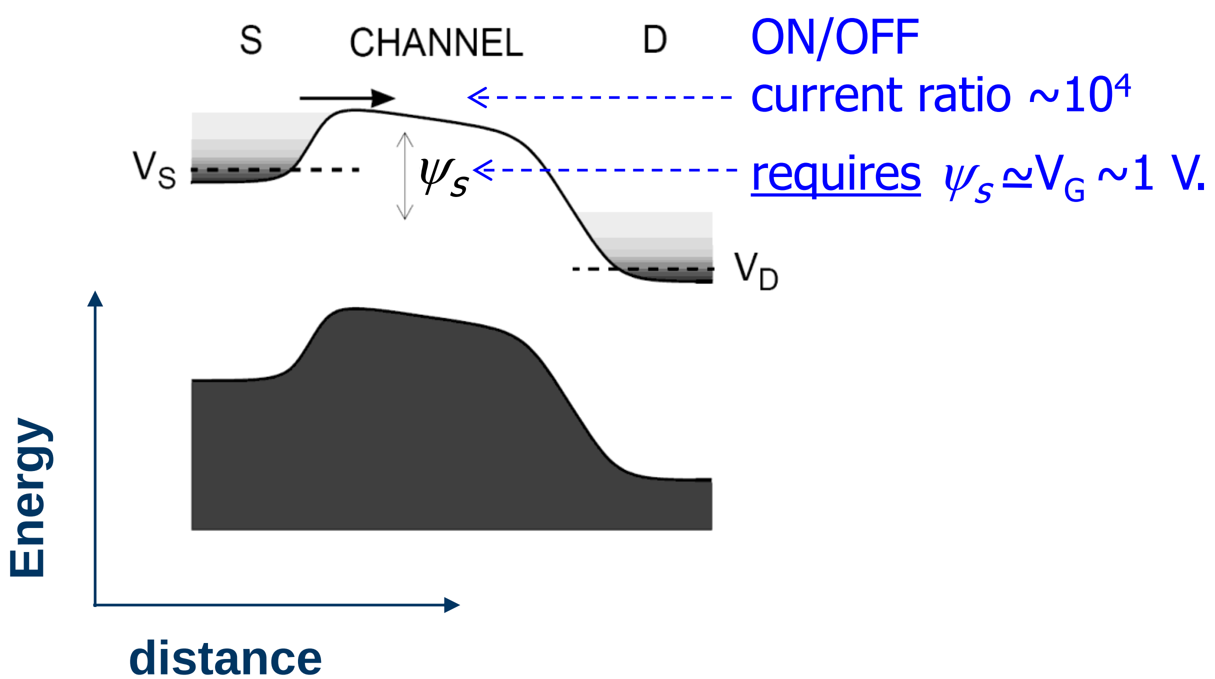
T.N. Theis and H.-S. P. Wong, Computing in Science and Engineering, to be published.

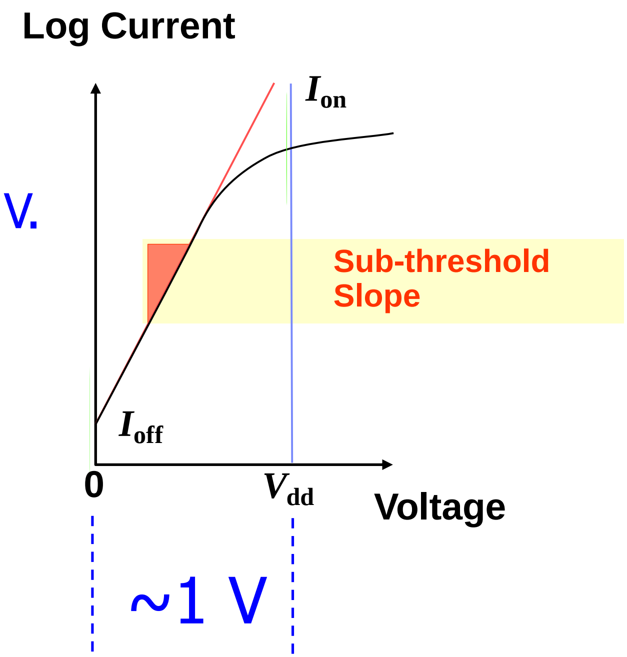
Computer clock frequencies have been stagnant since 2003.



http://www.gotw.ca/publications/concurrency-ddj.htm

Transistor operating voltage can no longer be reduced along with device dimensions.





With voltage swing already reduced to ~ 1V, The FET is close to its fundamental voltage limit for operation at ambient temperatures.

Consequences of Moving from Constant Field toward Constant Voltage Scaling

	Scaling Scenarios			
	Const. Field	Constant V		
		Max. f	Const. f	Multi-core
L_{gate}	$1/\alpha$	$1/\alpha$	$1/\alpha$	$1/\alpha$
W, L_{wire}	$1/\alpha$	$1/\alpha$	$1/\alpha$	$1/\alpha$
V	$1/\alpha$	1	1	1
C	$1/\alpha$	$1/\alpha$	$1/\alpha$	$1/\alpha$
$U_{stor} = ½CV^2$	$1/\alpha^3$	$1/\alpha$	$1/\alpha$	$1/\alpha$
f	α	α	1	1
$N_{tran}/core$	α^2	α^2	α^2	1
N_{core}/A	1	1	1	α
P_{ckt}	$1/\alpha^2$	1	$1/\alpha$	$1/\alpha$
P/A	1	α^2	α	1
$f\,N_{tran}\,N_{core}$	α^3	α^3	α^2	α

System Performance

Theis and Solomon, IEEE Proceedings **98**, pp. 2005-2014, Dec. 2010

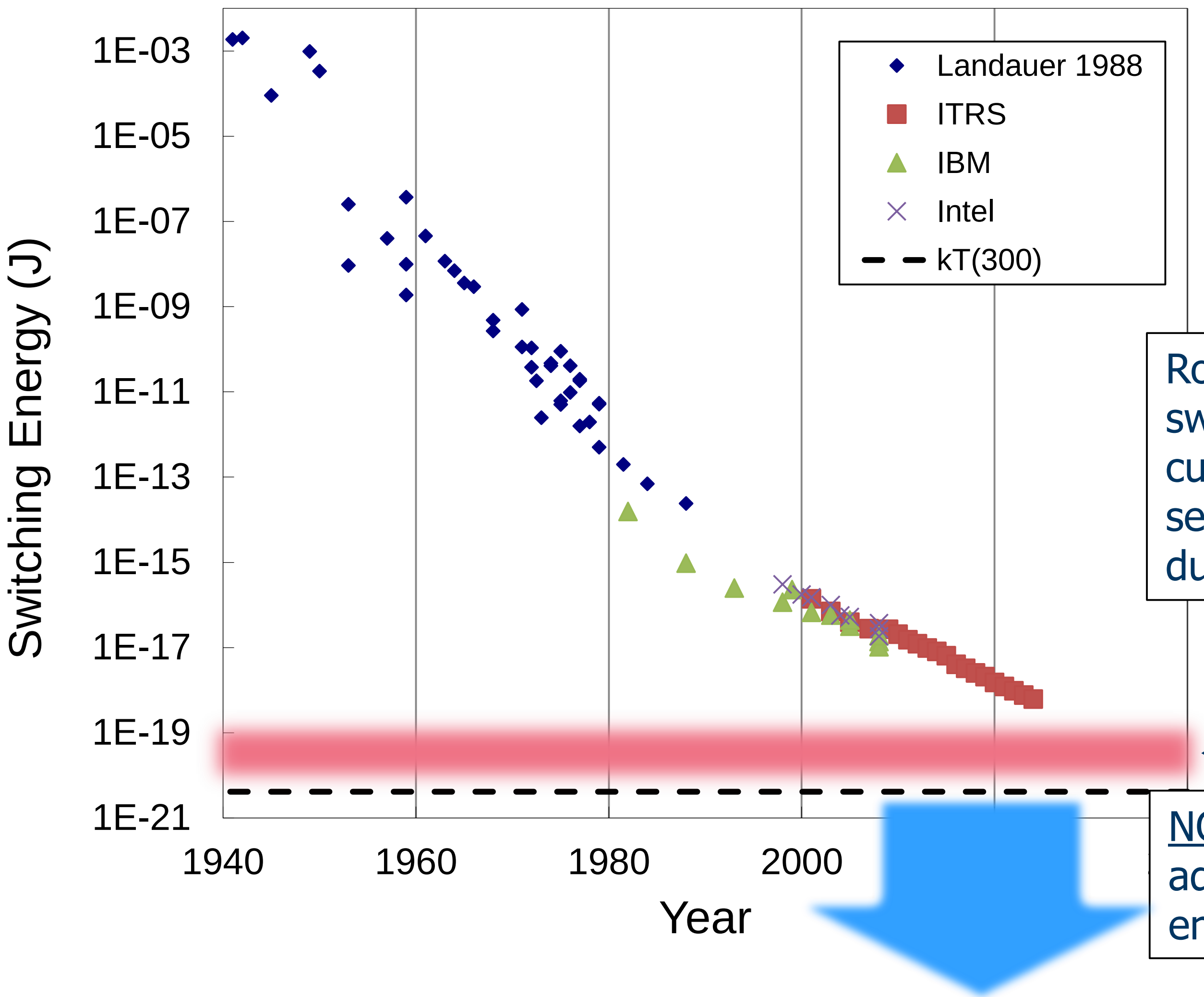
To change this outcome, we must fundamentally change the underlying device physics!

Briefly summarizing the last 10 years…

- To keep areal power density and total power within economically acceptable limits, industry froze clock speed and slowed the deployment of multiple cores.
  (See the simple constant voltage scaling argument by T.N. Theis and P.M. Solomon, “In Quest of the ‘Next Switch’: Prospects for Greatly Reduced Power Dissipation in a Successor to the Silicon Field-Effect Transistor,” IEEE Proc. 98, 2005–2014, Dec. 2010.)

- To escape this new status quo, we’ve begun to explore devices with switching mechanisms that are fundamentally different from that of the conventional FET, and architectures than are fundamentally different from the von Neumann architecture.

The Unexplored Research Landscape



Rough limit for abrupt switching (i.e. nearly all current device research) set by tolerable error rate due to thermal upsets.

<u>NO</u> lower limit for adiabatic switching in energy-conserving circuits.

Paths to (Truly) Low-power Logic

Focus of most post-CMOS device research

1. Abrupt Switching (i.e. Conventional Logic)
   Reduce the stored energy (½ CV^2 for the FET) toward some multiple of kT set by the tolerable rate of thermally induced errors. Use redundancy and error correction to keep the error rate in bounds.

2. Adiabatic Switching
   Maintain stored energy well above kT and implement adiabatic switching to reduce energy loss per switching event toward the Landauer erasure limit, kT ln(2).

Limited exploration to date

3. Reversible Logic
   Maintain stored energy well above kT, implement adiabatic switching, energy-conserving reversible logic circuits, and energy-recovering (i.e. resonant circuit) power supply to reduce energy losses per switching event, potentially to well below kT ln(2).

Well-funded research efforts

4. Quantum Computing

Growing Research Investments in New Devices and Architectures for Computing

Research funded by industry and government in recent years has given us a broader picture of what is possible.

- Founded in 2005, the Nanoelectronics Research Initiative (NRI) is a public-private partnership funding university research aimed at demonstrating *non-conventional, low-energy technologies for computation which can outperform CMOS on critical applications in ten years and beyond.*
- In 2013, NRI was joined in the focused exploration of post-CMOS devices by the former Focus Center Research Program, completely refreshed as STARnet.
- 3 NRI and 3 STARnet multidisciplinary, multi-university research centers are currently exploring a wide range of emerging device concepts, and stimulating additional research and invention by others.

NRI Research Centers

In Partnership with NIST

SRC Executive Director: An Chen

6 Universities

CNFD **Evgeny Tsymbal, Director**

The mission of CNFD is to develop low-energy memory and logic devices based on materials, structures, and phenomena non-traditional for existing technologies, such as magnetoelectricity, ferroelectricity, and spin dynamics, to advance the information technology beyond current limits.

8 Universities

INDEX **Alan Diebold Director**

The mission of INDEX is to discover and demonstrate nanoscale computing devices to extend Moore’s law beyond CMOS limits, organized around spin and graphene p-n junction logic devices and implemented in an advanced semiconducting fabrication facility.

7 Universities

SWAN **Sanjay Banerjee, Director**

The South West Academy for Nanoelectronics seeks to develop ultra-low power transistors based on novel single particle and collective tunneling effects in 2D materials such as graphene and transition metal dichalcogenides, as well as magnetoelectric switching on topological insulators.

STARnet Research Centers

In Partnership with DARPA

SRC Executive Director: Gilroy Vandentop

Beyond-CMOS Devices

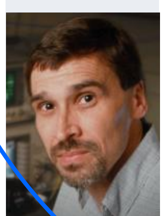
16 Universities

FAME Jane Pei-Chen Chang, Director
The mission of FAME is to create and investigate new nonconventional atomic scale engineered materials and structures of multi-function oxides, metals and semiconductors to accelerate innovations in analog, logic and memory devices for revolutionary impact on the semiconductor and defense industries.

14 Universities

C-SPIN Jian-Ping Wang, Director
The Center for Spintronic Materials, Interfaces and Novel Architectures (C-SPIN) seeks to overcome barriers to realizing practical spin-based memory and logic technology by assembling experts in magnetic materials, spin transport, novel spin-transport materials, spintronic devices, circuits, and novel architectures.

10 Universities



LEAST Alan Seabaugh, Director
The Center for Low Energy Systems Technology (LEAST) explores the physics of new materials and devices to enable more energy-efficient integrated circuits and systems.

New Architectures

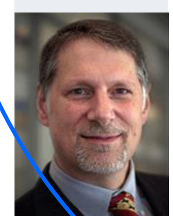
10 Universities

TerraSwarm Edward A. Lee, Director
The TerraSwarm Research Center aims to enable the simple, reliable, and secure deployment of a multiplicity of advanced distributed sense control-actuate applications on shared, massively distributed, heterogeneous, and mostly uncoordinated swarm platforms through an open and universal systems architecture.

8 Universities

SONIC Naresh Shanbhag, Director
SONIC will be guided by the following mission: To enable equivalent scaling in beyond-CMOS nanoscale fabrics by embracing their statistical attributes within statistical-inference-based applications, architectures, and circuits, to achieve unprecedented levels of robustness and energy efficiency.

15 Universities

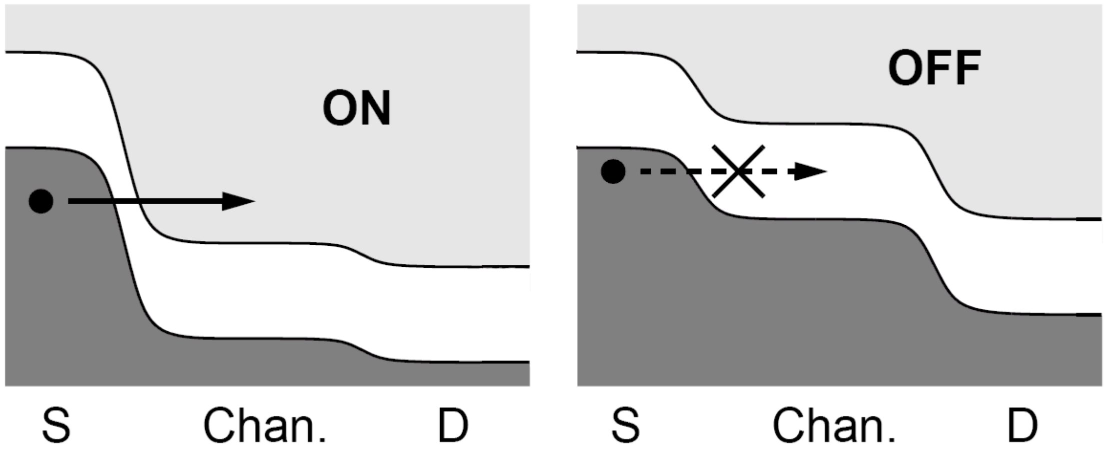


C-FAR Todd Austin, Director
The center's research agenda is guided by three initial technical vectors, whose intersections will help realize non-conventional architectures that address these pressing challenges: data-centric architectures, novel architectures based on emerging technologies, and beyond homogenous parallelism.

“Steep Slope” Devices

How long does it take to truly understand the potential of a promising device concept?

Let's consider today's most-studied emerging device – the Band-to-Band Tunneling Field Effect Transistor or TFET

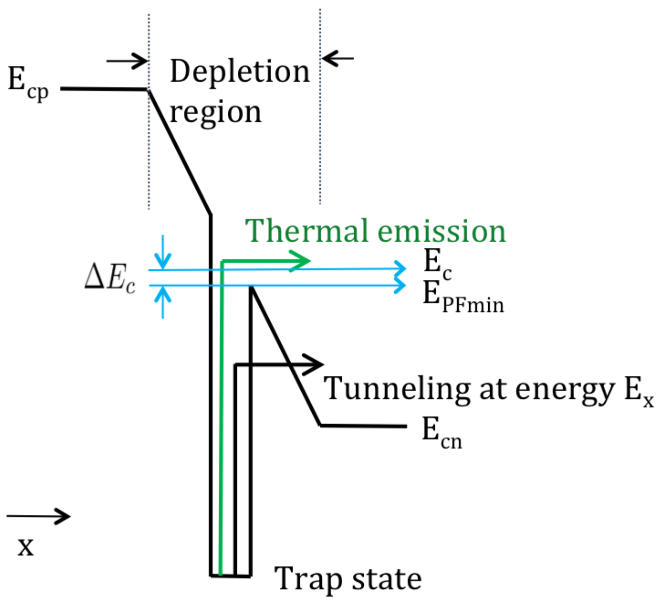


A Very Brief History of TFET Research

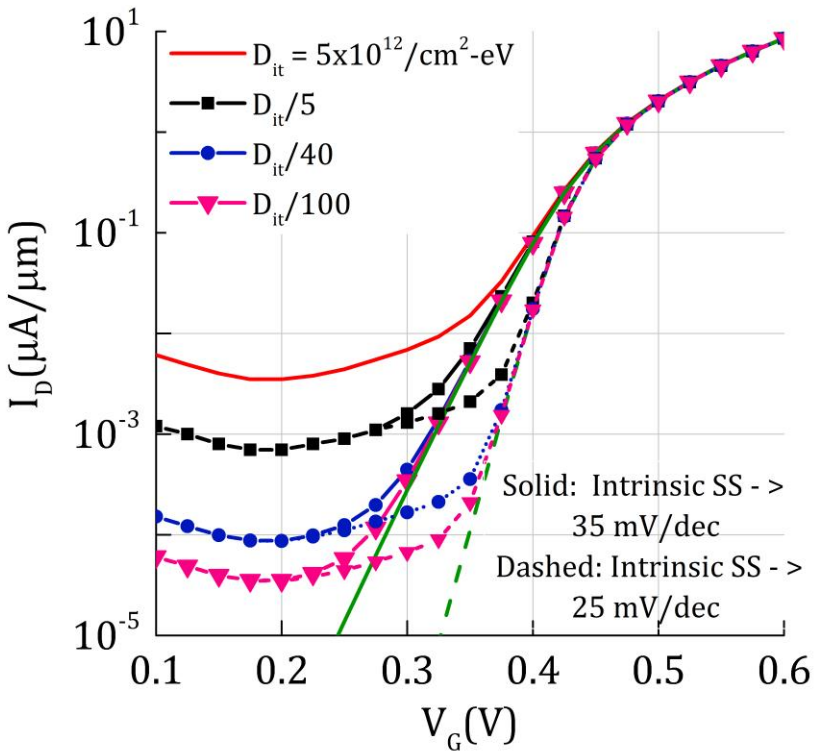
- 1989: First report of gated tunneling
  S. Banerjee *et al.*, IEEE Electron Device Lett. **EDL-8**, pp. 347–349, Aug. 1987.
- 2005: SS less than 60 mV/decade in CNT TFET
  Appenzeller, *et al.*, Phys. Rev. Lett. **93**, art. 196805, Nov. 2004.
- 2007: DARPA STEEP program focuses on Si and Si-Ge TFETs
- 2009: III-V broken-gap heterojunction TFET proposed
  S. O. Koswatta *et al.*, IEDM 2009.
- 2013: Prediction of new ultra-low power design space opened by TFETs U. Avci and I. Young, IEDM 2013.
- Current:
  - New TFET variants continue to emerge
    (i.e. graded composition nitrides; P. Fay *et al.*, Notre Dame)
  - <u>But</u> subthreshold slope in high-current (i.e. fast switching) devices continues to disappoint, and the fundamental leakage mechanisms that may explain this are still poorly understood.

Trap Assisted Tunneling

- Limits attainable range of steep subthreshold slope.
- In III-V's, D_{it} reduction by ~40x (→10^{11}/cm^2-eV) may be required.
  Sajjad *et al.*, arXiv:1603.06654v1 [cond-mat.mes-hall] 22 Mar 2016



Model

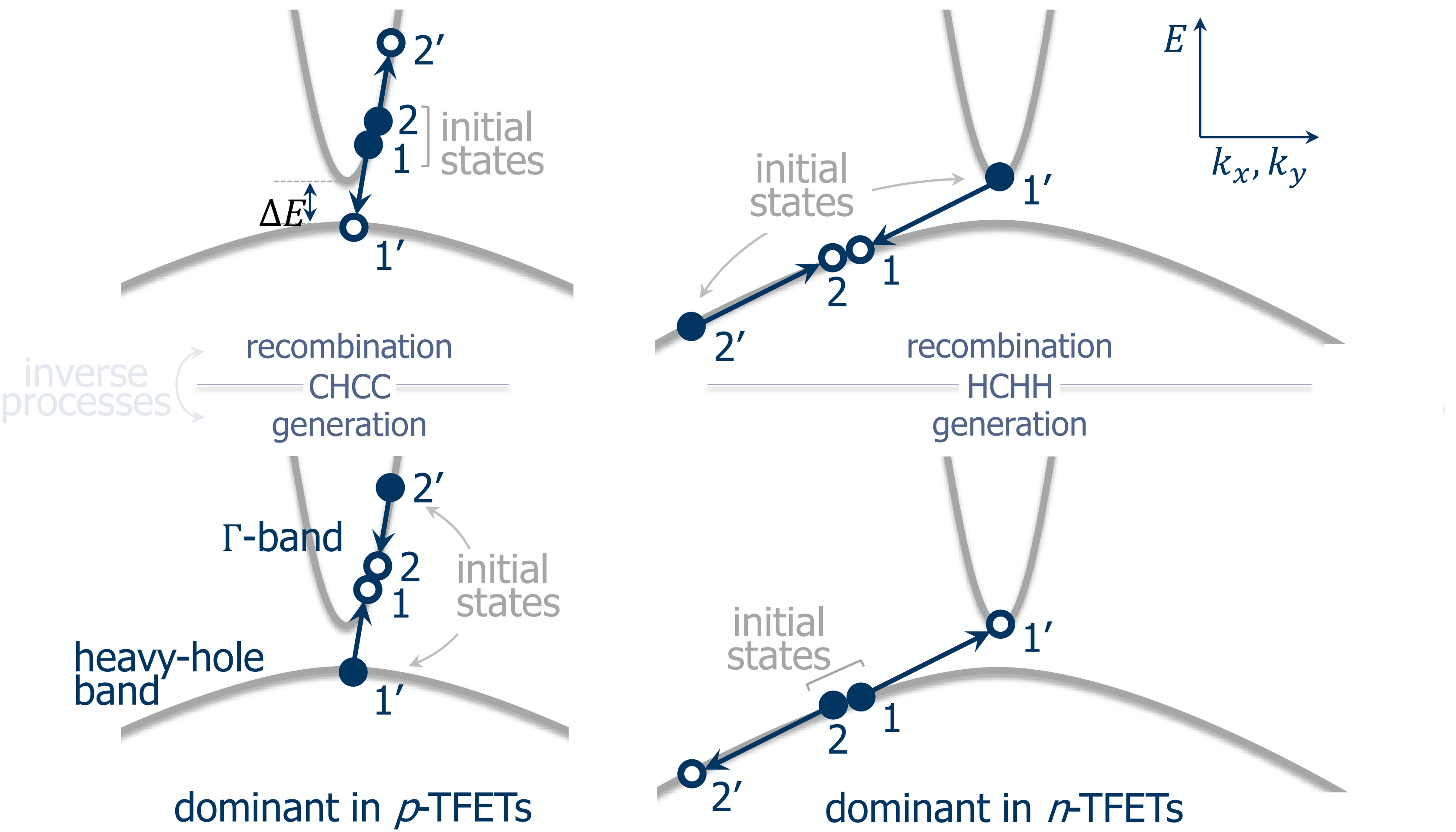


Calculated Transfer Characteristic

Generation/Recombination

A fundamental leakage mechanism

J. J. Teherani, *et al.*, J. Appl. Phys. 120, 084507 (2016)



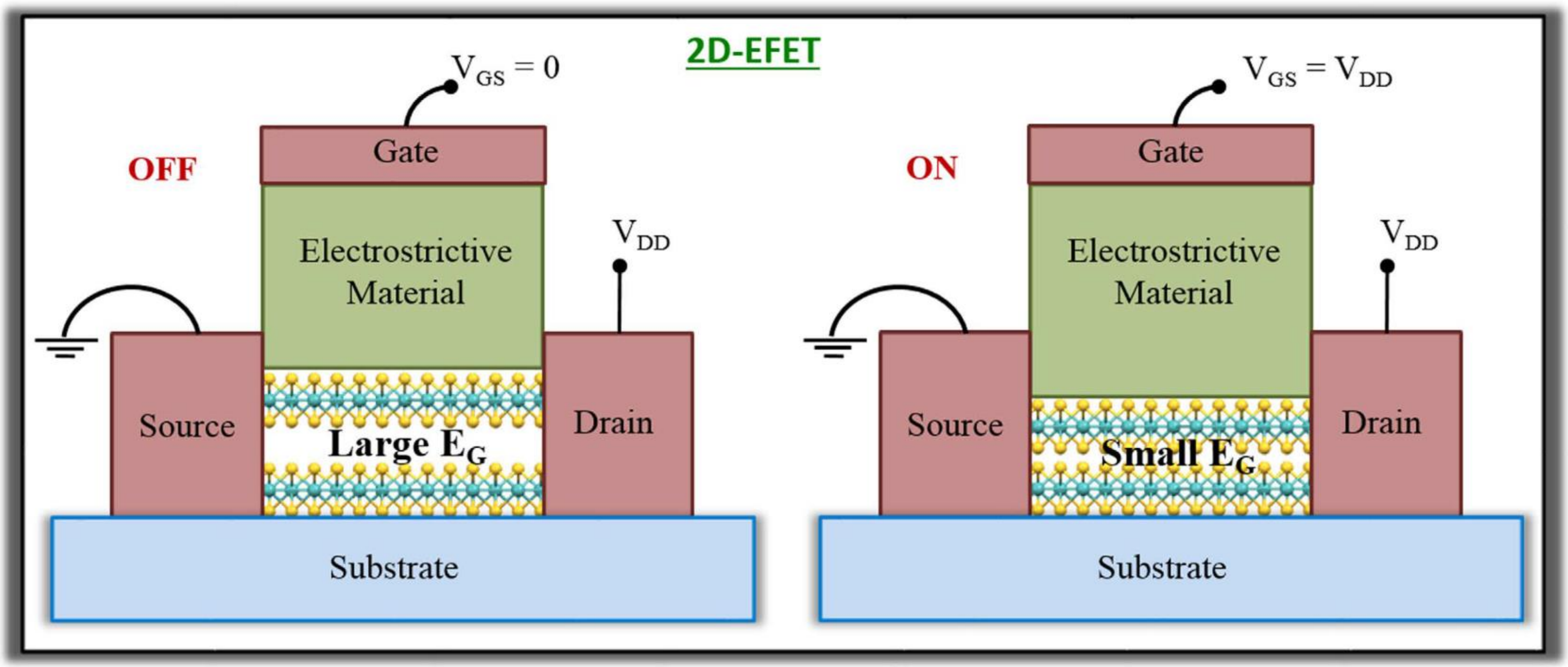
Newer steep slope device concepts continue to emerge.

- Negative Capacitance FET
  Salahuddin and Datta, Nano Lett., 2008, 8 (2), pp 405–410.
- Graphene p-n Junction (GPNJ) Device
  NRI INDEX center
  R.N. Sajjad and A. W. Gosh, arXiv:1305.7171, May 2013
- Piezoelectronic Transistor (PET; solid-state relay)
  D.M. Newns, B.G. Elmegreen, X.-H. Liu and G.J. Martyna,
  J. Appl. Phys., vol. 111, art. 084509, 2012
- PiezoFET
  STARnet LEAST center
  R. K. Jana, G. L. Snider, and D. Jena, *physica status solidi (c)*, vol. 10, no. 11, pp. 1469-1472, November 2013
- and more …

Electrostrictive Field Effect Transistor

Saptarshi Das, Scientific Reports, 2016; 6: 34811.

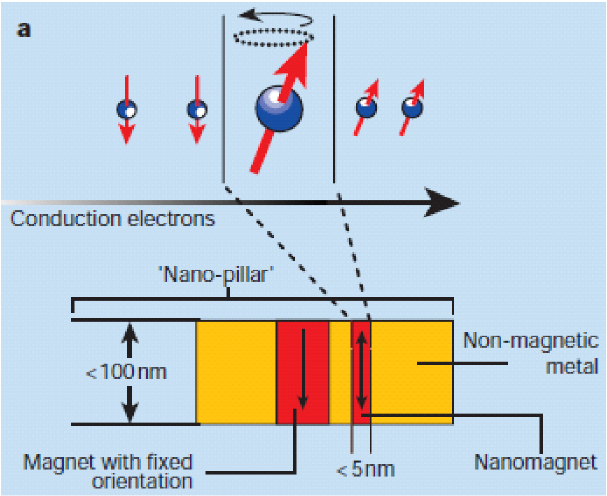
- voltage → pressure transduction enables steep slope
- Predicted high ON current



Nanomagnetic Devices

Modifying magnetization by spin currents

- Current, when passing through a ferromagnet, becomes spin-polarized
- Conduction electron spins exert a torque on magnetic moments: Spin-transfer torque (STT)
- STT can flip magnetization (spin valves, MTJs) or move domain walls
- Effect is unrelated to classical effects of moving charge, i.e. magnetic field, Lorentz force, Joule heating



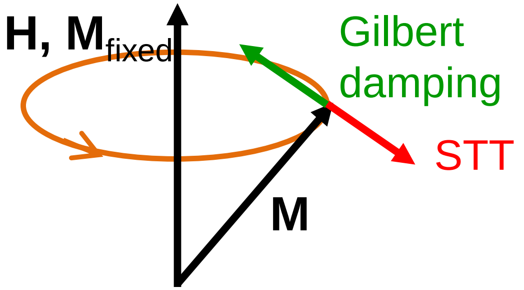
Magnetization of free layer in MTJ can be switched back and forth by switching current direction

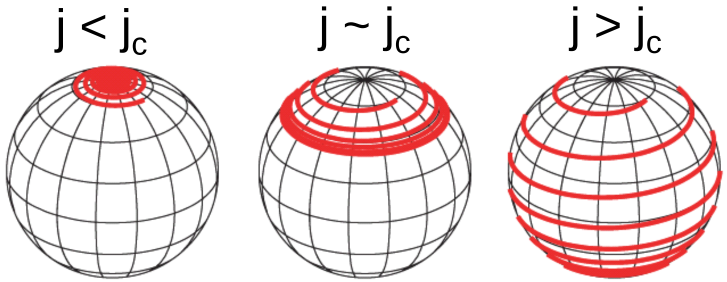
Berger, J. Appl. Phys. **55**, 1954 (1984)
Slonczewski, JMMM **159**, L1 (1996)
Berger, Phys. Rev. B **54**, 9533 (1996)

Spin torque Switching: The equation

- MTJ reversal:

$$\frac{d\vec{M}}{dt} = \gamma\,(\vec{M} \times \vec{H}_{eff}) + \frac{\alpha}{M}\,(\vec{M} \times \frac{d\vec{M}}{dt}) + \eta\, j\, \mu_B(\vec{M} \times (\vec{M} \times \vec{M}_{fixed}))$$



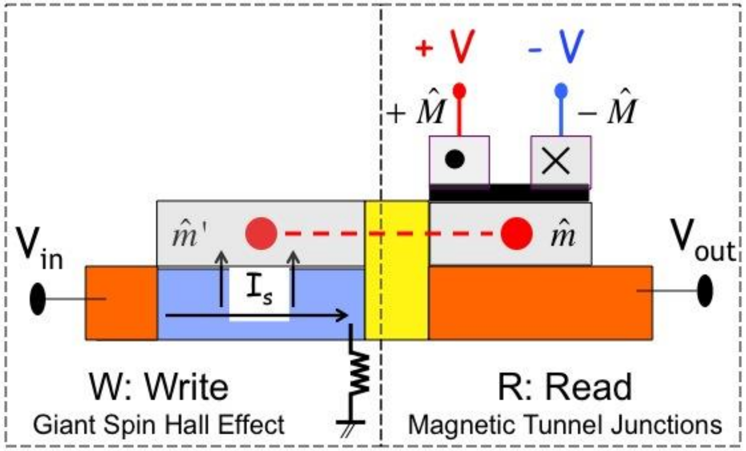


- Dynamics of domain wall motion requires some additional terms

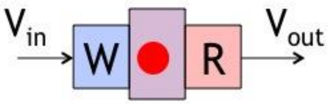
Charge-controlled Spin Logic

Datta, Salahuddin, and Behin-Aein, Appl. Phys. Lett. 101, 252411 (2012)

Spin switch



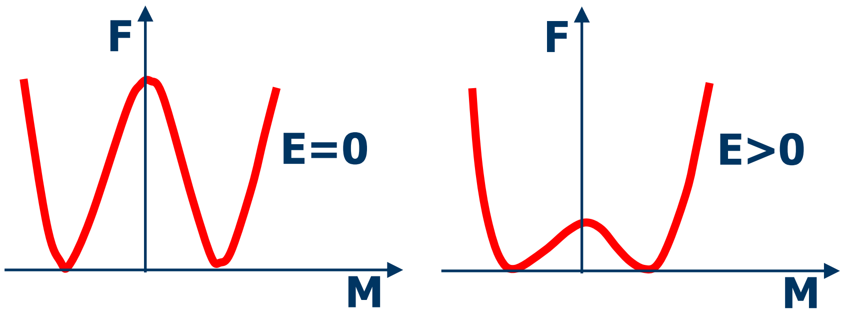
Symbol



- Read-magnet (m) dipole-coupled to Write-magnet (m') provides electrical *isolation* between them, which simplifies the design of circuits.

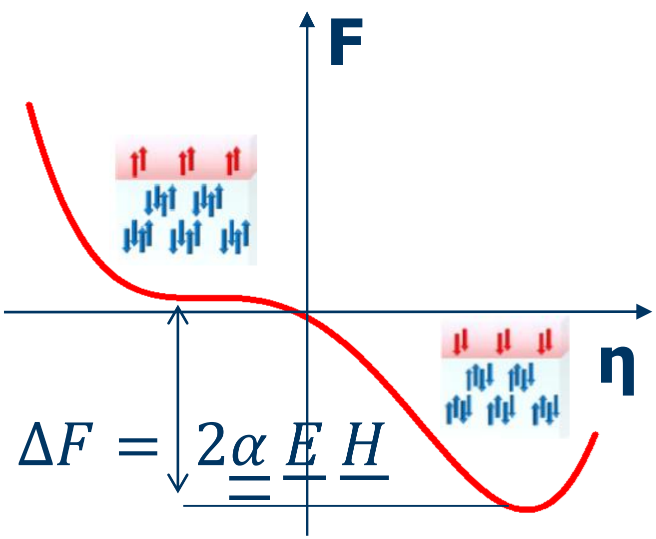
- Predicted gain and fan out capability → fully *concatenating* logic

Voltaged-switched (Magnetoelectric) Devices:
Two Mechanisms for Magnetization Reversal



Voltage Controlled Anisotropy

No thermodynamically preferred state, but precise timing of voltage pulses allows deterministic switching.
J.T. Heron *et al*., Nature **516**, 370 – 373, (2014).



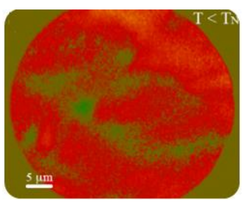
Voltage Controlled Exchange Bias

Applied voltage determines the thermodynamically preferred state.
X Hie *et al*., Nature Materials **9**, 579–585 (2010).

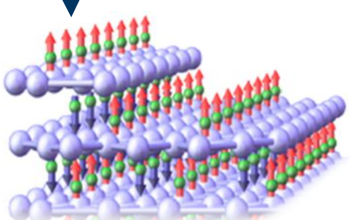
Magnetoelectric Antiferromagnets for Ultra-low Power Memory and Logic Device Applications

Goal: Voltage-switched ultra-low power MRAM
Approach: Reversal of free FM layer in perpendicular magnetic tunnel junction (p-MTJ) in the absence of electric current, based on voltage switching of the boundary magnetization in an antiferromagnetic thin film.

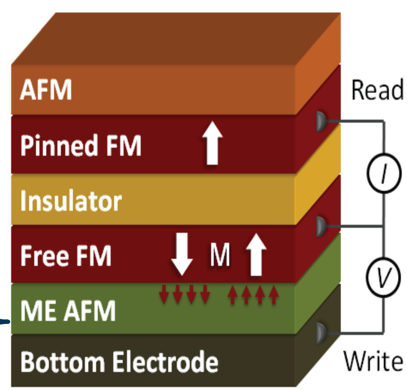
Boundary magnetization (BM) is a roughness insensitive generic property of antiferromagnetic materials.
K.D. Belashchenko, Phys. Rev. Lett. **105**, 147204 (2010)



XMCD-PEEM of BM



Magnetoelectric (ME) Cr_2O_3



Read out of non-volatile memory state through tunnel magneto-resistance of p-MTJ or potentially through inverse ME effect

Magnetization orientation of FM layer is voltage - controlled through BM of ME antiferromagnet

What are the prospects for these devices?

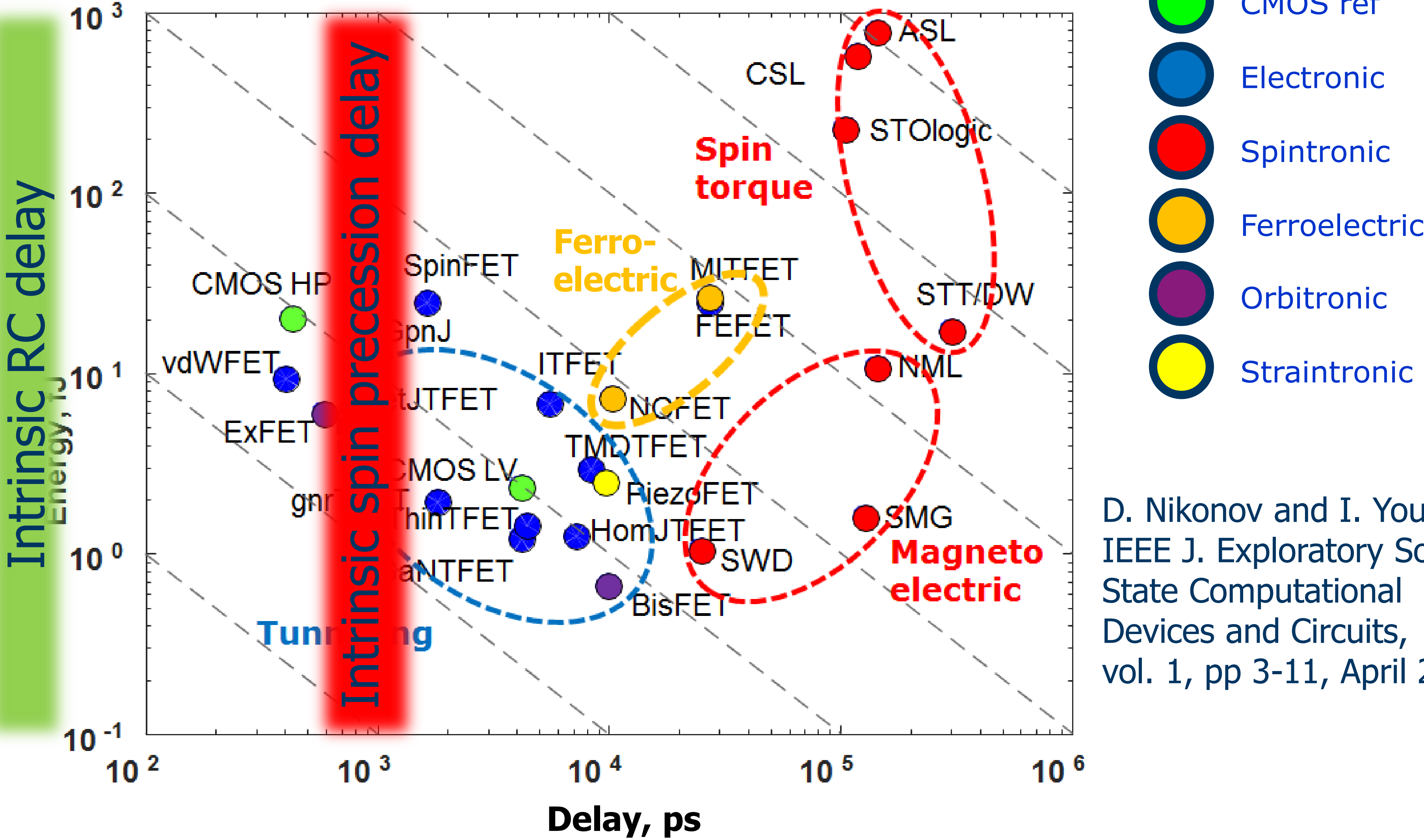
How can we compare them to each other and to CMOS?

NRI-STARnet Device Performance Benchmarking

- Selected Family of Representative Circuits
- Uniform Engineering Assumptions
- Increasingly Rigorous Compact Device Models

2015 Benchmarking Results:
NRI and STARnet Device Concepts

Energy vs. Delay for 32 Bit Adder Circuit



D. Nikonov and I. Young, IEEE J. Exploratory Solid-State Computational Devices and Circuits, vol. 1, pp 3-11, April 2015

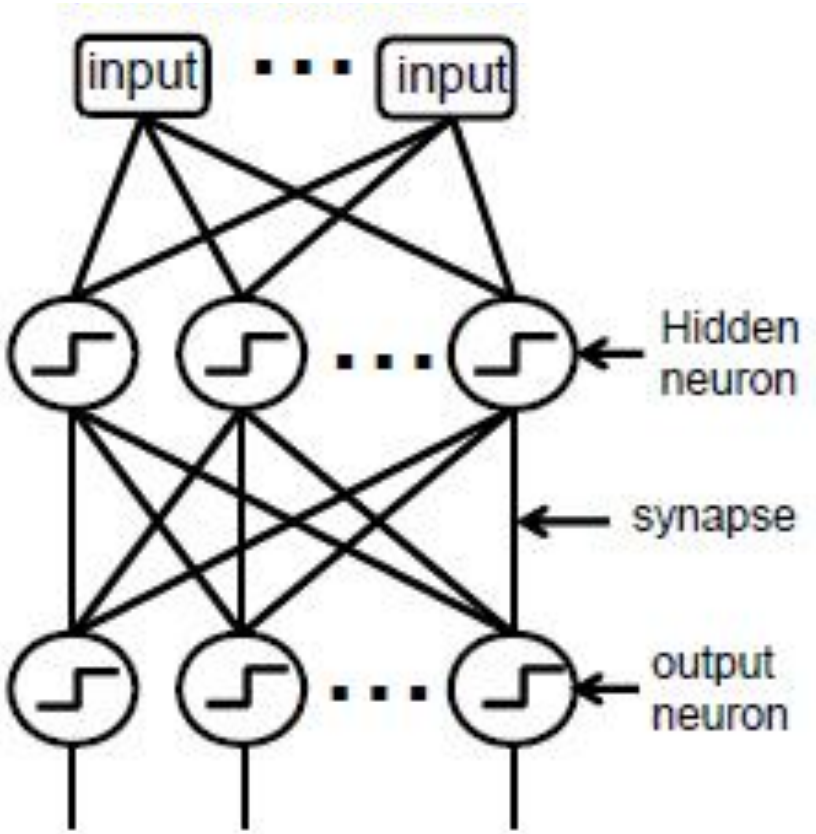
Takeaways from 5 Years of Benchmarking

- As device models improve, estimates of device attributes tend to become more conservative (and more accurate).
- While no clear winner has emerged, the number of device concepts benchmarked as competitive with CMOS has increased.
- New device concepts continue to emerge, suggesting that more (perhaps many more) *are yet to be invented.*

An Assessment of Current Device Research

- The rate of invention of new device concepts is increasing. It is therefore unlikely that we have already found the ultimate switch for digital computing.
- No truly new device will be a “drop in” replacement for the CMOS FET. Devices and circuits must be co-developed.
- Some devices may have characteristics that are particularly well suited to new and emerging architectures for computing.

As one example of a broad class increasingly important architectures, consider a Feed–forward Neural Network.

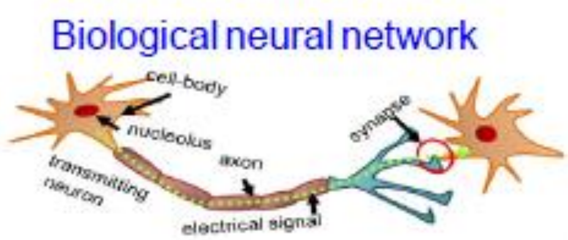


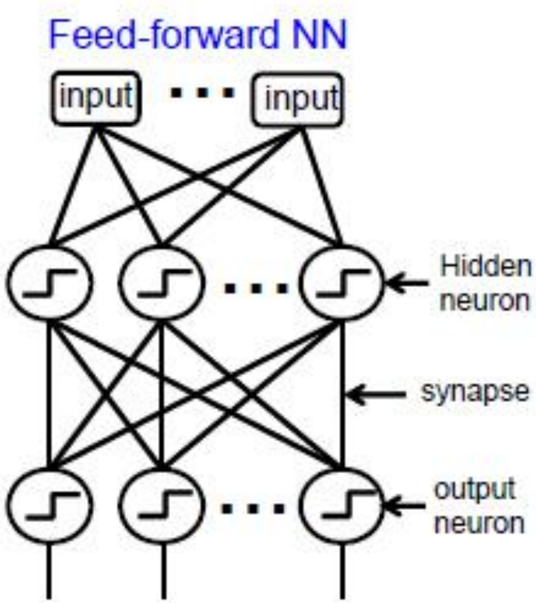
The computation in each node is simple.

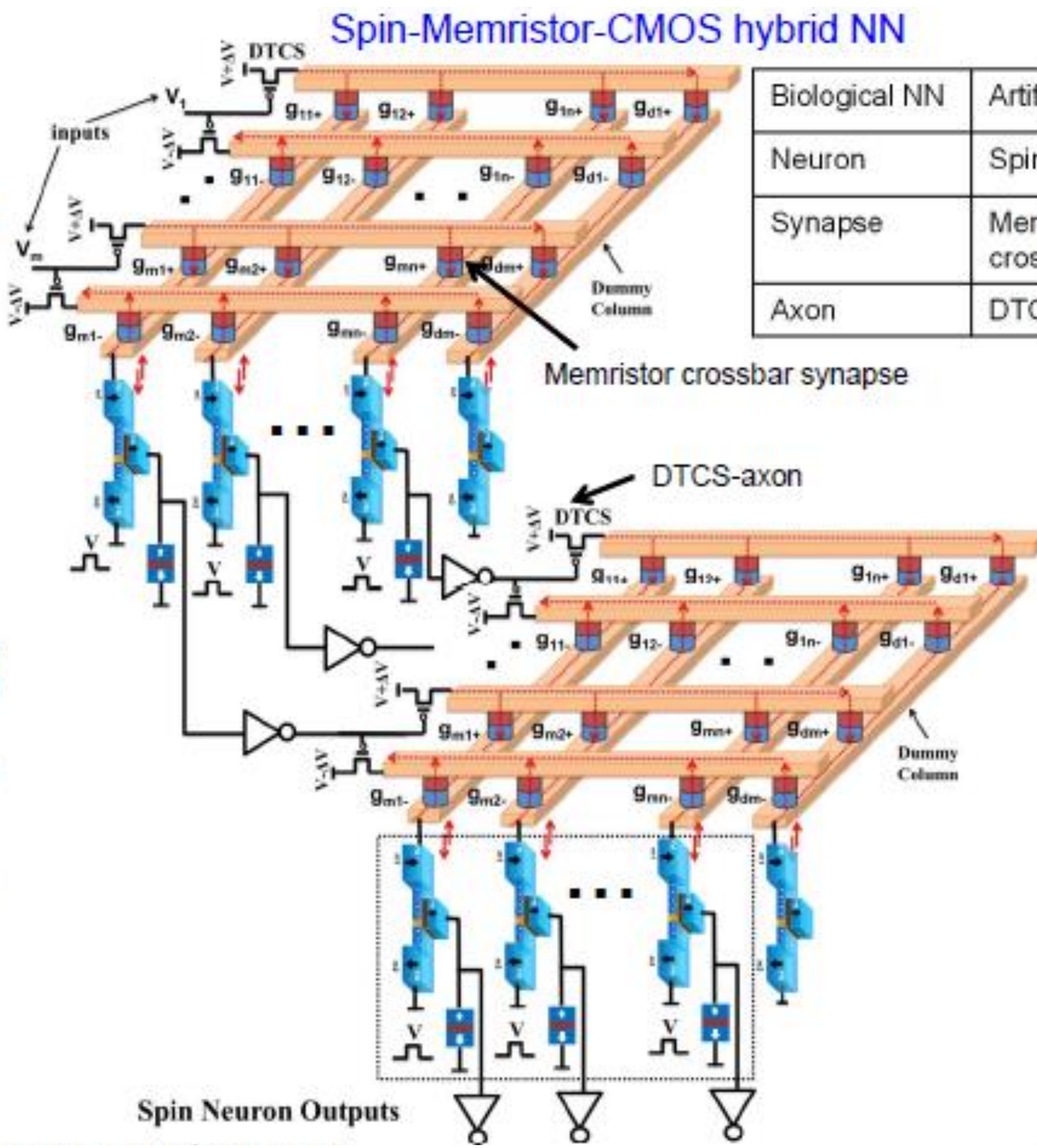
Can it be done by a single device?

Spin-Neuron Based Feed-Forward Neural Network

Sharad, Fan, Roy et al. DAC 2013/ TNANO 2014/ JAP 1014





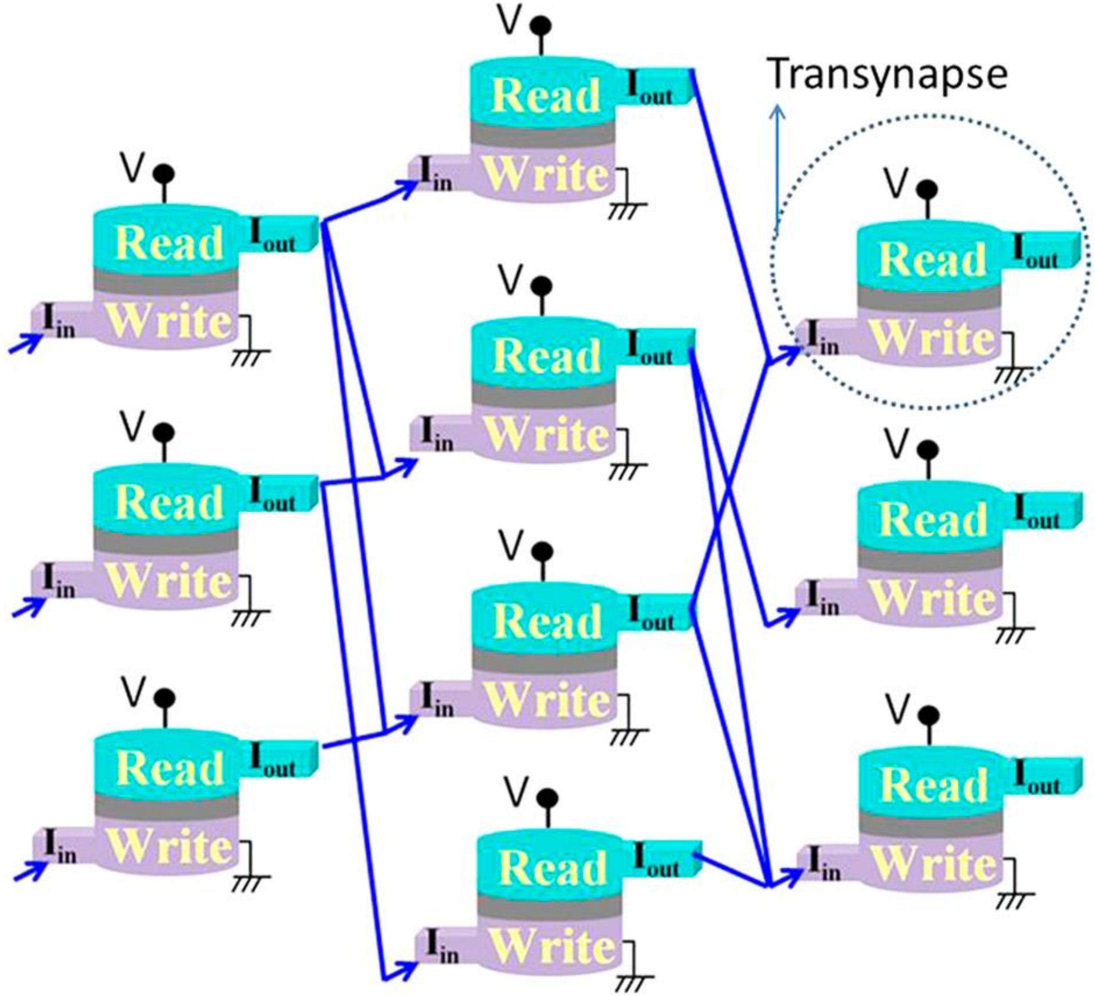


Biological NN	Artificial NN
Neuron	Spin-Neuron
Synapse	Memristor crossbar
Axon	DTCS

Another Example: The Transynapse

"A building block for hardware belief networks"

B. Behin-Aein, V. Diep, S. Datta - arXiv preprint arXiv:1606.00130, 2016

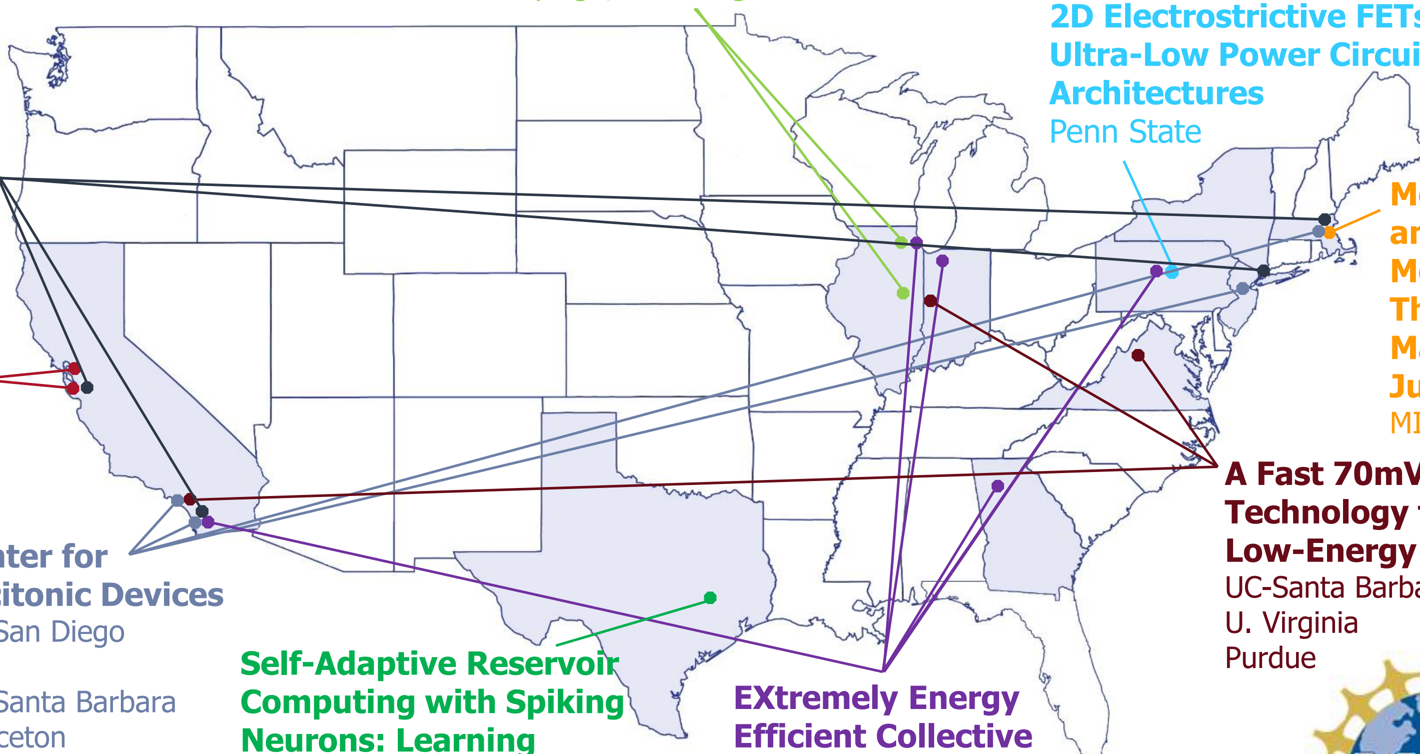


The Unexplored Research Landscape:

New Devices *and* New Architectures

E2CDA

Energy Efficient Computing: from Devices to Architectures
Funding 15 Universities in 10 States



Conclusion

Looking beyond conventional FETs and the von-Neumann architecture, there is a lot to explore!

Exploration of new devices and architectures for computing will drive materials research for many more years.

Thanks!